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Soft-Switched Resonant DC-DC Converter in Underwater DC Power Distribution Network

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SOFT-SWITCHED RESONANT DC-DC CONVERTER IN UNDERWATER DC POWER DISTRIBUTION NETWORK

by

Tarak Saha

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ABSTRACT

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Converters used in underwater system require operation with high reliability with little to no maintenance due to their geographical locations. Resonant converters offer quiet and efficient operation with low EMI due to low di/dt and dv/dt owing to sinusoidal current and/or voltage and soft-switching. This makes resonant converters an excellent choice for reliable, long term operation in underwater distribution system. However, designing

resonant converters with constant current input imposes certain challenges as compared voltage source input, which are analyzed in this work. Addressing these challenges it is shown how different resonant power conversion topologies can be suitably selected and designed to meet the end goal of regulating its output current or voltage for wide range of loads. Soft switching requirements of these topologies are also investigated with appropriate solutions to ensure devices used in these converters switch with low loss and dv/dt. Some of the critical loads in the system demand bidirectional power transfer capability which is also presented in this work with befitting topology. Detailed modeling, analysis, design and experimental results from hardware prototypes are presented for all the converters in the system operating with 250 kHz switching frequency, regulating its output voltage or current from 1 A DC current source, up to a power level of 1 kW.

(237 pages)

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To my family...

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ACRONYMS

AC	Alternating current
DC	Direct current
HVDC	High voltage direct current
PWM	Pulse width modulation
LED	Light emitting diode
RC	Resonant converter
SRC	Series resonant converter
PRC	parallel resonant converter
AUV	Autonomous underwater vehicle
WPT	Wireless power transfer
EMI	Electromagnetic interference
ZVS	Zero voltage switching
ZCS	Zero current switching
AVC	Asymmetrical voltage cancellation
ADC	Asymmetric duty control
FHA	Fundamental harmonic approximation
RMS	Root mean square
PF	Power factor
UPF	Unity power factor
THD	Total harmonic distortion
MOSFET	Metal oxide semiconductor field effect transistor
VA	Volt-Ampere
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
DAB	Dual active bridge
PCB	Printed circuit board
PBU	Power branching unit

IRN	Input relay network
ORN	Output relay network
FPGA	Field programmable gate array
HDL	Hardware description language

CHAPTER 1

INTRODUCTION

Electricity is distributed in two forms – alternating current (AC) and direct current (DC). The electricity received at the household is AC and it comes from the generating station, transmitted at high voltage (up to hundreds of kV) over long distance and then stepped down by distribution transformer to lower voltage *e.g.* 120 V, 240 V etc. suitable for household appliances. The AC power system has the advantage of easy step up or step down through use of power transformer. Being alternating in nature, AC voltage/current goes through zero in every cycle which makes design of circuit breaker for protection easy and thus enables reliable power system operation. However, AC distribution is susceptible to the voltage drop on the line due to cable impedance (resistance, inductance and capacitance). Whereas, with DC distribution voltage drop on the line happens only due to cable resistance. This is advantageous for power distribution over long distance and thus DC or high voltage DC (HVDC) transmission [3, 4] is used in the power system where generation and distributions load are geographically apart. Transmission at HVDC has the added advantage of lower transmission loss owing to lower current in the line.

DC distribution is widely used in renewable solar energy harvesting through photovoltaic cells [5–7], data centers [8–10], telecommunication [11, 12], aircraft [13] etc. and in many more applications. A typical structure of DC distribution with multiple loads and converters connected to it is shown in Fig. 1.1. The loads connected to the main DC distribution bus (V_{DC1}) typically are DC-DC converters feeding their local loads or can create another isolated or non-isolated DC bus (V_{DC2}) where again set of loads get connected, as shown by blue in Fig. 1.1.

The DC distribution architecture with voltage source shown in Fig. 1.1 works well when the converters/loads are in close proximity to the source. However, if the converters/loads are distributed over long distance from the source then the source voltage drops across the

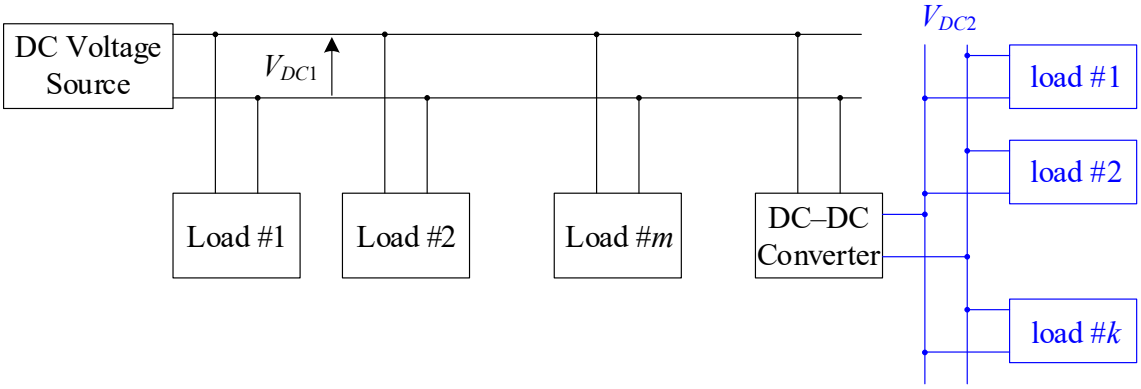


Fig. 1.1: DC voltage distribution architecture.

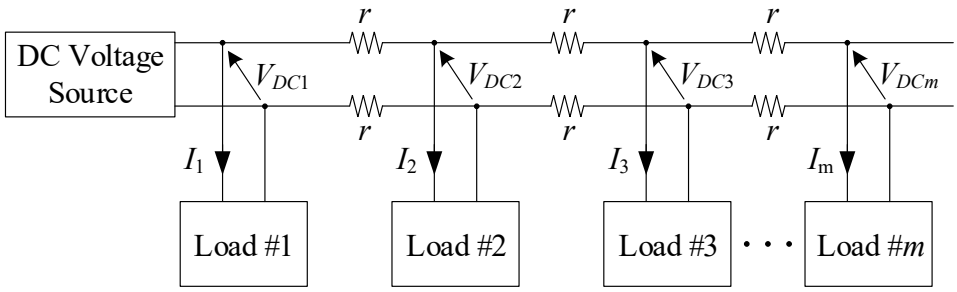


Fig. 1.2: DC voltage distribution architecture over long distance.

length of the distribution cable, due to cable resistance. This is shown in Fig. 1.2 where the input voltage at the each of the load(s) is of reduced magnitude than the preceding converters *i.e.* $V_{DCm} < \cdots < V_{DC3} < V_{DC2} < V_{DC1}$ due to voltage drop across the distribution line resistance (r). As an example, if all the load converters are of 1 kW with DC source voltage 100 V, ideally all the converter would draw 10 A with 100 V at its input. Now, if due to the line resistance, voltage at the last module drops to 80 V then for the same load, the first converter will be operating at 100 V, 10 A and the last one at 80 V, 12.5 A. If identical converters were used in this distribution network, all the converters need to be designed for the worst case voltage and current (100 V, 12.5 A) which means the converters have to rated for handling 1.25 kW, even though they are delivering only 1 kW. The situation can be worse if the distance (resistance) between source and farthest load/converter becomes very high.

DC current source is immune to any series non-idealities of the distribution line such

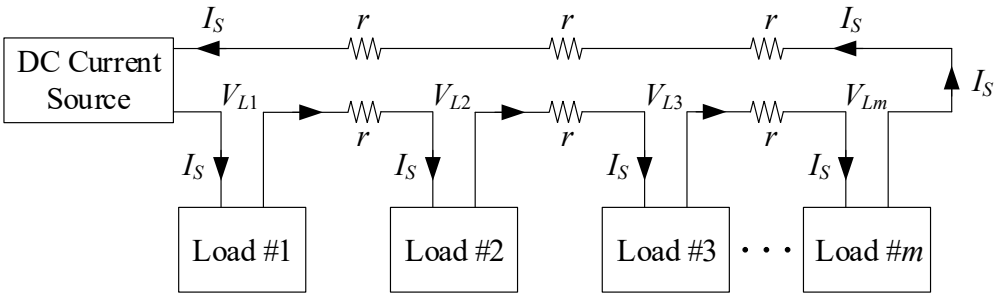
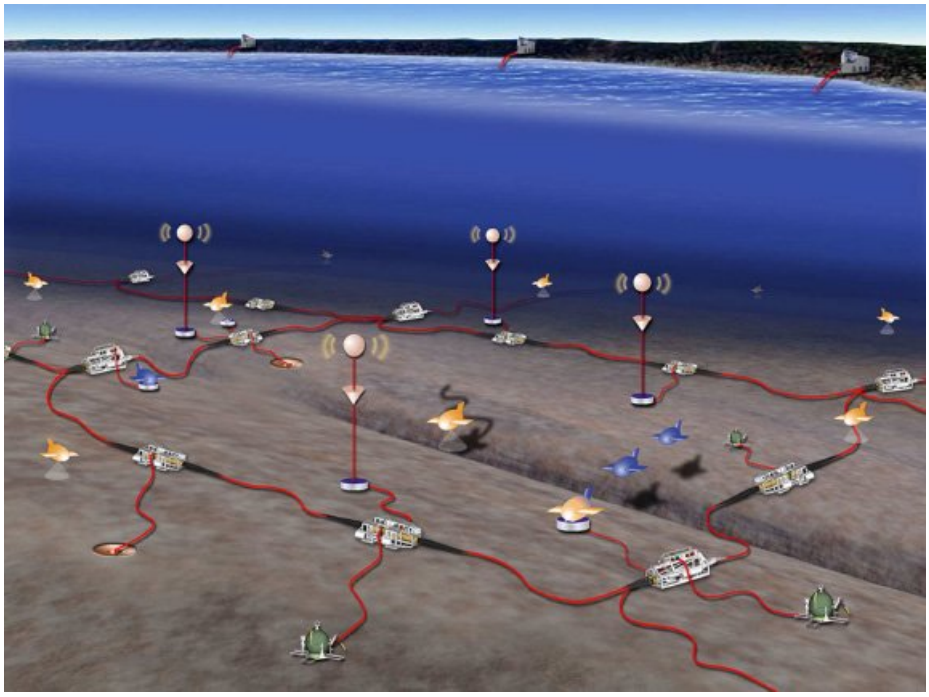


Fig. 1.3: DC current distribution architecture over long distance.

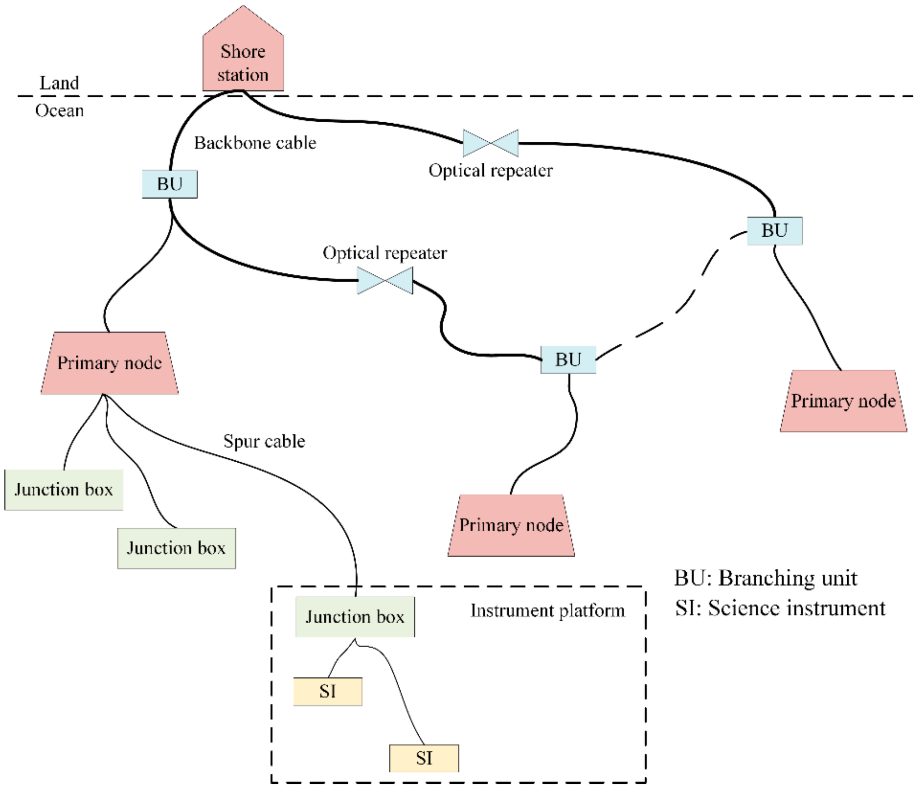
as resistance. This provides robustness against cable voltage drop by driving a constant current into the distribution line from which each of the load converters draw power for their respective load(s) which is shown in Fig. 1.3. As it can be seen from Fig. 1.3, all the load converters now operate from same input current of I_S, irrespective of their distance from the source. The input DC voltage for each of the converter(s) is now dependent on their individual load and if all the converters cater to same amount of load power, their input DC voltage will be same *i.e.* $V_{L1} = V_{L2} = V_{L3} = \cdots = V_{Lm}$. And hence, all the converters in the distribution network will see same maximum DC voltage and current and thus need not be over-designed.

1.1 Underwater Power Distribution

In recent times there is an increased interest in ocean exploration and underwater sensing for observation, marine resource development, earthquake and tsunami monitoring, etc. [1, 2, 14–24]. Power converter used in these applications are located deep into the sea and far from the shore. Because of long distance between the source and loads and among the loads, constant DC current distribution is used in this type of networks. The converters used in this system taps power from the constant current feed and provide power to their respective loads. The load can be a stationary local load or could be autonomous underwater vehicle (AUV) which can get charged through wireless power transfer (WPT) [25] or can be remote load demanding a sub-network of local constant current drive, as shown in Fig. 1.4(a) [1] and Fig. 1.4(b) [2].



(a)



(b)

Fig. 1.4: Underwater distribution system (a) from [1] and (b) from [2].

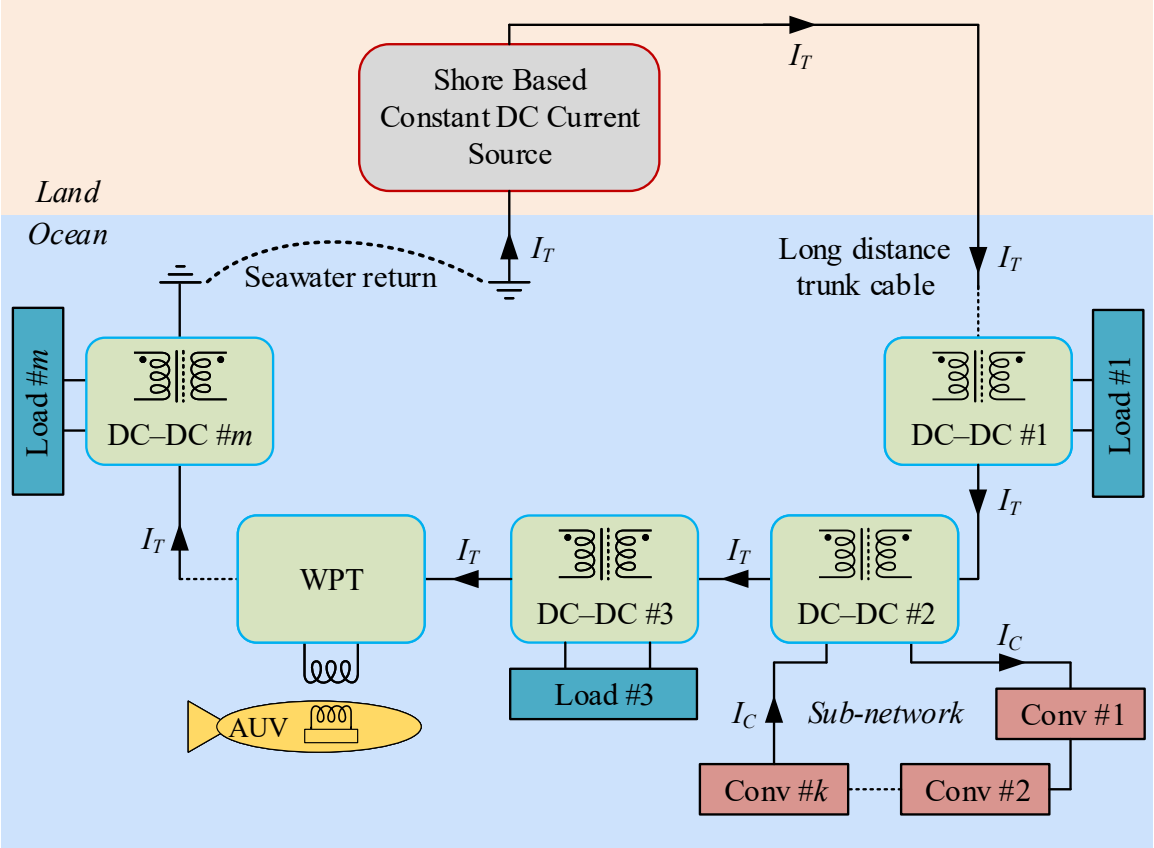


Fig. 1.5: Underwater long distance DC current distribution architecture.

A simplified block diagram of the underwater constant current distribution network is shown in Fig. 1.5 where the shore based source drives constant current (I_T) through the trunk cable which runs on the ocean floor to drive multiple converters connected in series. These converters are hermetically sealed within its enclosure(s) and the components of the converter do not come in contact with the sea water. Using the benefits of conductivity of saline water, the current in the trunk cable returns back to the source through the sea water. Some of these converters drive their local load with a constant voltage output, some of them drive another *sub-network* with constant current (I_C) drive for regional distributed loads, and in some cases converters drive WPT coils for wireless charging of AUVs.

For underwater power converter fed from current source an obvious choice for the topology is current fed converters which is presented in [26, 27] for sub sea oil and gas exploration application where it is operated at high current and low switching frequency for

limiting switching loss. In [2], current fed topology is used in constant current to constant voltage application, but shown only for low voltages. However, due to lack of ZVS for the switches, current fed topologies will be limited in switching frequency. Moreover, there is a need of input filter to smoothen the fluctuating input voltage which if not filtered adequately, can create instability through interaction with the inductance(s) and capacitance(s) of the submarine cable. These can potentially increase the converter size and reduce efficiency of power conversion.

Voltage fed PWM push-pull topologies are presented in [1, 28, 29] where the source is constant current source, suitable of underwater power distribution. Voltage fed topologies can achieve ZVS and can thus be operated at higher switching frequency that can reduce the size of the converter. However, typical PWM based topologies operate with hard switching of main active switches causing high dv/dt and rectifier diodes chop off current with high di/dt. These high dv/dt and di/dt, along with diode reverse recovery cause high frequency ringing due to the circuit parasitic components which increases EMI and loss in the system. Converters used in long distance underwater distributions are preferred to be operated with low EMI for long term, reliable operation due to challenges and cost of maintenance. Resonant converters, operating with sinusoidal voltage and/or current with soft switching reduce the dv/dt and di/dt in the circuit that reduce EMI emission and improves efficiency even at high switching frequencies. In addition, various circuit parasitic components such as leakage inductance of transformer, can be part of the resonant tank network which makes them very attractive in transformer isolated converters. Due to these advantages, resonant power conversion topologies are widely used in LED driver [30–32], energy storage [33, 34], telecommunication [35], DC microgrids [36,37], wireless power transfer [38,39] and numerous other applications. The resonant converters available in literature is operated and designed with voltage source input whereas, converters used in underwater system is supplied with DC current source which brings in new challenges. This forms the basis of this dissertation to investigate these limitations and come up with design of resonant converters to overcome such challenges in power conversion from DC current source which is a new and emerging

research field of interest and have not been explored with great details.

1.2 Resonant Converters in Constant Current Distribution

Due to the nature of the source, resonant converters in underwater distribution face certain challenges in design space which are highlighted in chapter 2. The basic structure of resonant converter with choice and modeling of different sections of the converter is discussed in chapter 2. Differences in power transfer capability with voltage and current sources are analyzed in this chapter as well. The modeling techniques presented in this chapter is used for designing different resonant converters in underwater distribution system.

1.2.1 Soft Switching Requirements

Generally resonant converters are controlled through switching frequency variation, above its resonant frequency, which gives advantage of ZVS through reactive power circulation in the tank. However, when multiple converters tap power from a common input bus (voltage or current), operating the individual converters at different switching frequencies can result in very low frequency AC signals injected into the bus that is very hard to filter out. So, the converters in the distribution network are operated at a fixed switching frequency and control of output is done through phase shift modulation. This brings in limitation on achieving ZVS for the active switches through tank current itself and thus ZVS assisting circuits are needed in conjunction with the main devices. The requirements for ZVS turn on of all the MOSFETs in a resonant converter are analyzed in chapter 3. It is shown how different types of ZVS assisting circuits can be used for different application needs with different resonant topologies. The advantage and need of voltage fed topologies over current fed ones are also highlighted in the chapter 3 with difference in losses between ZVS and ZCS, operating at high frequency and high voltage in underwater distribution system.

1.2.2 Series Resonant Converter

As presented in Fig. 1.5, some of the converters in the distribution network drive a

sub-network of loads with DC current. This type of converters need to regulate its output current from an input current source. In chapter 4, it is shown how a series resonant converter (SRC) fits aptly in this application. SRC design with output current regulation is used in LED drive [40], capacitor charging [41,42] and battery charging in constant current mode [43]. However, these applications are driven from voltage sources as opposed to current source in underwater distribution. With detailed analysis and modeling in chapter 4, it is shown how an SRC can be designed for constant current input to constant current output conversion over a wide load range, up to 1 kW.

1.2.3 Parallel Resonant Converter

For majority of the loads in the underwater distribution network need a voltage source at its input. Converters supplying power to these loads need to provide regulated voltage at its output from current source input. Parallel resonant converter (PRC) is a well suited topology for conversion of DC current source to DC voltage source that is presented in chapter 5. PRC is designed for constant current drive in [44–46], storage battery charger from solar power in [47], all with a voltage source at the input. Hence, analysis and design methodology in needed for use of PRC with constant current source at the input, which is presented in chapter 5, with steady state modeling, ZVS requirements, output filter design, etc. Designing a converter for regulated output voltage over wide range imposes a significant challenge in minimizing component stress and optimizing efficiency. A converter architecture involving a PRC with a multi-winding transformer and an output switch network that together minimize component stress and improve efficiency over the wide range of required operating conditions is also presented in chapter 5.

1.2.4 LCL-T Resonant Converter

Similar to PRC, LCL-T resonant converter can also be used for conversion of DC current source to DC voltage source. While PRC is simple and cost effective solution with low component count, LCL-T provides opportunity for optimizing the converter size and component ratings. Converters employing an LCL-T resonant tank are presented in [48–59]

to achieve a current source behavior from a DC voltage source input and authors in [60] have presented a DAB LCL-T resonant DC-DC converter with voltage sources, both input and output. However, since the source of power in underwater DC distribution system is from a constant current source these designs cannot be used as it is. In [61], an LCL-T resonant tank based non-isolated, DC-DC converter is presented for DC current source to DC voltage source application, but, without a design method. The design optimization for the transformer in isolated LCL-T resonant converters is also absent in the existing literature. Hence, a detailed design methodology for an isolated LCL-T resonant converter that converts a DC current source input to a DC voltage source output is presented in chapter 6. Comparison between passive and active rectification in LCL-T resonant converters for designing the converter with minimum VA rating is presented with detailed analysis, simulation and experimental results.

1.2.5 Bidirectional DAB LCL-T Resonant Converter

Under regular circumstances, the series connected isolated DC-DC converters deliver power from the constant current feed to their respective loads, regulating its output voltage. However, some of the loads on the sea-bed are critical in operation needing uninterrupted power delivery. In the event of any cable fault, these critical loads lose power and for these critical loads, a bidirectional converter with local auxiliary source(s) are provided. These bidirectional converters provide constant voltage to the load from the constant current feed under regular operation and convert an auxiliary voltage source to a constant current drive in the event of loss of power from main feed. Dual active bridge (DAB) based LCL-T resonant converter can be designed to meet the requirements of such critical loads which is presented in chapter 7. Detailed analysis, design with modulation is presented here for designing the converter, minimizing the overall VA rating for resonant tank, transformer and the H-bridges that is not available in the literature. Similar to PRC based converter for wide output voltage range, DAB LCL-T resonant converters can also be designed for bidirectional power conversion in systems interfacing current source at one end with wide voltage range at the other end. The converter architecture of such system is also presented

in chapter 7 with simulation results showing its performance.

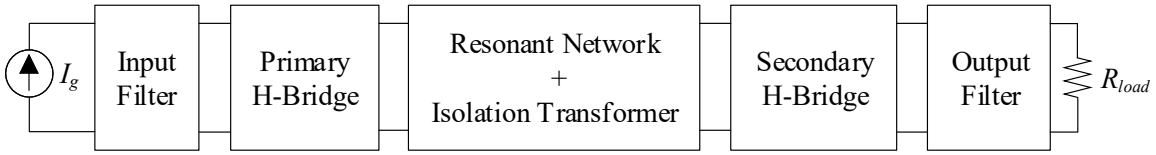


Fig. 2.1: Resonant DC-DC converter architecture with constant current input.

CHAPTER 2

INTRODUCTION TO RESONANT CONVERTER IN UNDERWATER SYSTEM

The resonant converter architecture and its modeling technique are introduced in this chapter. Choice of inverter stage for constant current input, underwater DC distribution system with its modulation technique is presented in section 2.1.1. The properties of resonant tank and basis for sinusoidal approximation is briefed in section 2.1.2 along with various resonant tank realization. Various secondary rectifier and filter stages for different types of resonant tank are presented in section 2.1.3. Detailed steady state modeling techniques for resonant converter is developed in section 2.1.4 along with its equivalent circuit. Section 2.2 presents salient characteristics and limitations for converters operating with constant current source, as opposed to conventional constant voltage source, to establish the basic criteria for design of resonant converters in underwater DC distribution system.

2.1 Resonant Converter

The basic architecture of resonant converter used in underwater distribution network is discussed in this section along with modeling of different parts of the converter. The converter architecture of an underwater resonant DC-DC converter is shown in Fig. 2.1 where the input power is drawn from a DC current source (I_g) and delivered to the load (R_{load}) regulating its output current or voltage. The converter has three distinct sections – primary H-bridge with input filter, resonant tank with isolation transformer and secondary H-bridge with output filter which are explained as follow.

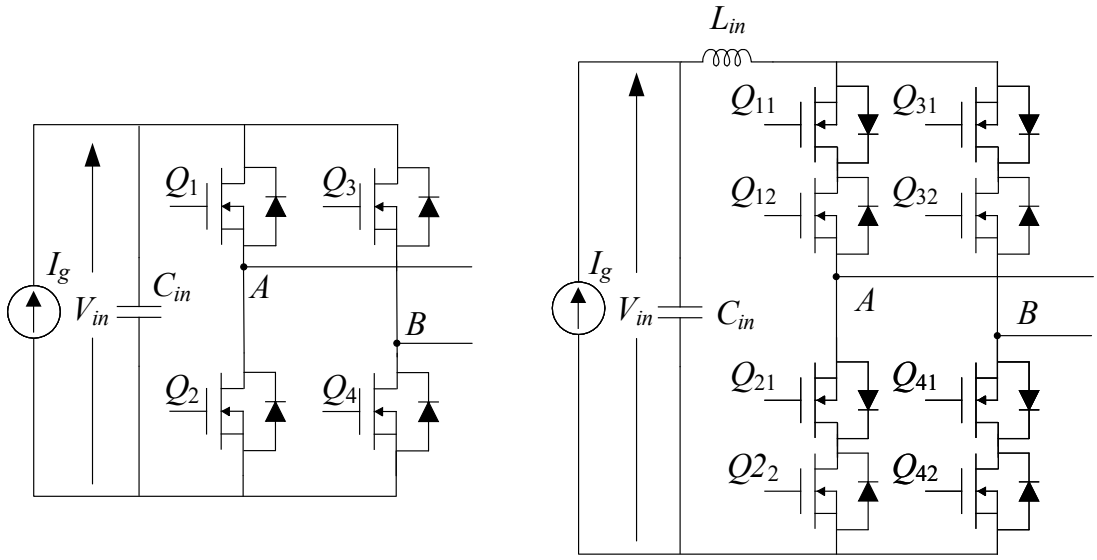


Fig. 2.2: Input filter and primary inverter stage for (a) voltage fed inverter (VFI) (b) current fed inverter (CFI)

2.1.1 Primary Inverter Stage

The first stage of power conversion is the input filter with a H-bridge to convert DC input to a quasi-square wave AC. For this stage of power processing, there are two options – voltage fed inverter (VFI) or current fed inverter (CFI) as shown in Fig. 2.2(a) and Fig. 2.2(b), respectively. The comparison of these two type of inverters are presented in Table 2.1.

From the comparison in Table 2.1, since the underwater observatory system is designed to operate with low current and high voltage, VFI based primary stage is the more practical choice for high switching frequency converter design. For example, for an ideal 1 kW converter in a system with 1 A input current, the DC input voltage will be 1 kV and thus the devices needed in VFI and CFI will be rated for 1.7 kV and 3.3 kV, respectively, based on commercially available MOSFETs. Moreover, with ZCS in CFI, the devices will still have its output capacitance energy dissipated within them which will lead to less efficient power processing. Thus designing the converter with VFI based primary stage will be efficient, power dense and cost effective, compared to CFI based primary stage. Use of CFI becomes

Table 2.1: Comparison between VFI and CFI

Voltage Fed Inverter (VFI)	Current Fed Inverter (CFI)
• 4 active switches required • Quasi-square wave voltage and sinusoidal current • Devices' voltage rating: V_{in} • Lower isolation voltage for gate drivers • Steady DC voltage at the DC side of the H-bridge • Capacitive input filter • Achieving ZVS is simple	• 8 active switches required • Quasi-square wave current and sinusoidal voltage • Devices' voltage rating: $> 1.6V_{in}$ • Higher isolation voltage for gate drivers • Oscillating voltage at the DC side of the H-bridge • $C - L$ input filter stage required • ZCS operation, achieving ZVS is a challenge

advantageous for systems with higher current, lower voltage, operating with low switching frequency up to a few tens of kHz [26, 27] and hence is not pursued in this work.

In general, for fixed frequency resonant converters, the primary stage inverter is driven by symmetric modulation scheme, *i.e.* each of the inverter leg switches are driven by 50 % duty ratio and the phase shift between inverter legs are controlled, as shown in Fig. 2.3. This type of symmetric modulation only produces odd harmonics in the inverter output voltage spectrum and is the preferred choice. Asymmetric modulation scheme can produce even order harmonics and is typically avoided, unless it provides some other significant advantage in converter operation [48, 62–65].

2.1.2 Resonant Tank and Transformer

The second stage in the power converter in Fig. 2.1 is the resonant tank and the isolation transformer. The quasi-square wave output from the primary bridge gets filtered by the resonant tank to pass only the fundamental frequency component and block other harmonics, as shown in Fig. 2.4. Hence, for the analysis of resonant converters, only fun-

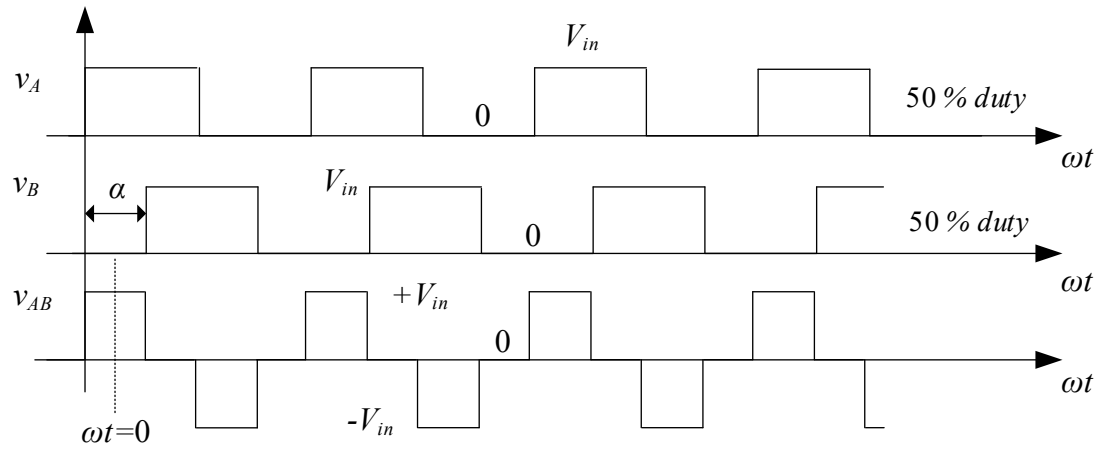


Fig. 2.3: Modulation waveform of the primary side inverter.

damental components of signals are considered and this technique is referred as sinusoidal approximation [66] or fundamental harmonic approximation (FHA) [67]. Different types of resonant tank configuration are shown in Fig. 2.5, *viz.* series resonant [67], parallel resonant [67], series-parallel LCC resonant [67], LLC resonant [68], $LCL-T$ resonant [49] and its dual $CLC-T$ resonant [49]. There are many more combinations of resonant tanks possible based on number of resonant elements. The choice of resonant tank in any application is dependent on the application and its need. The isolation transformer provides galvanic isolation between input and output which is needed in converters used in underwater distribution system where the DC-DC converters are series stacked at the input stage and output is grounded at seawater. In addition, the transformer provides step up or step down through its primary to secondary winding turns ratio that helps in optimizing the overall converter design. The various resonant tanks shown in Fig. 2.5 may also combine the parasitic elements *e.g.* leakage inductance of the isolation transformer which is a significant advantage of resonant topologies.

2.1.3 Secondary Rectifier Stage

Based on the resonant tank chosen for a particular application, the secondary side H-bridge may be driven by an AC voltage or AC current at its input as shown in Fig. 2.6. For resonant tank which has a series connected elements before the rectifier (*e.g.* series

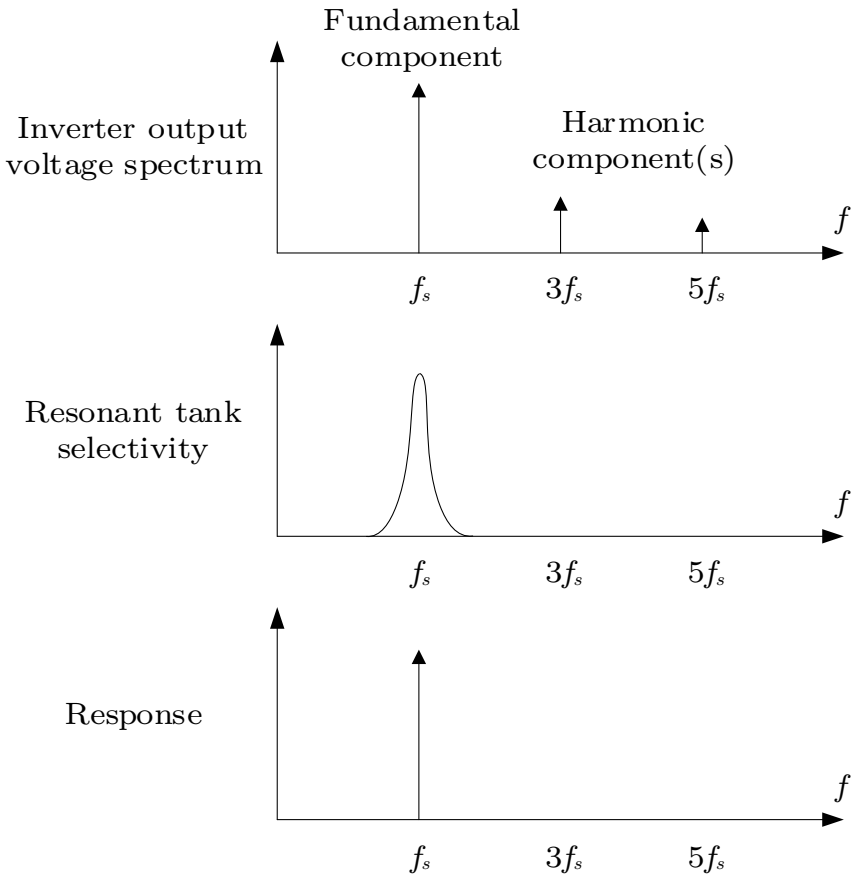


Fig. 2.4: Response of the resonant tank.

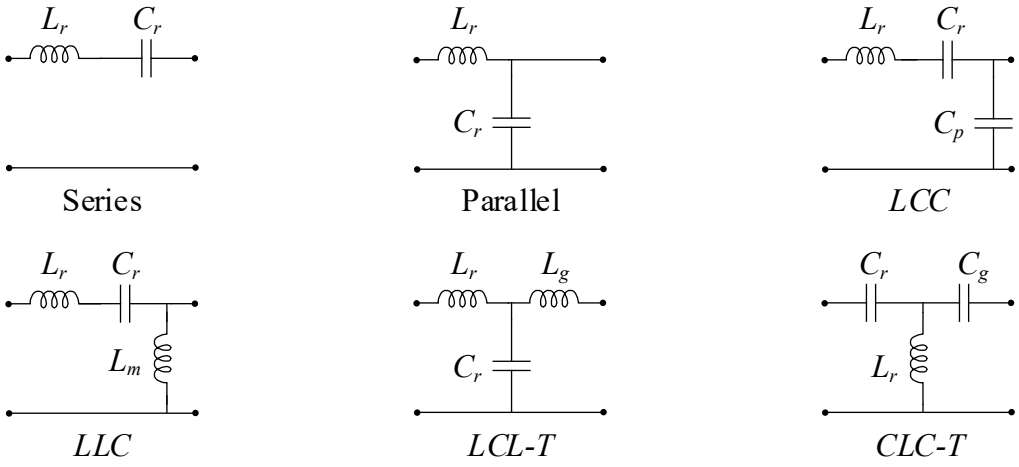
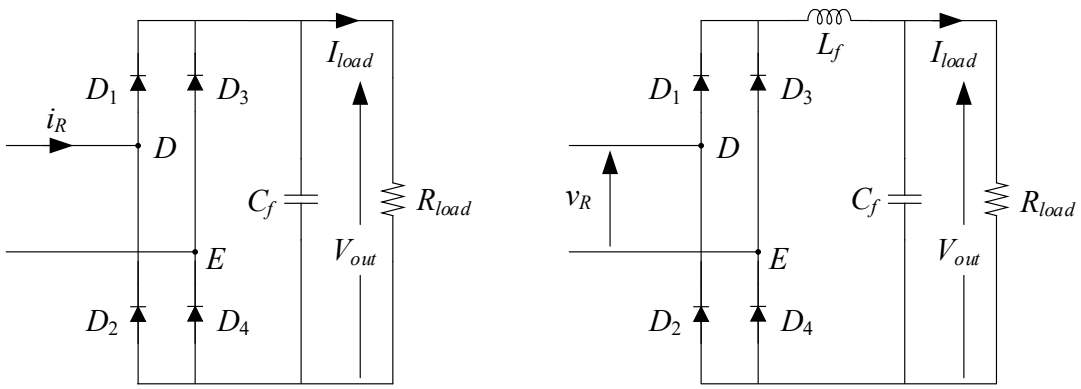


Fig. 2.5: Different types of resonant tanks.



(a) (b)

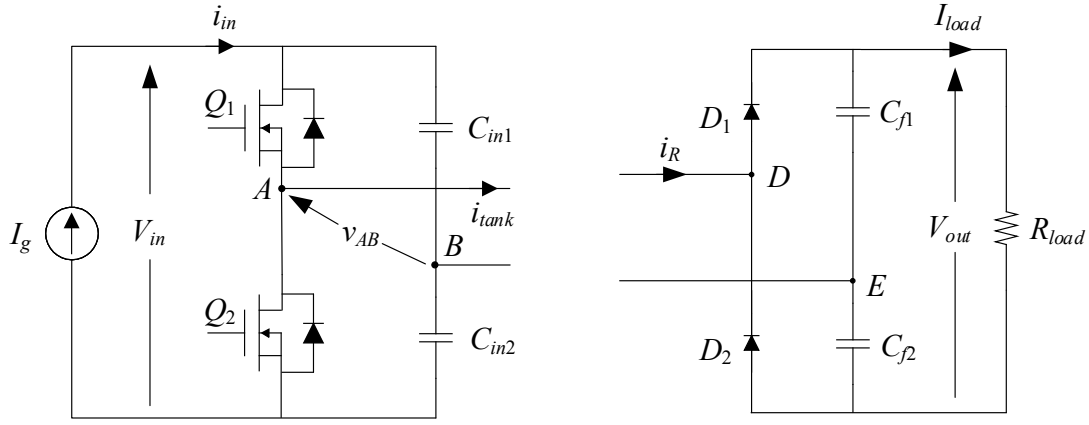
Fig. 2.6: Different rectifier configuration (a) AC current fed rectifier with capacitive filter and (b) AC voltage fed rectifier with $L-C$ filter.

resonant tank) is typically an AC current driven rectifier, as shown in Fig. 2.6(a) and needs a capacitive output filter. Whereas, for resonant tank with a capacitor connected across the rectifier (*e.g.* parallel resonant tank) would need an $L-C$ filter after the diode rectifier stage, as shown in Fig. 2.6(b). The secondary H-bridge used in converters with unidirectional power flow is typically built using diode bridge rectifier which in many occasion is substituted by MOSFETs for synchronous rectification for lower conduction loss and better efficiency.

The inverter shown in Fig. 2.2(a) and the rectifier in Fig. 2.6(a) are full-bridge inverter and rectifier, respectively. However, the inverter and/or rectifier could be built as half bridge circuit as well that can provide additional attenuation or gain by factor of two. A half-bridge inverter and rectifier circuit configuration(s) are shown in Fig. 2.7(a) and Fig. 2.7(b), respectively.

2.1.4 Modeling of Inverter and Rectifier

For the steady state analysis of resonant converter, an equivalent model for the primary inverter and secondary rectifier are developed here with fundamental components (FHA). The primary inverter, its operating waveform and equivalent circuit are shown in Fig. 2.8. For the inverter waveforms in Fig. 2.8, the fundamental inverter output voltage can be



(a) (b)

Fig. 2.7: Half bridge (a) inverter and (b) rectifier circuit.

derived from Fourier series expansion of v_{AB} and is given as

$$v_{AB,1}(t) = \frac{4}{\pi} V_{in} \sin\left(\frac{\alpha}{2}\right) \sin(\omega_s t), \tag{2.1}$$

where ω_s is the angular switching frequency and α is the modulation angle. The tank current is expressed as

$$i_{tank}(t) = I_{tank} \sin(\omega_s t - \phi_{in}), \tag{2.2}$$

where ϕ_{in} is the phase difference between $v_{AB,1}$ and i_{tank}.

The DC side current of the inverter (i_{in}) is determined by the tank current and switching state of the inverter and can be expressed as

$$i_{in}(t) = \frac{v_{AB}(t)}{V_{in}} i_{tank}(t). \tag{2.3}$$

The AC ripple in i_{in} is filtered out by input capacitor and average value is supplied by the DC current source (I_g) which is given as

$$I_g = \langle i_{in} \rangle = \frac{1}{T_s} \int_0^{T_s} i_{in}(t)\, dt, \tag{2.4}$$

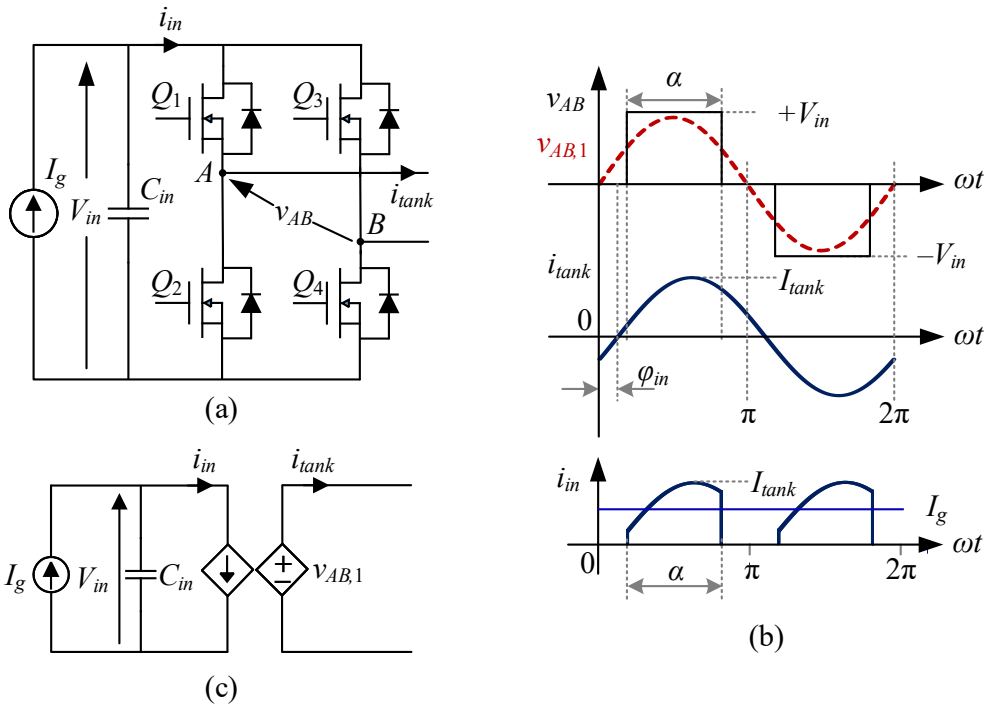


Fig. 2.8: (a) Primary side inverter with (b) its operating waveforms and (c) equivalent circuit.

where T_s is switching time period. From the waveform of i_{in} in Fig. 2.8, the relationship between DC and AC side current can be established from (2.5) as

$$I_g = \frac{1}{\frac{\pi}{\omega_s}} \int_{\frac{\pi}{2}-\frac{\alpha}{2}}^{\frac{\pi}{2}+\frac{\alpha}{2}} i_{tank}(t)\, dt = \frac{2}{\pi} I_{tank} \sin\left(\frac{\alpha}{2}\right) \cos(\phi_{in}). \tag{2.5}$$

Based on these derivations in (2.1 – 2.5), the AC side of the inverter can be modeled as a dependent voltage source and the DC side can be modeled as dependent current source as shown by the equivalent circuit in the bottom left in Fig. 2.8 with the balance between DC and AC power through lossless power conversion as

$$P_{DC} = V_{in} I_g = V_{AB,1,rms} I_{tank,rms} \cos(\phi_{in}) = P_{AC}, \tag{2.6}$$

where P_{DC} is the DC power input, P_{AC} is the active power output of the inverter, $V_{AB,1,rms}$ and $I_{tank,rms}$ are the rms value of inverter fundamental voltage and current, respectively.

For the output rectifier section, the time domain waveforms for AC current fed rectifier and AC voltage fed rectifier, corresponding to the circuit shown in Fig. 2.6(a) and Fig. 2.6(b), are shown in Fig. 2.9(a) and Fig. 2.9(b), respectively. As shown in Fig. 2.6(a), for the current fed rectifier, the rectifier input voltage is a square wave of amplitude V_{out} whose fundamental component and rectifier input current can be expressed as

$$v_{RI,1}(t) = \frac{4}{\pi} V_{out} \sin(\omega_s t - \phi_{RI}), \tag{2.7}$$

$$i_{RI}(t) = I_{RI} \sin(\omega_s t - \phi_{RI}), \tag{2.8}$$

where ϕ_{RI} is the phase shift of i_{RI} with respect to fundamental inverter output voltage ($v_{AB,1}$). It should be noted here that fundamental rectifier input voltage and current are always in phase. On the output of rectifier, the voltage is DC of magnitude V_{out} and the current (i_{RO}) is rectified sine wave of twice the switching frequency which are shown in Fig. 2.9(a). The rectified current can be expressed as

$$i_{RO}(t) = |i_{RI}(t)|. \tag{2.9}$$

The AC ripple in i_{RO} is filtered by output capacitor and its DC value goes to the load and thus the relationship between AC and DC current of the rectifier can be established as

$$I_{load} = \langle i_{RO} \rangle = \frac{2}{T_s} \int_0^{\frac{T_s}{2}} i_{RI}(t)\, dt = \frac{2}{\pi} I_{RI}. \tag{2.10}$$

Since the rectifier process only active power with its input AC voltage and current in phase, the rectifier can be modeled as an AC equivalent resistance given as

$$R_{eI} = \frac{v_{RI,1}(t)}{i_{RI}(t)}, \tag{2.11}$$

which, using (2.7), (2.8) and (2.10) can be expressed as

$$R_{eI} = \frac{8}{\pi^2}\frac{V_{out}}{I_{load}} = \frac{8}{\pi^2}R_{load}. \tag{2.12}$$

Based on these derivations, the equivalent circuit model derived for the AC current fed rectifier is shown in Fig. 2.10(a).

Following a similar process, the signals for AC voltage fed rectifier circuit from Fig. 2.6(b) can be derived as

$$v_{RV}(t) = V_{RV}\sin(\omega_s t - \phi_{RV}), \tag{2.13}$$

$$i_{RV,1}(t) = \frac{4}{\pi}I_{load}\sin(\omega_s t - \phi_{RV}), \tag{2.14}$$

where ϕ_{RV} is the phase shift of v_{RV} with respect to fundamental inverter output voltage ($v_{AB,1}$). It should be noted here that the DC value of i_{Lf} (I_{Lf}) is equal to the load current (I_{load}). On the output of rectifier, the voltage (v_{RO}) is rectified sine wave of twice the switching frequency which is shown in Fig. 2.9(b) and can be expressed as

$$v_{RO}(t) = |v_{RV}(t)|. \tag{2.15}$$

The AC ripple in v_{RO} is filtered by output $L_f - C_f$ filter and its DC value appears across the load and thus the relationship between AC and DC voltage of the rectifier can be established as

$$V_{out} = \langle v_{RO} \rangle = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} v_{RV}(t)\,dt = \frac{2}{\pi}V_{RV}. \tag{2.16}$$

Again, the voltage fed rectifier can also be modeled as an AC equivalent resistance given as

$$R_{eV} = \frac{v_{RV}(t)}{i_{RV,1}(t)}, \tag{2.17}$$

which, using (2.13), (2.14) and (2.16) can be expressed as

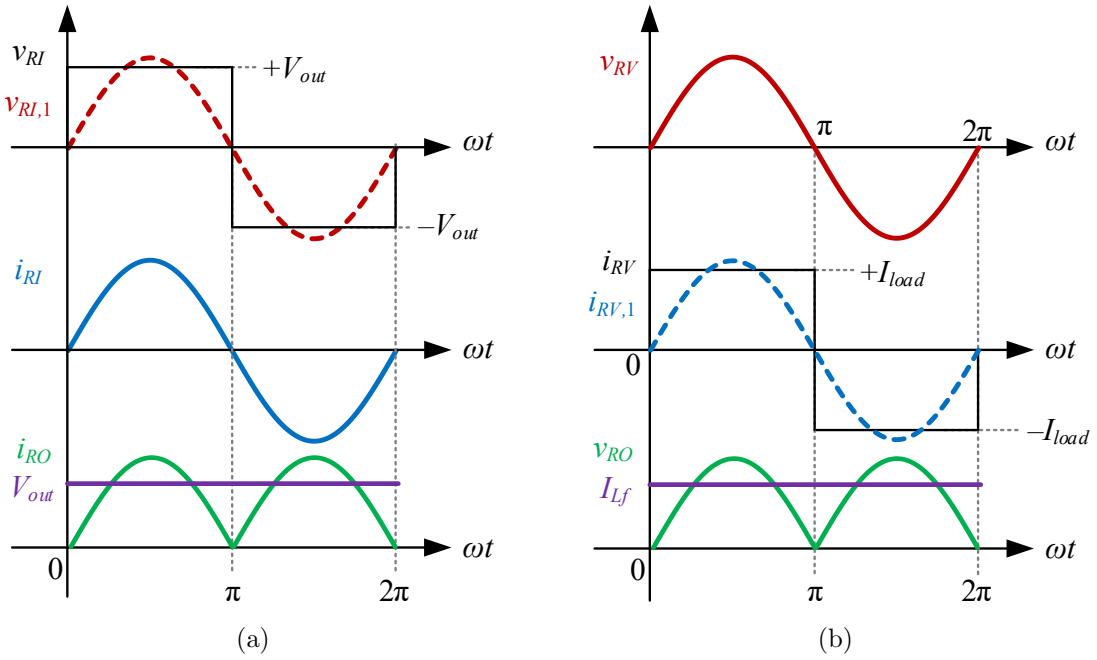


Fig. 2.9: Waveform of the (a) AC current fed rectifier and (b) AC voltage fed rectifier.

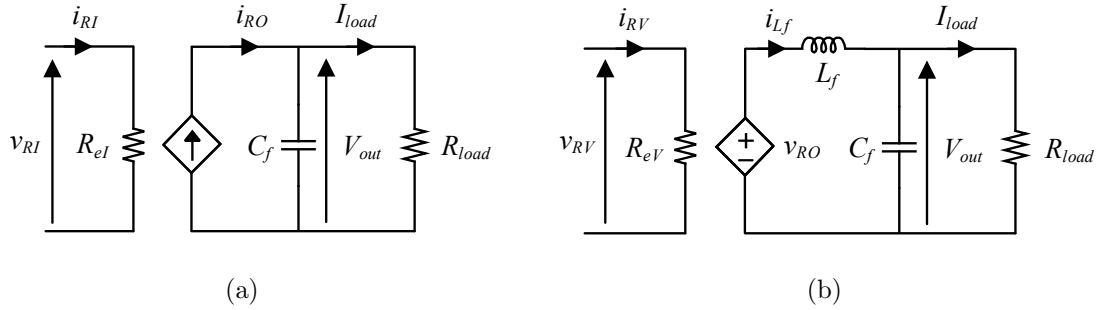


Fig. 2.10: Equivalent circuit of output rectifier and filter for (a) AC current fed rectifier and (b) AC voltage fed rectifier.

$$R_{eV} = \frac{\pi^2}{8}\frac{V_{out}}{I_{load}} = \frac{\pi^2}{8}R_{load}. \tag{2.18}$$

Based on these derivations, the equivalent circuit model derived for the AC voltage fed rectifier is shown in Fig. 2.10(b).

2.1.5 Steady State Model for the Resonant Converter

The models derived for the inverter and rectifier now can be used to model the entire

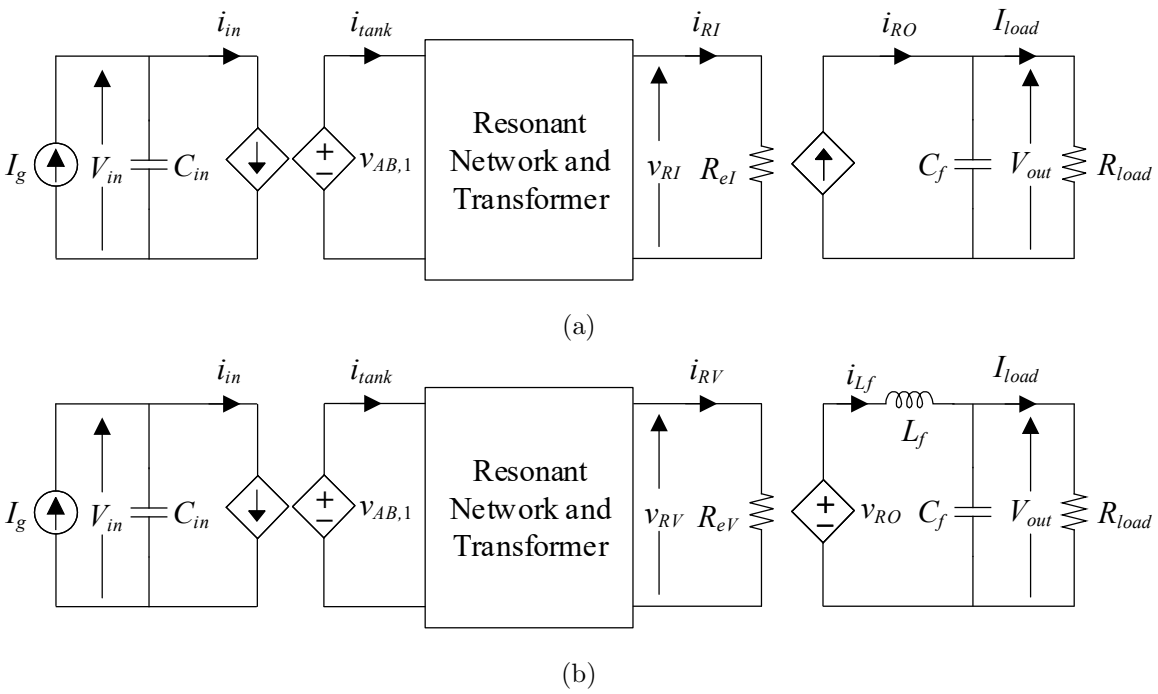
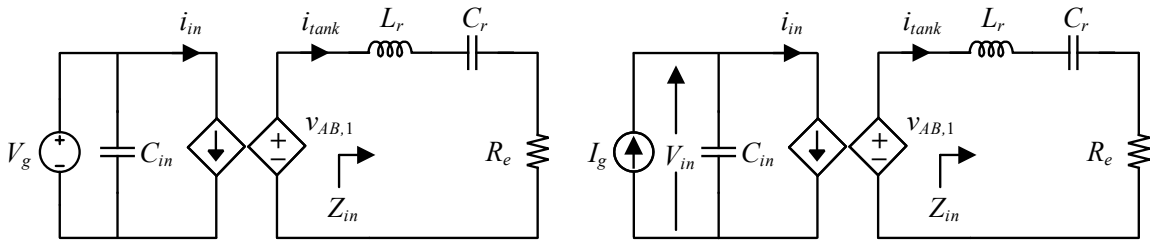


Fig. 2.11: Steady state equivalent circuit of the resonant converter from Fig. 2.1 for (a) AC current fed rectifier and (b) AC voltage fed rectifier.

resonant converter architecture shown in Fig. 2.1 and are shown in Fig. 2.11(a), for AC current fed rectifier and in Fig. 2.11(a), for AC voltage fed rectifier. Since the resonant tank and transformer in the converter are linear, passive components, they are modeled in the equivalent circuit as they are. This steady state model of the converter shown in Fig. 2.11 along with the derivations presented in this section will be used in the remaining chapters for deriving the steady state input output relationship of the converter(s).

2.2 Power Transfer through Resonant Converter

In this section the governing equation for power transfer in a resonant converter is established with comparison between resonant converters with DC voltage source and DC current source input. It is also shown how the choice of resonant tank elements and its operating point affect the power transfer limit through the converter. As an example, a series resonant converter that is simplest of all resonant tank, is considered for analysis and this analysis can be extended to any other resonant tank with suitable equivalent circuit.



(a) (b)

Fig. 2.12: Equivalent circuit of a series resonant converter (a) with DC voltage source input and (b) with DC current source input.

First, the converter is analyzed with DC voltage source and its equivalent circuit is shown in Fig. 2.12(a) and then for converter with DC current source whose equivalent circuit is shown in Fig. 2.12(b). For the analysis, it is assumed that the converters are lossless, driven by symmetrical phase shift modulation presented in Fig. 2.3 and the output side(s) are full-bridge rectifier. The following analysis is conducted with FHA. The AC equivalent resistance, referred to transformer primary side, shown in Fig. 2.12 is given from (2.12) as

$$R_e = \frac{8n^2}{\pi^2} R_{load}, \tag{2.19}$$

where n is the primary to secondary turns ratio of the isolation transformer. The impedance of the loaded resonant tank is expressed as

$$Z_{in} = R_e + j\omega_s L_r - j\frac{1}{\omega_s Cr}. \tag{2.20}$$

With the following definition of angular resonant frequency (ω_o), characteristic impedance (Z_o) and normalized switching frequency (F)

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}, \quad Z_o = \sqrt{\frac{L_r}{C_r}}, \quad F = \frac{\omega_s}{\omega_o} = \frac{f_s}{f_o}, \tag{2.21}$$

Z_{in} from (2.20) can be expressed as

$$Z_{in} = R_e + jZ_o\left(F - \frac{1}{F}\right). \tag{2.22}$$

With FHA, the power factor of the primary inverter is given as

$$\cos\left(\phi_{in}\right) = \frac{R_e}{\sqrt{R_e^2 + Z_o^2\left(F - \frac{1}{F}\right)^2}}. \tag{2.23}$$

The active power transferred from the inverter to the load (R_e) is given as

$$P_V = \frac{V_{AB,1,rms}^2}{|Z_{in}|}\cos\left(\phi_{in}\right). \tag{2.24}$$

Using (2.22) and (2.23), (2.24) can be expressed as

$$P_V = \frac{8}{\pi^2}V_g^2\sin^2\left(\frac{\alpha}{2}\right)\frac{R_e}{R_e^2 + Z_o^2\left(F - \frac{1}{F}\right)^2}. \tag{2.25}$$

Now, for the converter with constant current input, as shown in Fig. 2.12(b), the power transferred can not be directly determined from (2.25) since the DC input voltage is not an independent variable. From the relationship established in (2.5), the tank current amplitude can be given as

$$I_{tank} = \frac{\pi}{2}\frac{I_g}{\sin\left(\frac{\alpha}{2}\right)\cos\left(\phi_{in}\right)}. \tag{2.26}$$

Using (2.26), the power transferred to the load can be expressed as

$$P_I = \frac{I_{tank}^2 R_e}{2} = \frac{\pi^2}{8}\frac{I_g^2 R_e}{\sin^2\left(\frac{\alpha}{2}\right)\cos^2\left(\phi_{in}\right)}. \tag{2.27}$$

Substituting $\cos\left(\phi_{in}\right)$ from (2.23), (2.27) can be expressed as

$$P_I = \frac{\pi^2}{8}\frac{I_g^2}{\sin^2\left(\frac{\alpha}{2}\right)}\frac{R_e^2 + Z_o^2\left(F - \frac{1}{F}\right)^2}{R_e}. \tag{2.28}$$

From the power delivery expression(s) in (2.25) and (2.28), it can be seen that for a given resonant converter setup and load resistance, the power output increases with increase

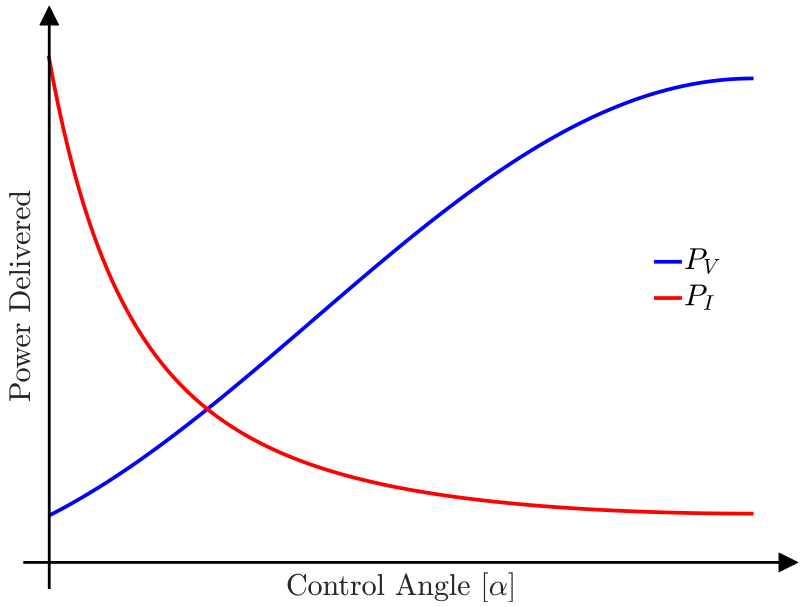


Fig. 2.13: Variation of power delivery with respect to control angle (α). Blue plot is with constant voltage source and red is for converter with constant current source.

in control angle (α) when the input is DC voltage source. Whereas, for DC current source input power output increases with decrease in control angle, *i.e.*

$$P_V \propto \sin^2\left(\frac{\alpha}{2}\right), \qquad P_I \propto \frac{1}{\sin^2\left(\frac{\alpha}{2}\right)}. \tag{2.29}$$

This is an important distinction between converters fed from constant current source and constant voltage source. This can also be understood as: with constant voltage input, increasing α increases the driving voltage from the inverter (v_{AB}) as presented in (2.1), which in turn delivers more power; whereas, with constant current input, decreasing α increases the driving current in the tank (i_{tank}) as derived in (2.26), delivering more power. With α ranging within [0°, 180°], from (2.25), (2.28) and (2.29) it can be seen that for voltage source input, maximum power transfer happens at $\alpha = 180°$, whereas, at the same operating point with $\alpha = 180°$, power transfer is at its minimum point for converters operating with current source input. The variation of power delivery with respect to the control angle (α) is shown in Fig. 2.13 for constant voltage source input (in blue) and for constant current source (in red) input.

Now, the power transfer limits for each of the converters shown in Fig. 2.12(a) can be determined as follow. For the converter with voltage source input, the maximum power transfer limit can be obtained from maximum power transfer theorem which can also be determined through derivative tests. Equating the first derivative of P_V from (2.25) with respect to R_e to zero, R_{emV} can be determined as

$$\frac{dP_V}{dR_e} = 0 \quad \Rightarrow \quad R_{emV} = \left| Z_o \left(F - \frac{1}{F} \right) \right|. \tag{2.30}$$

The second derivative of P_V with respect to R_e, evaluated at $R_e = R_{emV}$ is

$$\left. \frac{d^2 P_V}{dR_e^2} \right|_{R_e = R_{emV}} = -\frac{4}{\pi^2} \frac{V_g^2 \sin^2\left(\frac{\alpha}{2}\right)}{R_{emV}^3} \; < \; 0, \tag{2.31}$$

which means maximum power transfer occurs at $R_e = R_{emV} = \left| Z_o \left(F - \frac{1}{F} \right) \right|$ and the value, evaluated with $\alpha = 180°$, is given as

$$P_{V\_max} = \frac{4}{\pi^2} \frac{V_g^2}{\left| Z_o \left(F - \frac{1}{F} \right) \right|}. \tag{2.32}$$

For the converter with current source input, equating the first derivative of P_I from (2.28) with respect to R_e to zero, R_{emI} can be determined as

$$\frac{dP_I}{dR_e} = 0 \quad \Rightarrow \quad R_{emI} = \left| Z_o \left(F - \frac{1}{F} \right) \right|. \tag{2.33}$$

The second derivative of P_I with respect to R_e, evaluated at $R_e = R_{emI}$ is

$$\left. \frac{d^2 P_I}{dR_e^2} \right|_{R_e = R_{emI}} = \frac{\pi^2}{4} \frac{I_g^2}{R_{emV} \sin^2\left(\frac{\alpha}{2}\right)} \; > \; 0, \tag{2.34}$$

which means minimum power transfer occurs at $R_e = R_{emI} = \left| Z_o \left(F - \frac{1}{F} \right) \right|$ and the value, evaluated with $\alpha = 180°$, is given as

$$P_{I\_min} = \frac{\pi^2}{4} I_g^2 \left| Z_o \left(F - \frac{1}{F} \right) \right|. \tag{2.35}$$

From these derivations it can be seen that similar to maximum power transfer theorem for voltage source case, a minimum power transfer limit exists for current source input case and the condition at which these power limit(s) occur is same for either case as given in (2.30) and (2.33) *i.e.* when the equivalent load resistance is equal to the magnitude of the tank impedance. It can be further noticed from these power limit expressions in (2.32) and (2.35) that there will not be any theoretical limitation at $F = 1$ *i.e.* if the converter operates with switching frequency equal to its resonant frequency and thus the converter can operate without any restriction on power limit. This important property is utilized while designing resonant converters in underwater systems with constant DC current input, as presented in the remaining part of the thesis.

The minimum power limit from (2.35), the input impedance of the loaded resonant tank from (2.22) and the inverter power factor from (2.23) can be expressed at $F = 1$ operating condition as

$$P_{I\_min}|_{F=1} = 0, \tag{2.36}$$

$$Z_{in}|_{F=1} = R_e, \tag{2.37}$$

$$\cos(\phi_{in})|_{F=1} = 1, \tag{2.38}$$

which means that the primary inverter will be operating at unity power factor with resistive impedance when there is no minimum power limit, for converters with constant current input. Even though the example exercised in this chapter is a series resonant converter, the basic principle of the power limits stays the same, irrespective of the resonant tank topologies and this limit can be derived by deriving suitable Thevenin or Norton equivalent circuit of the loaded resonant tank.

Summary

In this chapter resonant converter architecture used in underwater distribution system is introduced. It is shown how a voltage fed inverter (VFI) is advantageous over current fed inverter (CFI) in such system with low current, high voltage and operating at high switching frequency. Modulation scheme for VFI is presented with its steady state modeling technique. Equivalent circuits are developed for both the primary inverter and secondary rectifier with different types of output filter for different types of resonant tank. With an example resonant converter consisting of series resonant tank it is presented how the converter behaves differently with constant current source input, compared to converter with traditional constant voltage source input. Limitation(s) of power transfer through the resonant converter on the tank design and operating point are also presented. The modeling techniques and equivalent circuits derived in this chapter will be used in the following chapters for design of various resonant converters in underwater DC current distribution system.

CHAPTER 3

ZERO VOLTAGE SWITCHING REQUIREMENTS

Resonant converters have found its popularity in DC-DC converter and DC-AC high frequency inverters due to its advantages such as high power density, high efficiency, low EMI and high reliability due to its soft switching capability. Different basic half-bridge resonant converter topologies are presented in [67] which provides a comparison among these topologies. Half-bridge topologies are suitable and cost-effective for low power converters whereas, full-bridge topologies are essential for high power converters.

Full bridge converters, both load resonant and non-resonant are popular in high power isolated converters due to better utilization of magnetics and other circuit components [69, 70]. Operation of converters at higher frequencies are pushed to reduce the size of reactive components. But, operating at higher frequencies comes with the disadvantage of higher switching loss in the devices resulting in poor efficiency. Hence, soft transition of the switches are essential in order to reduce the size of heat sink and improve efficiency of power conversion. Since MOSFETs are the prime choice for operating at high frequency, zero voltage switching (ZVS) of the devices are needed for efficient and clean power conversion [71]. On the other hand zero current switching (ZCS) is much more suitable for minority carrier devices such as IGBT [71]. Notably, with ZCS, energy stored in the output capacitance of the device will be lost within the device during turn ON and hence ZVS is preferred for MOSFET based power converters [71].

In order to ensure soft switching in a converter, it is important to understand its requirements and dependencies on device's parasitic output capacitance. A typical, voltage fed half bridge setup, converting DC input V_{in} to AC voltage v_{sw} at the switch node, built with MOSFETs Q_T and Q_B is shown in Fig. 3.1 where C_T and C_B represent the output parasitic capacitance (C_{oss}) of top and bottom MOSFETs, respectively. Though it's shown for half bridge, full bridge or $3-\phi$ systems are mere extension of half bridge. Typical

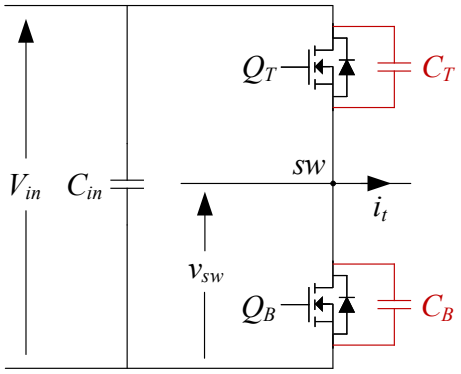


Fig. 3.1: A voltage fed half-bridge circuit with MOSFETs and its output capacitance.

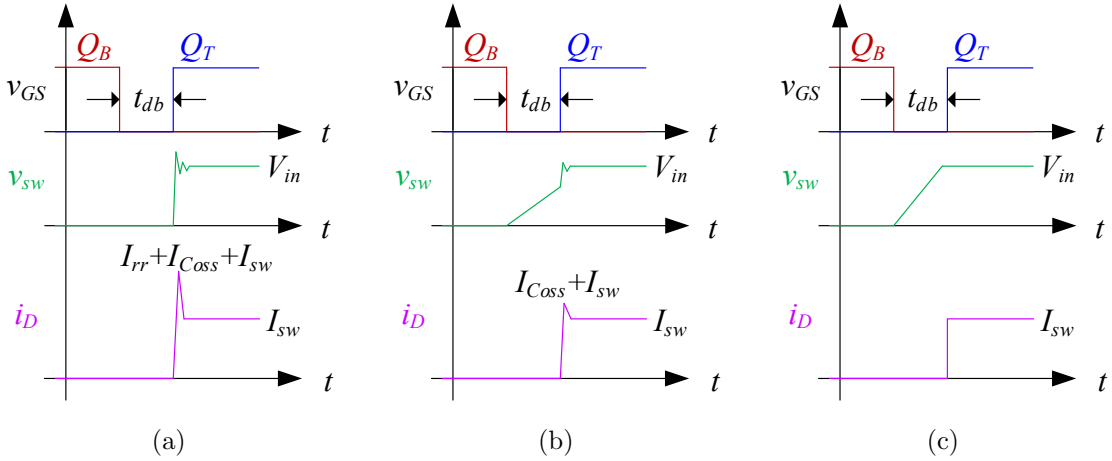


Fig. 3.2: Switching waveform of a half bridge circuit for (a) hard switching (b) partial soft switching (c) total soft (ZVS) turn on.

operating waveform of the half bridge of Fig. 3.1 is shown in its simplified form, with gate signals (v_{GS}), switch node voltage (v_{sw}) and device current for top device (i_D), in Fig. 3.2 for hard switching (Fig. 3.2(a)), partial soft switching (Fig. 3.2(b)) and soft switching with ZVS turn on (Fig. 3.2(c)). In Fig. 3.2, I_{sw} is the current out of the switch node during the transition from bottom switch to top switch, t_{db} is the dead time between the switches, I_{rr} is the reverse recovery current of the body diode of the complementary MOSFET and I_{Coss} is the current due to C_{oss} discharged into the device. In the hard switching case (Fig. 3.2(a)), the total turn on switching energy loss (E_{on_HS}) is distributed in three parts given as

$$E_{on\_HS} = E_{VI} + E_{rr} + E_{Coss}, \tag{3.1}$$

where E_{VI} is the switching energy loss in the device due to voltage and current overlap, E_{rr} is the loss due to reverse recovery effect of complementary device's body diode and E_{Coss} is the loss due to device's output capacitance (C_{oss}). In case of partial soft switching (Fig. 3.2(b)), the loss due to reverse recovery is absent and total turn on switching energy loss (E_{on_PSS}) only consists of partial voltage and current overlap loss (ΔE_{VI}) and partial C_{oss} discharge loss (ΔE_{Coss}), given as

$$E_{on\_PSS} = \Delta E_{VI} + \Delta E_{Coss}. \tag{3.2}$$

In case of ZVS turn on (Fig. 3.2(c)), the output capacitance of the MOSFET is totally discharged and its body diode starts conduction before turning the gate on and thus the turn on switching loss becomes zero, given as

$$E_{on\_SS} = 0. \tag{3.3}$$

For turn off of MOSFET, the output capacitance of the device delays the rise of voltage across it which makes the device current go to zero before voltage rises significantly and thus the turn off loss due to voltage and current overlap remains very low and is not considered in switching loss *e.g.* $E_{off} \approx 0$.

From the waveforms in Fig. 3.2, it can be seen that the voltage waveform in hard switching of MOSFETs introduces EMI due to oscillations [72, 73] and often results in spurious gate turn-ON of devices and possible device failure due to high dv/dt, particularly with wide bandgap devices [74, 75]. Soft-switching with zero voltage switching (ZVS) reduces the switching losses as well as EMI in the converter, as there are no associated ringing.

A typical MOSFET's output capacitance is non-linear and it is dependent on the voltage across it (V_{DS}), as shown in Fig. 3.3 by the magenta dots, for the device C2M1000170D

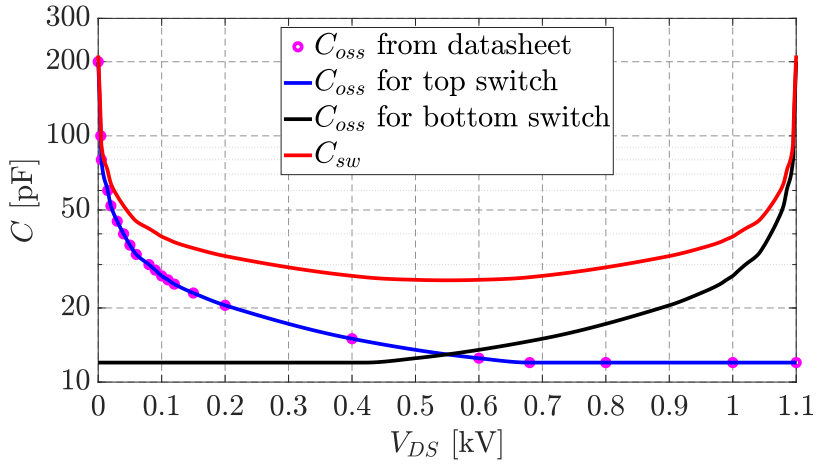


Fig. 3.3: Non-linear output capacitance of MOSFETs with respect to the voltage across top device, in a half bridge configuration.

which is used in the converters in this work. The total capacitance on the switch node (C_{sw}) is sum of the capacitance across top and bottom switches, since the DC link capacitor C_{in} is much higher than C_T and C_B. The variation of C_T, C_B and C_{sw}, with respect to variation on V_{DS} across top switch, are shown in Fig. 3.3 in blue, black and red, respectively.

Analyzing a circuit with voltage dependent non-linear capacitance is a challenge and hence linear equivalent capacitance(s) are derived as per [76]. The charge equivalent capacitance (C_{eq_Q}) and energy equivalent (C_{eq_E}) of the MOSFET with respect to operating voltage is shown in Fig. 3.4, in blue and red, respectively. Using the linear equivalent capacitance(s), the power loss in an H-bridge inverter (as presented in Fig. 2.2(a)), only due to its output capacitance across drain–source of the MOSFETs, is plotted in Fig. 3.5 in blue. Here, for each device, two C2M1000170D MOSFETs are considered connected in parallel and operating with a switching frequency of 250 kHz which are the hardware configuration used in this work. In practical converter built on a printed circuit board (PCB), there will be additional parasitic capacitance across the devices which will further increase the loss in the inverter, as shown by the red curve in Fig. 3.5, for additional 10 pF PCB parasitic capacitance across each of the devices. It can be seen from these plots in Fig. 3.5 that the loss due to the devices' output capacitance can be significant depending on the operating voltage, which makes it challenging for efficient power conversion and thermal design. This

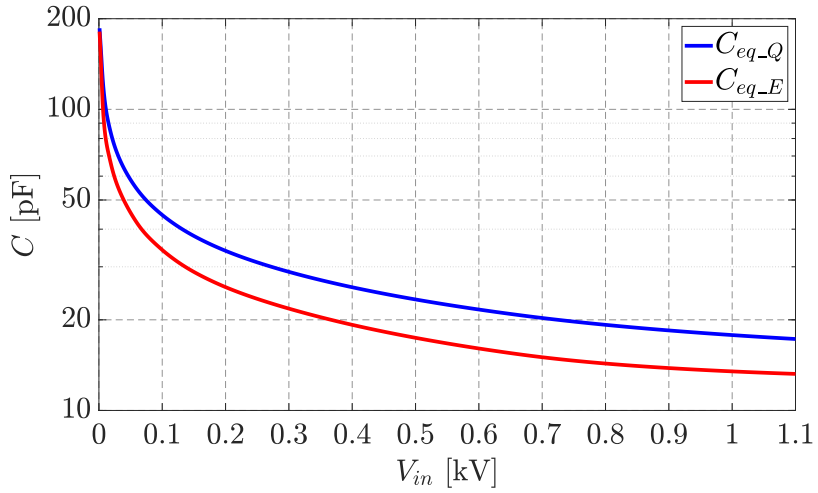


Fig. 3.4: Charge equivalent (C_{eq_Q}) and energy equivalent (C_{eq_E}) linear capacitance of the MOSFET with respect to operating DC voltage (V_{in}),in blue and red, respectively.

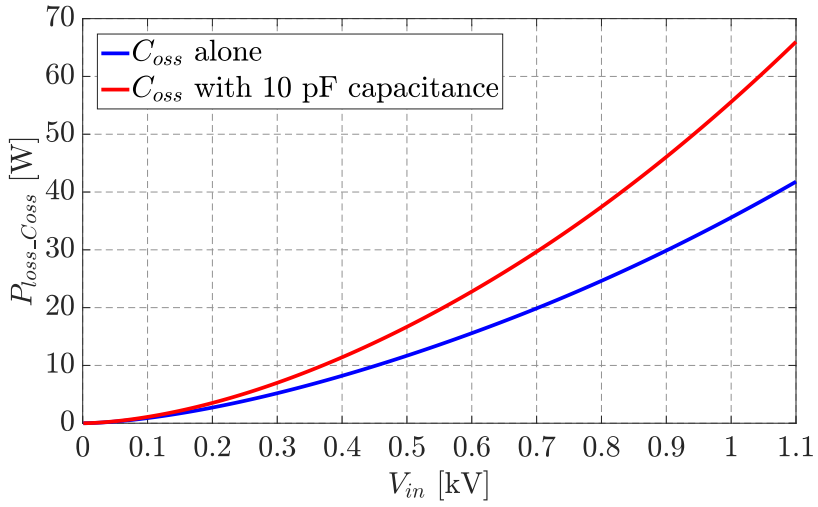


Fig. 3.5: Energy lost in a H-bridge due to parasitic capacitance across device(s) with respect to DC bus voltage (V_{in}).

loss due to output capacitance will be present in CFI with ZCS as described in section 2.1.1 which makes use of CFI in high voltage system less efficient. So, with VFI, it is important to discharge the parasitic output capacitances before turning on a MOSFET or in other words have ZVS turn on.

The fundamental principle of achieving zero voltage turn on of a MOSFET is to make its body diode conduct before its gate pulses are applied so that the energy in device's output capacitance is not lost into the device [77]. For a typical half bridge configuration

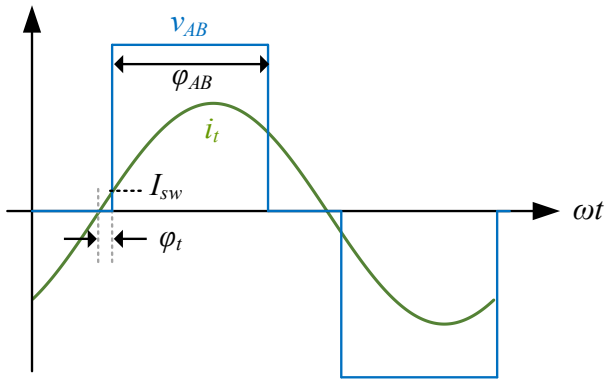


Fig. 3.6: Voltage (v_{AB}) and current (i_t) waveform of a full bridge phase shift modulated inverter.

of switches this can be achieved if the current out of switch node is sufficiently negative when the bottom switch is turned off. Circuit topology of a converter can be carefully chosen/designed to have this benefit of achieving natural zero voltage turn on. However, it is not always guaranteed to operate under such scenario across the load range of the converter, due to various operating constraints.

The resonant converters employed in this work uses a full bridge VFI as presented in Fig. 2.2(a) in chapter 2. Typical waveform of inverter output voltage (v_{AB}) and current (i_t) are shown in Fig. 3.6 where the positive zero crossing of i_t leads positive rising edge of i_t by an angle ϕ_t. Depending on the resonant tank, its operating point, load and inverter modulation angle (ϕ_{AB}), angle ϕ_t can be positive or negative making I_{sw} positive or negative which means ZVS is not guaranteed for the leading leg (leg A) MOSFETs. Hence a ZVS assisting circuit is necessary for leg A when I_{sw} is positive. On the other hand, since the resonant tank is designed to operate $F \geq 1$, tank current at the positive falling edge will always be positive which means MOSFETS in lagging leg (leg B) will have ZVS (full or partial) turn on. Due to half wave symmetry in v_{AB}, the conditions for ZVS remains similar in the negative half of v_{AB}.

Different kinds of passive and active methods are proposed in literature to achieve ZVS for a half-bridge configuration of active switches within a converter [71, 78, 79]. In these methods, an auxiliary circuit is added to the switching leg which helps in achieving zero

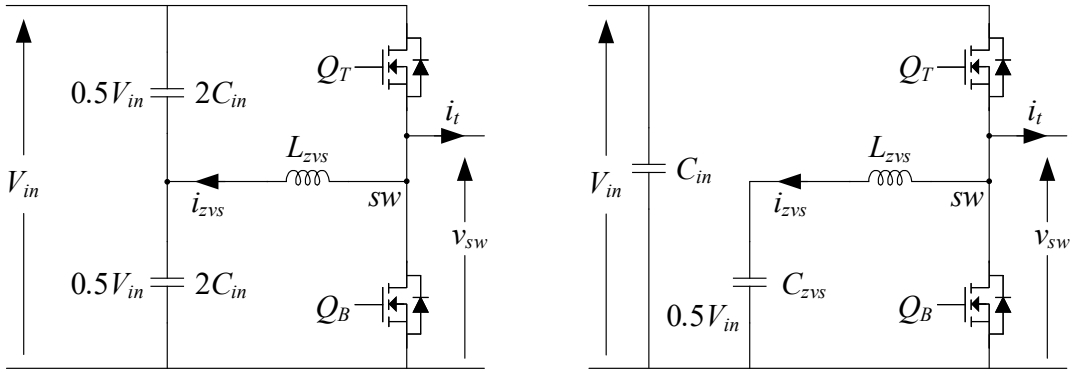


Fig. 3.7: A voltage fed half-bridge circuit with passive inductive auxiliary leg (a) with DC bus mid point available (b) without DC bus mid point available.

voltage turn on of the MOSFETs in a half-bridge. These methods are explored next in this chapter and suitable ZVS assisting technique(s) are developed for use with the resonant converters used in constant current distribution system.

3.1 Passive ZVS Assisting Techniques

A simple passive auxiliary ZVS assisting circuit is presented in [70] where an inductor is connected between switch node of a half-bridge and the mid point of dc bus, as shown in Fig. 3.7(a). However, the DC bus mid point may not be available in all systems. An alternate passive ZVS assisting circuit is presented in Fig. 3.7(b) where the ZVS assisting inductor (L_{zvs}) is in series with a DC blocking capacitor (C_{zvs}), connected between the switching node and DC bus return. The corresponding theoretical switching waveforms are presented Fig. 3.8. In Fig. 3.8, the voltage at switch node sw swings between V_{in} and zero with 50 % duty ratio at the switching frequency (f_s). So, the voltage seen by L_{zvs} (v_{Lzvs}) is a square waveform of magnitude ($\pm 0.5V_{in}$), which results in a triangular AC current (i_{zvs}) with amplitude I_{zvs} in the assisting branch whose peak and valley are synchronized with the switching transitions of the half bridge leg.

As it can be seen from Fig. 3.8, the auxiliary inductor provides a negative current out of the switching node sw at the instant when bottom MOSFET Q_B is gated off. Now,

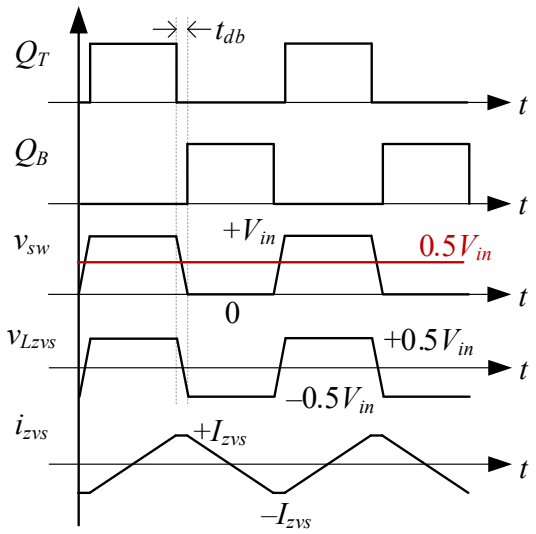


Fig. 3.8: Switching waveforms of a half-bridge circuit with passive inductive auxiliary leg.

depending on the value of i_t at the switching transition (I_{sw}), and input voltage V_{in}, L_{zvs} can be chosen such that the overall current out of switch node is sufficiently negative at the turn off instant of Q_B so that the effective capacitance at switch node (C_{sw}) is charged to V_{in} within dead time (t_{db}) and top MOSFET Q_T can turn on with zero voltage across it. A similar passive ZVS assisting circuit is presented in [80] where the current in assisting leg is pseudo-resonant. The value of L_{zvs} should be chosen in such a way that the minimum value of I_{zvs} is sufficient to overcome I_{sw} to ensure ZVS and this corresponding value of L_{zvs}, L_{zvs_max} can be calculated as

$$L_{zvs\_max} = \frac{V_{in}}{8f_s\left(I_{sw} + \frac{C_{sw}V_{in}}{t_{db}}\right)}. \tag{3.4}$$

It is assumed here that the tank current has very little change during the dead-time interval and the inductive ZVS assisting branch behaves as a constant current source during the dead-time period. The capacitance at switch node (C_{sw}) is taken as the charge equivalent linear capacitance of the MOSFETs. The passive ZVS assisting circuit shown in Fig. 3.7(b) is tested with a series resonant converter operating at 400 kHz whose details are presented in Table 3.1 and the converter test setup is shown in Fig. 3.9. Details of this

Table 3.1: Details of the SRC with passive ZVS assisting circuit

Component / Parameter	Part Number / Value
I_g [A]	1
I_{out} [A]	0.33
f_s [kHz]	400
P_{out_max} [W]	450
L_r [µH]	101.6
C_r [nF]	1.6
Transformer turns ratio	1:2
MOSFET	C2M1000170D (2 in parallel)

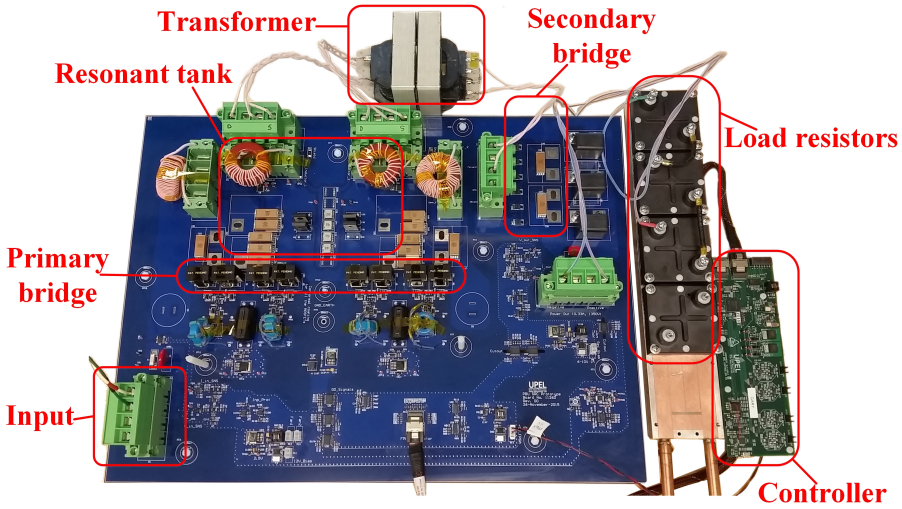


Fig. 3.9: Photograph of the SRC setup for testing passive ZVS assisting circuit.

converter can be found in [81, 82].

The steady state waveform of tank current i_t, inverter output voltage v_{AB}, current in ZVS branch i_{zvs} and total current out of node A, $(i_t + i_{zvs})$ are shown in Fig. 3.10. This test was performed at full load with 1 A input current source and a load resistance of 4120 Ω with the phase shift modulation angle adjusted to regulate the output current at 0.33 A current. The value of L_{zvs} required to achieve ZVS for the MOSFETs was 39 µH in this experiment, whereas the calculated value from (3.4) was 44 µH. It can be seen from the red waveform in Fig. 3.10 that the total switch node current of leg A is negative at the positive

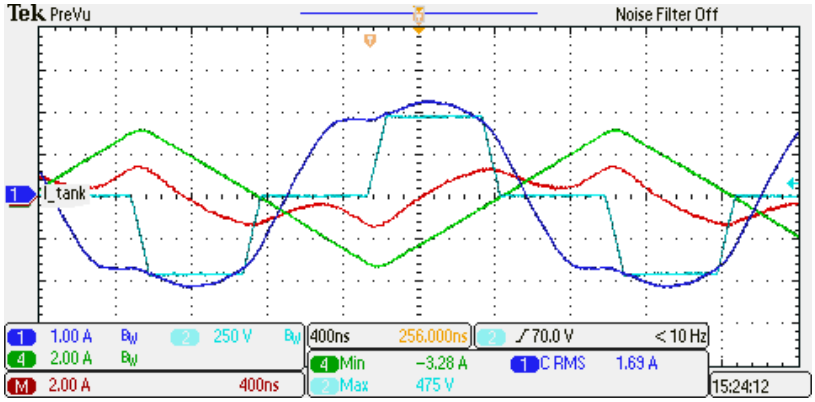


Fig. 3.10: Steady state waveform of the converter operating at rated load with $L_{zvs} = 39\,\mu\text{H}$. CH1 (blue): i_t, CH2 (cyan): v_{AB}, CH4 (green): i_{zvs}, CHM (red): total current out of switching node of leg A ($i_t + i_{zvs}$).

rising edge of v_{AB} signifying ZVS turn on of leg A top switch.

Next, experiments were performed with different output load resistance values while regulating the output current at 0.33 A. The value of L_{zvs} was adjusted such that the current in the ZVS assisting branch is enough to achieve ZVS for the MOSFETs. These values of L_{zvs_max} from this experiment are plotted in Fig. 3.11 along with the calculated values of L_{zvs_max} from (3.4) to compare the analytical and experimental results. The experimental data points in Fig. 3.11 (magenta dots) are interpolated to get a smooth plot of L_{zvs_max} at different R_{load}. Deviation between analytical and experimental value of L_{zvs_max} is primarily due to the assumptions of tank current being sinusoidal and constant during the transition period.

Steady state waveform of the converter at 50 % load, with $L_{zvs} = 28\,\mu\text{H}$ to achieve ZVS, is shown in Fig. 3.12. It can be seen from Fig. 3.12 that v_{AB} reaches V_{in}, just before the gate-source signal for top device of leg A is about to turn on, thus demonstrating ZVS operation.

The efficiency of the power converter, with the maximum L_{zvs} for a given load, is plotted in Fig. 3.13 where blue dots are actual measured data and these data points are interpolated to get a smooth plot shown in dashed blue line. The efficiency for minimum load is 82.3 % and for the full load is 94.5 %. The red dots in Fig. 3.13 represent measured

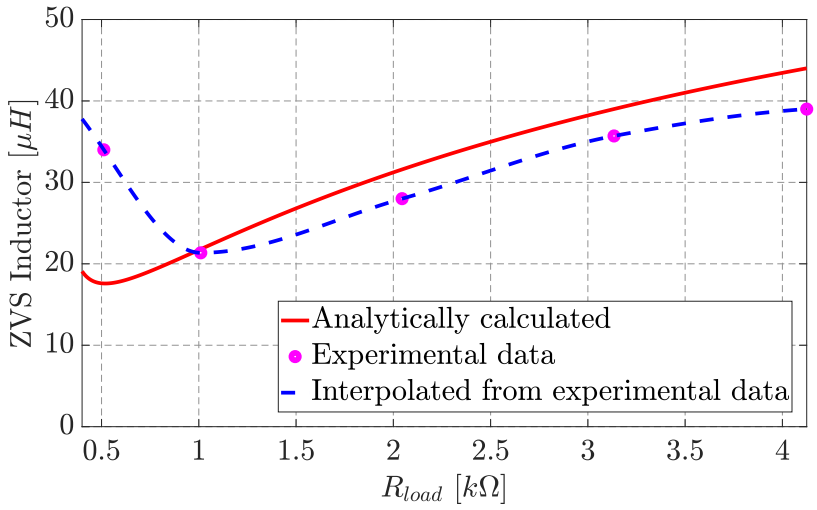


Fig. 3.11: Comparison of analytical and experimental values of L_{zvs_max} at different load resistance (R_{load}) with output load current regulated at 0.33 A. Red: analytical result, magenta: experimental data, dashed blue: interpolated curve from experimental data.

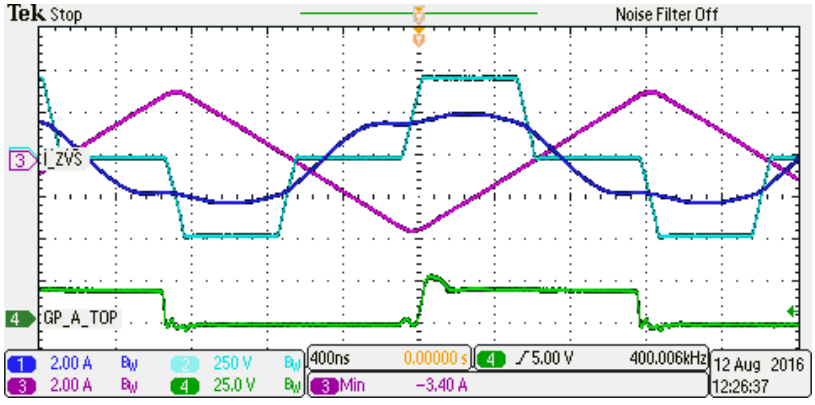


Fig. 3.12: Steady state waveform of the converter operating at 50 % load with $L_{zvs} = 28\,\mu$H. Blue (CH1): CH1 (blue): i_t, CH2 (cyan): v_{AB}, CH3 (purple): i_{zvs}, CH4 (green): gate-source signal of top MOSFET in leg A.

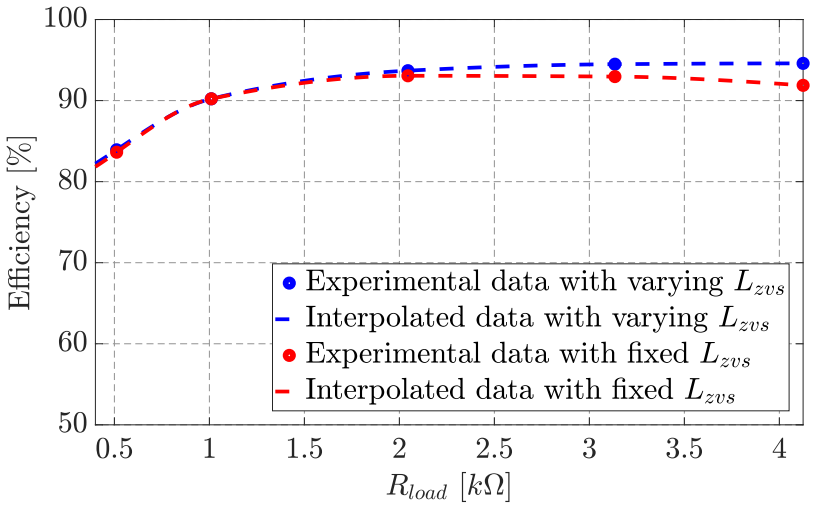


Fig. 3.13: Efficiency of the converter at different R_{load} with output load current regulated at 0.33 A. Blue: efficiency with different adjusted L_{zvs} to achieve ZVS at different load, red: efficiency with fixed $L_{zvs} = 21.4\,\mu$H.

efficiency data points with fixed value of $L_{zvs} = 21.4\,\mu$H ($\approx 22\,\mu$H), and the red dashed line is the result of interpolation to get a smooth curve. This value of L_{zvs} is chosen in a way so that ZVS is achieved for 25 % to 100 % load using a single inductor and therefore inductance of 22 µH is selected. For loads less than 25 %, MOSFETs are expected to have partial hard switching. But, for light loads, V_{in} is also reduced which results in lower switching loss. In addition, EMI due to partial hard switching at light load is not a concern because of the low value of V_{in}. With the fixed L_{zvs}, efficiency is 82 % for minimum load and 92 % for full load. It can be seen from Fig. 3.13 that with the fixed L_{zvs}, efficiency of the converter at higher load drops despite having ZVS of the MOSFETs. This is due to higher loss in the ZVS assisting branch and the main MOSFETs of leg A, resulting from more than necessary current in the branch because of higher value of V_{in} at heavy loads.

The passive auxiliary circuit shown in Fig. 3.7 is a simple solution to achieve ZVS and works very well if the converter operating point is fixed *e.g.* narrow range of DC input voltage V_{in} and small variation in load or the ZVS requirements vary within a small range when the DC input source is current source with varying V_{in}. But, if the input DC voltage and the load vary over a range such that the ZVS requirements also vary over a wide range, the advantages of passive auxiliary circuit falls short as either it can not provide

sufficient assisting current to maintain ZVS across the operating range or have more than necessary current in itself over a range of operating conditions. This causes either a increase in switching loss in main converter or increase in conduction loss in the auxiliary circuit, both of which are detrimental for efficient power conversion.

In order to achieve ZVS with a passive auxiliary circuit, over the entire input voltage and load range, the auxiliary circuit has to designed for the worst case scenario such as minimum input voltage with minimum load. But, this could result in more than necessary current in the auxiliary circuit, at other operating points, causing high rms current in the assisting inductor. This results in excessive conduction loss in the auxiliary circuit making the converter efficiency poor. In [69, 83] a modified passive auxiliary circuits are presented which replaces the single inductor ZVS assisting circuit by an LCL network. The new LCL passive auxiliary circuit reshapes the assisting current in such a way that necessary current for discharging device capacitances are provided but at the same time rms current in the auxiliary circuit is reduced. A comparison of single inductor v LCL auxiliary circuit is provided in In [69, 83]. However, the range of operating points for which the rms current is low, is narrow.

A saturable inductor based technique is proposed for full-bridge converter in [84] which can reduce conduction loss in the inductor. Coupled magnetics based auxiliary circuits are proposed in [85–88] which can assist in achieving ZVS. In [85], the proposed auxiliary circuit provides ZVS assistance for a set of switches for a dual active bridge series resonant converter. A new modulation strategy is proposed here which helps in achieving ZCS. In [86] the auxiliary inductor helps in achieving ZVS under light load conditions in conjunction with the transformer leakage inductance which can provide ZVS under heavy load conditions. A coupled winding including an auxiliary inductor is used for ZVS assistance in [87], similar to [85]. However, passive ZVS assisting circuit can be designed for a specific operating point or a narrow range of operating points. In [88], the assisting circuit is focused on achieving ZVS for one leg and ZCS for another, employing coupled magnetics. Advantages of having ZCS in one leg is that there are no circulating current during zero output voltage

of the primary side inverter *i.e.* when there in no power transfer and thus reduces the conduction loss. In addition, making the current zero in the circuit eliminates the chance of transformer saturation. However, the turn on loss in the MOSFET is not totally eliminated with ZCS (Fig. 3.5) and can result in unacceptable EMI levels.

In transformer isolated converters magnetizing inductance of the transformer can also be utilized for ZVS assistance. In [89,90], a hybrid half/full bridge converter is introduced which has the benefit of lower ripples at the input and output of the converter when compared to conventional full-bridge converter. It is discussed in these papers how the modified hybrid topology helps in achieving ZVS with the help of transformer's magnetizing inductance L_m of the half bridge circuit with reduced rms current from L_m of conventional full-bridge converter. There is no requirement of ZVS assisting leg, as in full-bridge converter, since the half bridge circuit helps with that. However, it is mentioned that the lagging leg may not achieve ZVS under light load conditions and may need ZVS assistance.

The passive auxiliary circuits used for ZVS assistance discussed so far has advantages of simple implementation methods, high reliability etc. These are well suited for converters whose operating domain is limited to a narrow range. For a converter operating over a wide range of input or output, such as resonant converters with constant current input in underwater DC distribution system, a fixed passive ZVS assisting circuit will result in poor power conversion efficiency due to high conduction loss. Hence, to optimize the ZVS assisting circuit, in order to improve circuit performance, active methods of ZVS assistance are needed.

3.2 Active ZVS Assisting Techniques

For the converters in DC current distribution system, the input voltage of each series connected power converter module(s) varies over a wide range as a function of the load power. This behavior brings unique challenges to maintaining zero voltage switching (ZVS) for resonant converters, making simple passive techniques impractical for applications with a wide load range. Hence, active ZVS assisting circuits are preferred to achieve ZVS over the resulting wide input voltage and load range.

Active ZVS assistance methods can control the ZVS assisting current injected into the switching node of the converter. This is very helpful when there is large variation in DC input voltage or the converter operates over wide load range. Controlling the assisting current to the right amount ensures minimum conduction loss in the auxiliary circuit which is the major drawback of passive auxiliary circuit based zero voltage turn on assistance.

Among various active ZVS assistance methods in literature, auxiliary resonant commutated pole (ARCP) [91] presents a simple method of achieving ZVS with low conduction loss in the assisting circuit. The auxiliary circuit provides necessary current for the main switches only when it's needed in a switching period and does not conduct for the remaining time. This helps in achieving ZVS for the main switches and at the same time keeps the rms current low in the auxiliary circuit. A similar resonant snubber with auxiliary switches is presented in [92]. In [93], the presented method of ZVS assistance is also based on an active auxiliary circuit whose operating principle is same as ARCP. However, the circuit implementation is different and employs a transformer in the auxiliary circuit.

An auxiliary half-bridge based ZVS assisting circuit is presented in [94], for a full-bridge converter. An inductor is connected between switching node of the main bridge and added auxiliary leg. The switches in the auxiliary leg are switched in such a way so that the ZVS assisting current is a short pulse of triangular current similar to the assisting current in ARCP. A generalized approach to use coupled inductor in conjunction with active switches to assist for soft switching is presented in [95]. Switch controlled inductor (SCI) introduced in [96] is used for achieving ZVS [97] for some of the active switches and ZCS for the remaining.

The active ZVS assistance circuits discussed so far, suffer from a major drawback of not having zero voltage turn on of the auxiliary switches themselves. Some of them have zero current turn on and off for the auxiliary switches, but, will dissipate the energy stored in their output capacitances resulting in higher loss and more importantly may result in higher EMI due to high dv/dt. This problem can be avoided if the ZVS assisting inductor is made to conduct for the entire switching period, with a trapezoidal shaped current, as

mentioned in [77]. But, this technique needs two converters operating together which may not be the case always. However, similar ZVS assistance can be achieved using an auxiliary half-bridge leg, for a single full-bridge converter. The disadvantage of this ZVS assisting technique is that the rms current in the assisting leg can be high, when wide input voltage operation is demanded.

Another method of controlling the ZVS assistance is presented in [98] where a simple inductor based passive auxiliary circuit is used for achieving ZVS. The current in the auxiliary circuit is adaptively controlled by modifying the operating frequency of the converter. However, operating a converter with variable switching frequency has its own drawbacks such as challenge in EMI filter design, gate driver design, introduction of low frequency oscillations when multiple converters are operated in series or parallel etc.

Various modulation strategies for full-bridge resonant converters have been proposed in [48, 62–65] where asymmetrical voltage cancellation (AVC) or asymmetric duty control (ADC) is used over symmetric voltage cancellation (SVC) or phase shift modulation (PSM) techniques. These modified modulation strategies help in achieving ZVS of the active switches by aligning the switch transition instants properly with respect to the resonant tank current. These methods, however, are complex in implementation or are dependent on the load. In addition, AVC and ADC introduces even order harmonics into the tank network which results in higher total harmonic distortion (THD) in tank current and often causes EMI for surrounding circuits.

3.2.1 Active ZVS Assisting Circuit

The active ZVS assisting circuit used in this work is shown in Fig. 3.14 where a half bridge (leg Z) is connected to leg A of the main inverter through an inductor L_{zvs} in series with a DC blocking capacitor C_{zvs}. The purpose of C_{zvs} is to block any DC component arising in v_{AZ} due to mismatch in leg A and leg Z. The ideal operating waveform of the ZVS assisting circuit is shown in Fig. 3.15.

In Fig. 3.16 waveform from a hardware prototype employing active ZVS assisting circuit of Fig. 3.14 is shown where the switch node voltage of leg A (v_A) is shown in blue, gate-

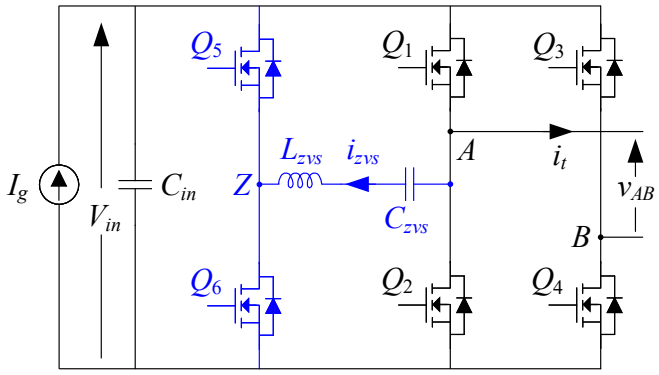


Fig. 3.14: Full bridge inverter with active ZVS assisting circuit.

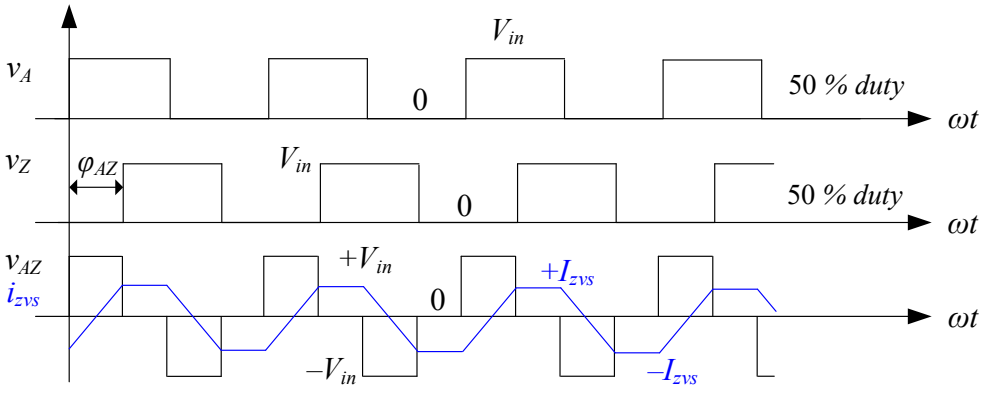


Fig. 3.15: Modulation of active ZVS assisting leg.

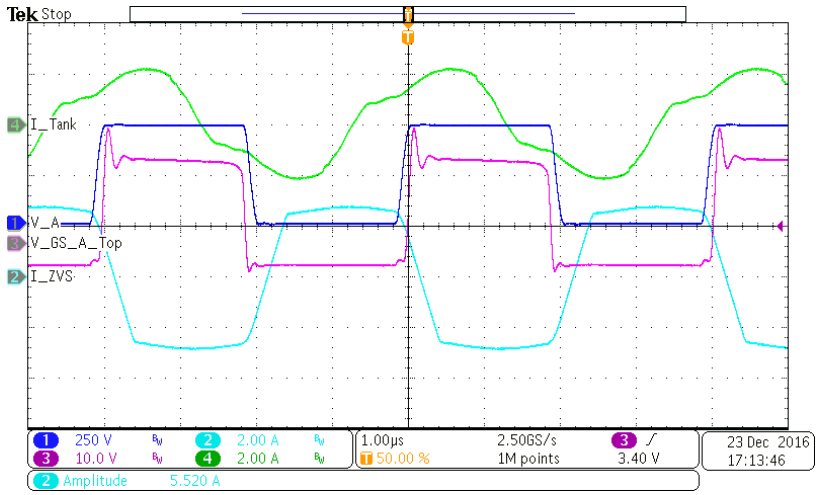


Fig. 3.16: Operating waveform of the ZVS assisting circuit of Fig. 3.14. CH1 (blue): v_A, CH2 (cyan): $-i_{zvs}$, CH3 (purple): $v_{GS\_A\_T}$, CH4 (green): i_t.

source signal for the top MOSFET in leg A ($v_{GS\_A\_T}$) is shown in purple, inverter current i_t is shown in green and the ZVS assisting current in reverse polarity ($-i_{zvs}$) is shown in cyan. It can be seen from this result that v_A clamps to DC input voltage before $v_{GS\_A\_T}$ is on, implying ZVS turn on.

The required current for ZVS assistance (I_{zvs}) is calculated as

$$I_{zvs} = C_{sw\_eq\_Q}\frac{V_{in}}{t_{db}} + I_{sw\_A}, \tag{3.5}$$

where $C_{sw\_eq\_Q}$ is the charge equivalent linear capacitor of switch node of leg A at the operating DC input voltage (V_{in}) and I_{sw_A} is the current out of leg A during the commutation from bottom switch to top switch in leg A and it is assumed to have negligible variation during the dead-time (t_{db}). The desired value of I_{zvs} is obtained by controlling ϕ_{AZ} which is given as

$$I_{zvs} = \frac{\phi_{AZ}V_{in}}{4\pi f_s L_{zvs}} \quad \Rightarrow \quad \phi_{AZ} = \frac{4\pi f_s L_{zvs} I_{zvs}}{V_{in}}. \tag{3.6}$$

Value of auxiliary inductor L_{zvs} is selected based on the lowest load (V_{in}) at which ZVS is desired, I_{zvs} calculated from (3.5) and maximum value of ϕ_{AZ} that is 180°. Equation (3.5) gives the value of current required in the auxiliary inductor L_{zvs} to achieve ZVS in the

main leg. Here, it should be noted that the same current I_{zvs} does ZVS for the switches in the auxiliary leg as well. Assuming all the switches have the same output capacitance, the auxiliary switch output capacitance is discharged (and charged) with a higher current than the main switches ($I_{zvs} - I_{sw\_A}$). This results in increased dv/dt at the switch node of the auxiliary leg and depending on the magnitude of I_{zvs}, the dv/dt value could be very high which can trigger false turn on of the switches [75] and thus impact reliability of circuit operation. The dv/dt value at the switch node Z can be given by

$$\left.\frac{dv}{dt}\right|_Z = \frac{I_{zvs}}{C_{sw\_eq\_Q\_Z}}, \tag{3.7}$$

where $C_{sw\_eq\_Q\_Z}$ is the charge equivalent capacitance at the switch node Z. From (3.5) and (3.7), it can be seen that the dv/dt rate at node Z cannot be reduced by controlling t_{db} and I_{zvs} is decided by the requirements from main switches in leg A. Hence, the dv/dt rate at node Z is reduced by increasing $C_{sw\_eq\_Q\_Z}$, by adding external capacitance (C_{ext_Z}) across the switch(es) whose value is determined by

$$C_{ext\_Z} = \frac{1}{2}\left[\frac{I_{zvs}}{\left(\frac{dv}{dt}\right)_{limit}} - C_{sw\_eq\_Q\_Z}\right]. \tag{3.8}$$

In (3.8), based on a desired dv/dt limit value, C_{ext_Z} can be evaluated. Addition of capacitances across switches do increase conduction loss some, but do not increase switching losses in the converter since these capacitors are charged and discharged by i_{zvs}, before device turn on. For selecting C_{ext_Z}, we need to select dv/dt limit on node Z which is decided by the reverse transfer capacitance of the MOSFET used ($C_{rss\_eq\_Q}$), gate drive resistance (R_G) including internal gate resistance (R_{G_int}) of the MOSFET, gate drive voltage for turning the MOSFET off (V_{drive_off}) and gate to source threshold voltage of the MOSFET (V_{GS_th}). It should also be noted that the allowed dv/dt limit should be high enough to allow discharge of switch node capacitance within dead time t_{db}, for the maximum input voltage V_{in_max}. The dv/dt limit value thus can be selected through

$$\frac{V_{in\_max}}{t_{db}} \leq \left(\frac{dv}{dt}\right)_{limit} \leq \frac{V_{GS\_th} - V_{drive\_off}}{R_G C_{rss\_eq\_Q}}. \tag{3.9}$$

It should be noted here that addition of C_{ext_Z} is not always necessary. It is required based on the application and range of operating conditions. For example, for the SRC in chapter 4 which operates up to 1 kW power, $C_{ext\_Z} = 100$ pF is connected across each devices in leg Z with a dv/dt limit considered as 15 V/ns. Whereas, for PRC in chapter 5 and LCL-T resonant converters in chapter 6 and chapter 7, the converters were operated up to 500 W and no C_{ext_Z} was added to the active ZVS assisting leg.

The steady state waveforms of active ZVS assisting circuit of Fig. 3.14 operating in conjunction with an SRC designed in chapter 4 are shown in the following figures with a comparison between use of active and passive (3.7(b)) ZVS assisting circuits. The details of the converter is presented in section 4.3 in chapter 4. The operational waveforms with active ZVS assisting circuit with $L_{zvs} = 55$ µH inductor is shown in Fig. 3.17 at 550 W output load with ZVS achieved for both main leg (leg A) and auxiliary leg (leg Z) MOSFETs. And for the same load, operational waveforms with passive ZVS assisting circuit with $L_{zvs} = 120$ µH inductor is shown in Fig. 3.18 where ZVS is almost achieved at this load. The active ZVS assisting circuit is designed to achieve ZVS from 100 W to 1 kW whereas, the passive ZVS circuit was designed for operating range of 550 W to 1 kW. The difference in ZVS assisting current (i_{zvs}) can be seen from the green trace in these two figures where i_{zvs} is trapezoidal in case of active ZVS assisting circuit and i_{zvs} is triangular with passive ZVS assisting circuit as per the waveforms presented in Fig. 3.15 and Fig. 3.8, respectively.

The converter efficiency and ZVS range for active ZVS assistance and passive ZVS assistance technique(s) are compared in Fig. 3.19. The red plot shows the case with active ZVS assistance where ZVS is maintained for full load range of 100 W to 1 kW. The blue plot depicts the efficiency when 120 µH inductor is used as passive ZVS inductor and the converter operates with complete soft-switching for load power ≈ 550 W and above. A third efficiency plot with lower passive ZVS inductor of 60 µH is portrayed by the black curve where the soft-switching operation starts from ≈ 330 W load power. However, the efficiency

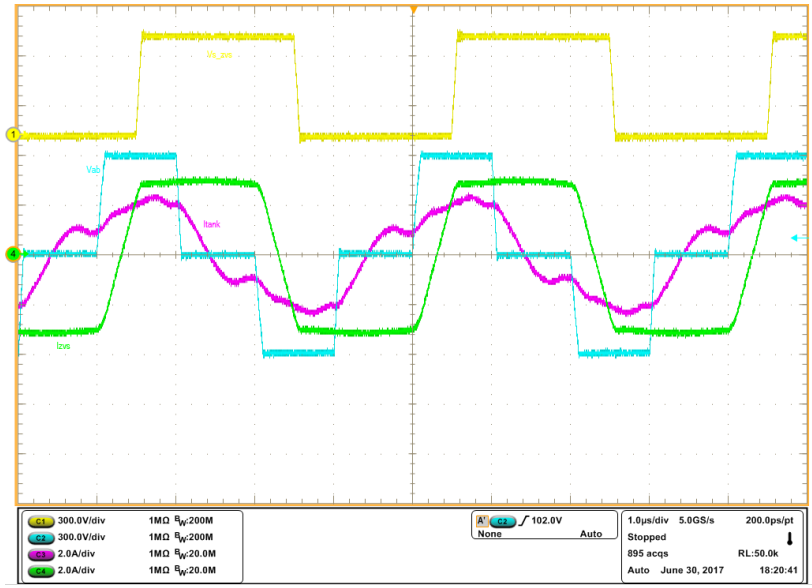


Fig. 3.17: Waveforms of SRC operation at 550 W output load, with active ZVS assistance through 55 µH inductor. CH1 (yellow): v_Z, CH2 (cyan): v_{AB}, CH3 (purple): i_t, CH4 (green): i_{zvs}.

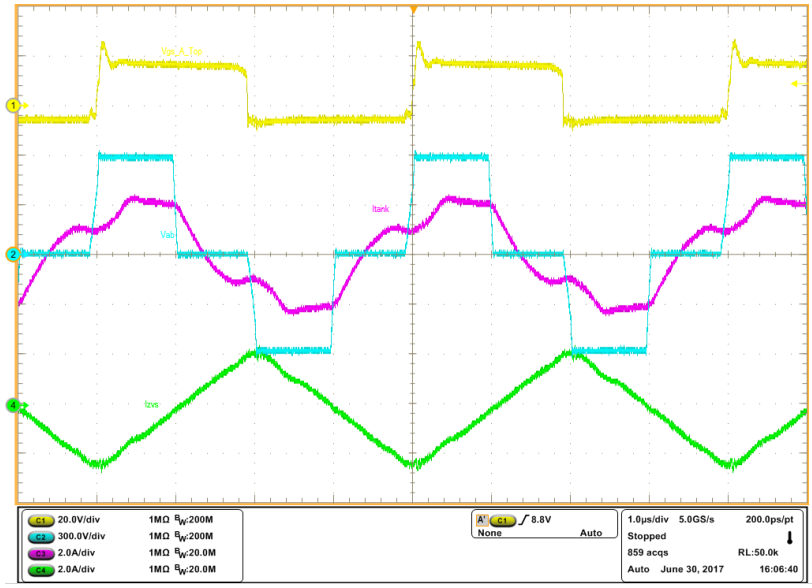


Fig. 3.18: Waveforms of SRC operation at 550 W output load, with passive ZVS assistance through 120 µH inductor. CH1 (yellow): $v_{GS\_A\_T}$, CH2 (cyan): v_{AB}, CH3 (purple): i_t, CH4 (green): i_{zvs}.

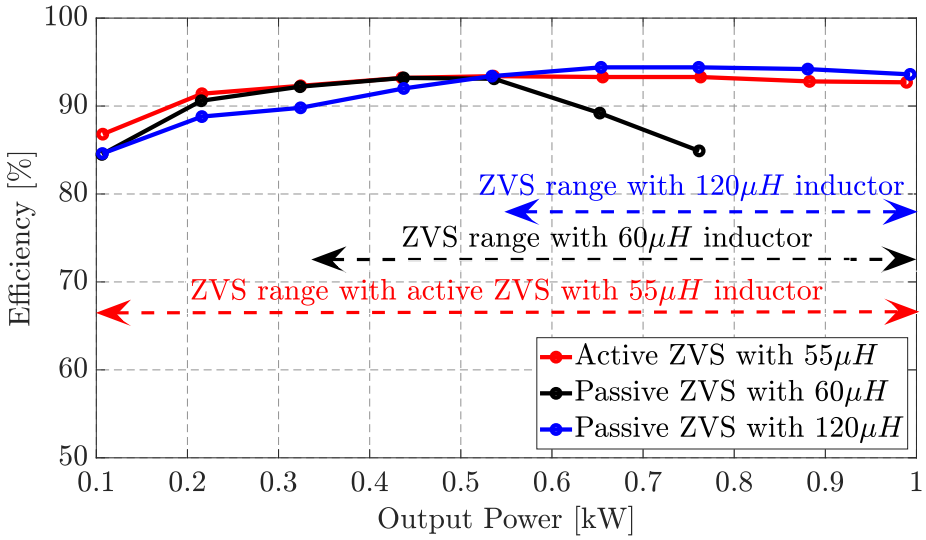


Fig. 3.19: Comparison of experimental efficiency data with different ZVS assistance. Red plot is for active ZVS with 55 µH inductor, blue plot is for passive ZVS with 120 µH inductor and black plot is for passive ZVS with 60 µH inductor.

drops drastically at higher load due to excessive ZVS assisting current and associated high dv/dt in the inverter leg (leg A) and hence not suitable for practical use. It can be seen from the red and blue plots of Fig. 3.19 that the efficiency is higher at heavy loads with passive assistance circuit owing to lower conduction loss due to absence of leg Z MOSFETs, but, due to lack of ZVS at lighter loads, it drops to a lower value than the efficiency achieved with active assistance circuit.

Summary

In this chapter the need of soft switching in converters operating with high switching frequency is presented. The requirements and advantages of ZVS over ZCS are shown for converters operating with high voltage with high frequency which is typical in converters employed in long distance underwater DC distribution system. ZVS requirements for the resonant converters used in such system are evaluated and suitable passive or active ZVS assisting circuits are presented. Since the converters with constant current input see a wide variation in input voltage over load range, passive ZVS assisting circuits are useful when the range of operating conditions are limited. Whereas, when operation with ZVS over

a wide range of operating conditions is desired, use of active ZVS assisting circuits are essential. Limitations of ZVS assisting circuits such as high dv/dt and methods to mitigate such limitations are discussed. Finally, comparisons are made for operation with passive and active ZVS assisting circuits used in a full-bridge series resonant converter to showcase their benefits over the region of operation.

CHAPTER 4

SERIES RESONANT CONVERTER FOR CONSTANT CURRENT DRIVE

In underwater DC distribution network, some converters need to regulate its output to another DC current level which then drives constant current to a local group on converters/load. In this chapter series resonant converter (SRC) is introduced and with detailed analysis it is shown how an SRC can be designed to naturally maintain constant output current over a wide load range, when the input is a constant current source. Starting with steady state modeling in section 4.1, detailed analysis is presented to derive converter output current expression and stress on resonant tank elements which is then used for designing the resonant tank elements, presented in section 4.2. The details of hardware prototype developed for experimental verification is presented in section 4.3 with results of converter operation from no load (short circuit) to full load of 1 kW showing a good match between analysis and experimental data.

4.1 Steady State Modeling and Analysis

The SRC circuit topology operating from a constant current input is shown in Fig. 4.1. On the primary side of the converter, MOSFETs $Q_1 - Q_4$ form the DC-AC inverting stage, which operates with DC input voltage V_{in}, with a symmetrical phase shift modulation between leg A and leg B with phase shift angle α and produces a quasi-square wave voltage (v_{AB}) at the inverter output, as shown in Fig. 4.2. The resonant tank is formed by inductor L_r, split in half in forward and return AC lines for symmetry, and capacitor C_r connected in series on the primary side of an $1 : n$ isolation transformer. The secondary of the transformer is connected to a diode half bridge (D_1, D_2 and D_3, D_4) based rectifier circuit (as presented in Fig. 2.7(b)) which provides additional voltage gain of two and current attenuation of half. The rectified current is filtered by output capacitors ($C_{o1} - C_{o4}$ and C_o) to provide a DC regulated current (I_{out}) to the load (R_L).

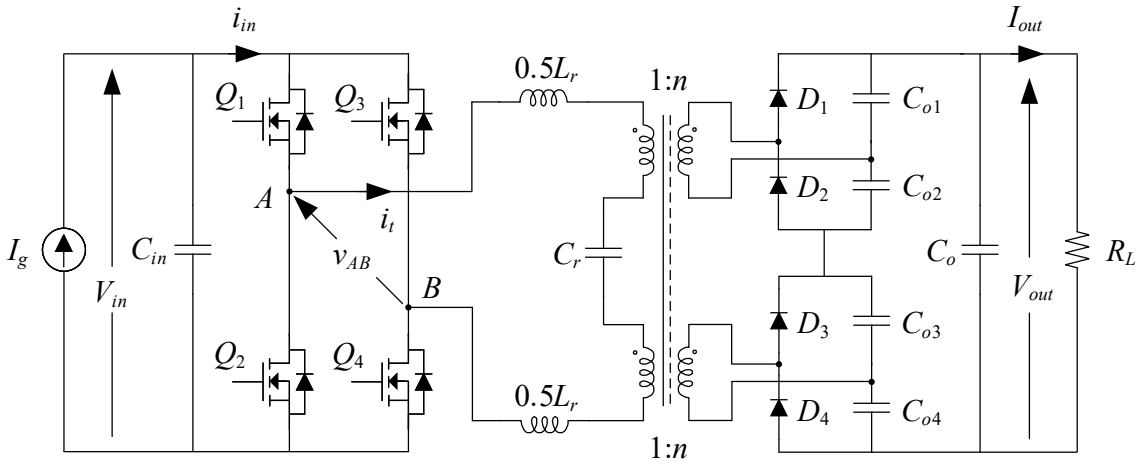


Fig. 4.1: SRC circuit topology with constant current input.

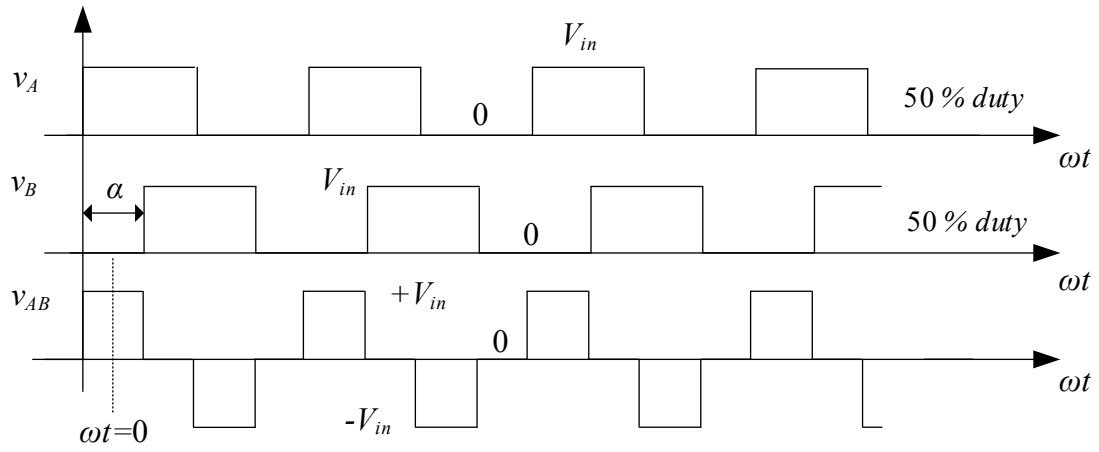


Fig. 4.2: Phase shift modulation of the primary side inverter in SRC circuit topology of Fig. 4.1.

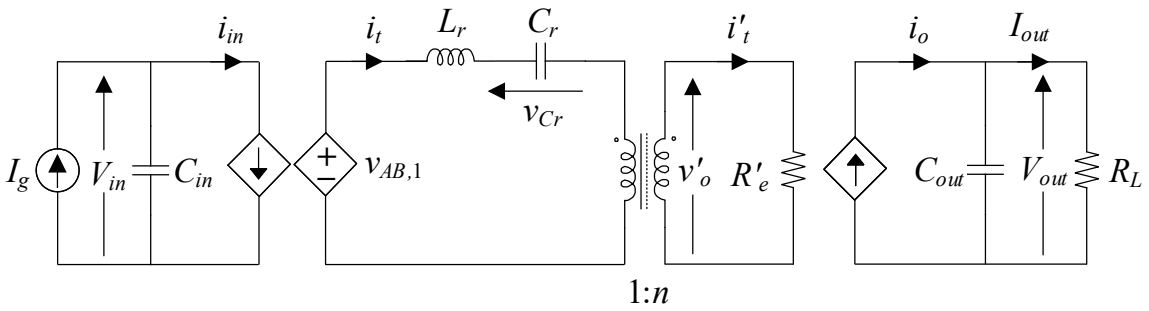


Fig. 4.3: Equivalent circuit of the SRC topology from Fig. 4.1.

The equivalent circuit of the SRC is drawn in Fig. 4.3 with FHA and assuming lossless power conversion. The fundamental inverter output voltage $v_{AB,1}$ is given by

$$v_{AB,1}(t) = \frac{4}{\pi} V_{in} \sin\left(\frac{\alpha}{2}\right) \cos(\omega_s t), \tag{4.1}$$

In Fig. 4.3, the input current is expressed as

$$I_g = \langle i_{in} \rangle = \frac{2I_t}{\pi} \sin\left(\frac{\alpha}{2}\right) \cos(\phi_{in}), \tag{4.2}$$

where ω_s is the angular switching frequency, average value of signal x is represented by $\langle x \rangle$, amplitude of AC side signal x_y is represented by X_y and signal or parameter x is expressed with a prime (x') on the secondary side of the transformer. In (4.2), ϕ_{in} is the angle between primary side inverter output voltage and current which is given as

$$\phi_{in} = \angle Z_{in}, \tag{4.3}$$

where Z_{in} is input impedance of the loaded resonant tank, seen from the primary inverter side, as depicted in Fig. 4.4. Fig. 4.4 shows the simplified AC equivalent circuit of the converter, reflected to the primary side of the transformer, which is the loaded resonant tank connected to the primary inverter.

In Fig. 4.3 and Fig. 4.4, the AC equivalent resistance is derived considering half bridge rectifier circuit in Fig. 4.1 whose waveform pattern in shown in Fig. 4.5. The two half bridge

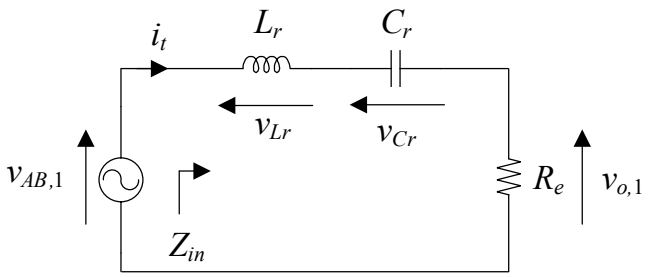


Fig. 4.4: AC equivalent circuit of the loaded series resonant tank.

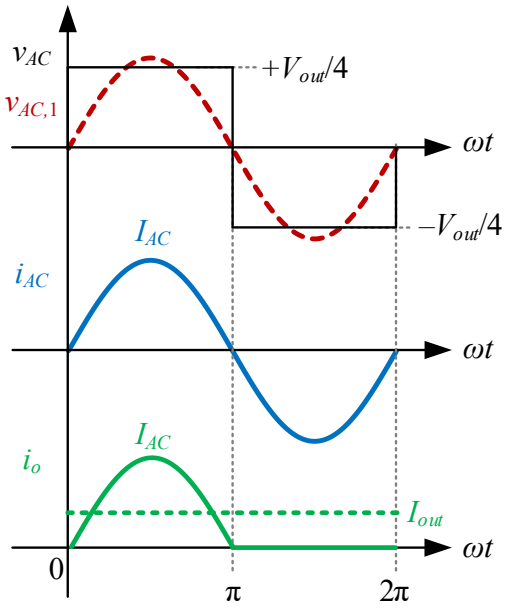


Fig. 4.5: Waveforms of the half bridge rectifier section of the SRC circuit in Fig. 4.1.

sections in Fig. 4.1, connected to each of the secondary windings, are identical and hence the AC equivalent resistance is derived for one section and then multiplied by two to get the total equivalent resistance. From Fig. 4.1, each of the half bridge capacitor(s) ($C_{o1} - C_{o4}$) has a DC voltage of magnitude $V_{out}/4$ and thus the voltage across transformer secondary is a square wave of amplitude $V_{out}/4$, as shown in Fig. 4.5 and its fundamental component is given by

$$V_{AC,1} = \frac{4}{\pi}\frac{V_{out}}{4} = \frac{V_{out}}{\pi}. \tag{4.4}$$

The rectified AC current (i_o) is half wave sinusoid for half cycle and zero for the other half and its average value is equal to the load current (I_{out}) and their relationship is given as

$$I_{out} = \langle i_o \rangle = \frac{I_{AC}}{\pi}. \tag{4.5}$$

Using the relationship between AC and DC side components in (4.4) and (4.5), the AC equivalent resistance for each of the half bridge sections can be determined as

$$R_{AC} = \frac{V_{AC,1}}{I_{AC}} = \frac{\frac{V_{out}}{\pi}}{\pi I_{out}} = \frac{1}{\pi^2}\frac{V_{out}}{I_{out}} = \frac{1}{\pi^2}R_L. \tag{4.6}$$

Now, the total AC equivalent resistance for two half bridge sections connected in series in Fig. 4.1, is given as

$$R'_e = 2R_{AC} = \frac{2}{\pi^2}R_L, \qquad R_e = \frac{2}{n^2\pi^2}R_L. \tag{4.7}$$

From the AC equivalent circuit of the loaded resonant tank in Fig. 4.4, the input impedance (Z_{in}) can be given as

$$Z_{in} = R_e + j\omega_s L_r - j\frac{1}{\omega_s C_r} = R_e + jZ_o\left(F - \frac{1}{F}\right), \tag{4.8}$$

where the parameters for the resonant tank are defined as

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}, \quad Z_o = \sqrt{\frac{L_r}{C_r}}, \quad F = \frac{\omega_s}{\omega_o} = \frac{f_s}{f_o}, \quad Q = \frac{Z_o}{R_e}. \tag{4.9}$$

The tank current (i_t) can be determined using (4.1), (4.8) and (4.9) as

$$i_t = \frac{v_{AB,1}}{Z_{in}} = \frac{4}{\pi}\frac{V_{in}\sin\left(\frac{\alpha}{2}\right)}{R_e\sqrt{1 + Q^2\left(F - \frac{1}{F}\right)^2}}\angle - \phi_{in}, \tag{4.10}$$

where ϕ_{in} is determined from (4.8) as

$$\phi_{in} = tan^{-1} \frac{Z_o \left(F - \frac{1}{F}\right)}{R_e}. \tag{4.11}$$

The output DC current can be determined from half wave rectified averaged value of i_t through transformer turns ratio and using expression from (4.10), I_{out} is given as

$$I_{out} = \frac{I_t}{n\pi} = \frac{4}{n\pi} \frac{V_{in} \sin\left(\frac{\alpha}{2}\right)}{R_e \sqrt{1 + Q^2 \left(F - \frac{1}{F}\right)^2}}. \tag{4.12}$$

With ideal, lossless power conversion, equating the input and output DC power of the converter, the input DC voltage (V_{in}) can be given as

$$V_{in} I_g = I_{out}^2 R_L \quad \Rightarrow \quad V_{in} = \frac{I_{out}^2 R_L}{I_g}. \tag{4.13}$$

Substituting V_{in} from (4.13) into (4.12), the output DC current can be expressed as

$$I_{out} = \frac{I_g}{2n \sin\left(\frac{\alpha}{2}\right)} \sqrt{1 + Q^2 \left(F - \frac{1}{F}\right)^2}, \tag{4.14}$$

and the DC output voltage is given as

$$V_{out} = I_{out} R_L = \frac{I_g R_L}{2n \sin\left(\frac{\alpha}{2}\right)} \sqrt{1 + Q^2 \left(F - \frac{1}{F}\right)^2}. \tag{4.15}$$

Substituting (4.14) in (4.13), the DC input voltage (V_{in}) can be now expressed as

$$V_{in} = \frac{I_g R_L}{4n^2 \sin^2\left(\frac{\alpha}{2}\right)} \left[1 + Q^2 \left(F - \frac{1}{F}\right)^2\right]. \tag{4.16}$$

From (4.12), using the expression of I_{out} from (4.14), the tank current can be given as

$$i_t(t) = \frac{\pi}{2} \frac{I_g}{\sin\left(\frac{\alpha}{2}\right)} \sqrt{1 + Q^2 \left(F - \frac{1}{F}\right)^2} \cos\left(\omega_s t - \phi_{in}\right). \tag{4.17}$$

From the expression of i_t in (4.17), the voltage across the resonant capacitor is given as

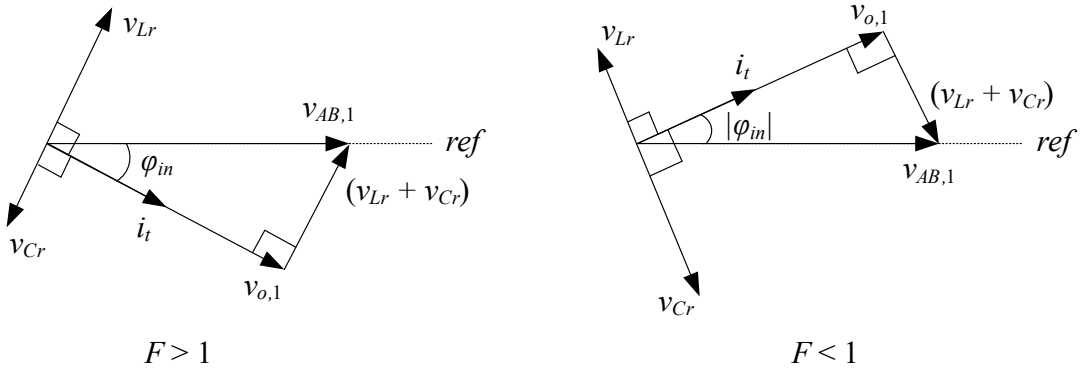


Fig. 4.6: Phasor diagram for the signals of the loaded series resonant tank for $F > 1$ and $F < 1$.

$$v_{Cr}(t) = -j\frac{Z_o}{F}i_t = \frac{\pi}{2}\frac{Z_o I_g}{F\sin\left(\frac{\alpha}{2}\right)}\sqrt{1+Q^2\left(F-\frac{1}{F}\right)^2}\cos\left(\omega_s t - \frac{\pi}{2} - \phi_{in}\right). \tag{4.18}$$

The fundamental AC output voltage ($v_{o,1}$) from Fig. 4.4, can be expressed as

$$v_{o,1}(t) = i_t R_e = \frac{\pi}{2}\frac{I_g R_e}{\sin\left(\frac{\alpha}{2}\right)}\sqrt{1+Q^2\left(F-\frac{1}{F}\right)^2}\cos\left(\omega_s t - \phi_{in}\right). \tag{4.19}$$

From (4.17) and (4.18), the rms tank current ($I_{t,rms}$) and capacitor voltage ($V_{Cr,rms}$) can be obtained as

$$I_{t,rms} = \frac{\pi}{2\sqrt{2}}\frac{I_g}{\sin\left(\frac{\alpha}{2}\right)}\sqrt{1+Q^2\left(F-\frac{1}{F}\right)^2}, \tag{4.20}$$

$$V_{Cr,rms} = \frac{\pi}{2\sqrt{2}}\frac{Z_o I_g}{F\sin\left(\frac{\alpha}{2}\right)}\sqrt{1+Q^2\left(F-\frac{1}{F}\right)^2}. \tag{4.21}$$

The phasor diagram for the AC quantities in Fig. 4.4 can now be drawn from the expressions in (4.1), (4.17), (4.18) and (4.19), which is shown in Fig. 4.6. In Fig. 4.6, the phasor diagram is shown for both $F > 1$ and $F < 1$ cases where the tank current lags the inverter output voltage for $F > 1$ and tank current leads the inverter output voltage for $F < 1$.

4.2 Design of Series Resonant Converter

Based on the steady state modeling and derivations presented in the last section, the operating point and resonant tank elements are designed in this section.

4.2.1 Operating Point

From the DC output current expression in (4.14), it can be seen that the output current is dependent on operating conditions *e.g.* F, α, load and tank components (Q) and transformer (n). The normalized output current with a given transformer (n) and control angle (α) is expressed as

$$I_{out\_norm} = \frac{I_{out}}{I_{base}} = \sqrt{1 + Q^2 \left(F - \frac{1}{F}\right)^2}, \tag{4.22}$$

where I_{base} is defined as

$$I_{base} = \frac{I_g}{2n \sin\left(\frac{\alpha}{2}\right)}. \tag{4.23}$$

The variation of normalized output current (I_{out_norm}) with respect to normalized switching frequency (F) is plotted in Fig. 4.7, for different load (Q). And from this plot, it can be seen that at $F = 1$, *e.g.* when the converter is operated at switching frequency equal to its resonant frequency, the DC output current becomes independent of load, when supplied from constant current source. Moreover, as established in section 2.2, at $F = 1$ there remains no restriction on minimum power operation for which output can be regulated.

With $F = 1$, the DC output current from (4.14) can now be expressed as

$$I_{out}|_{F=1} = \frac{I_g}{2n \sin\left(\frac{\alpha}{2}\right)}. \tag{4.24}$$

The input and output DC voltage at $F = 1$, from (4.16) and(4.15) are given as

$$V_{in}|_{F=1} = \frac{I_g R_L}{4n^2 \sin^2\left(\frac{\alpha}{2}\right)}, \tag{4.25}$$

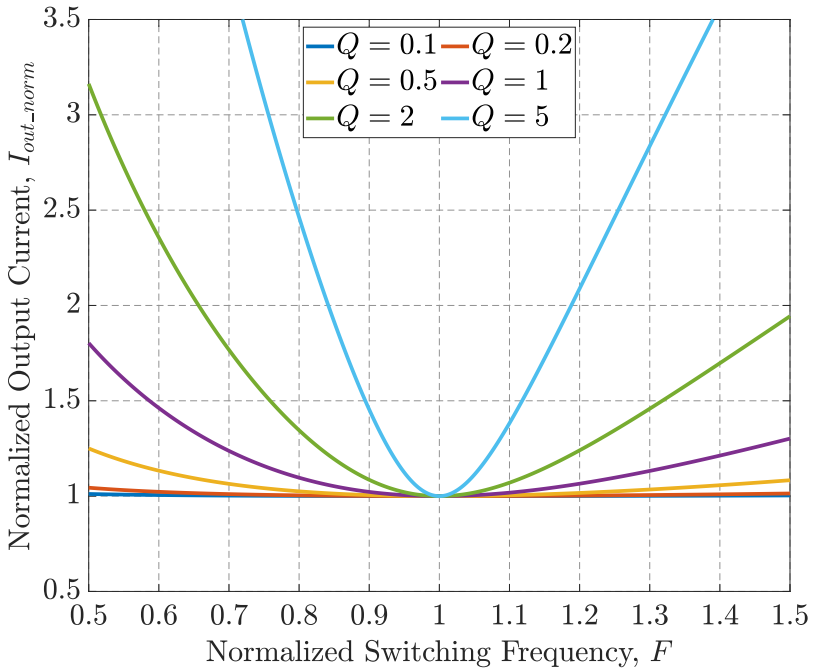


Fig. 4.7: Normalized output current v normalized switching frequency.

$$V_{out}|_{F=1} = \frac{I_g R_L}{2n \sin\left(\frac{\alpha}{2}\right)}. \tag{4.26}$$

From these expressions (4.24 – 4.26) it can be seen that I_{out} is independent of load but, both the input and output DC voltage increases with load.

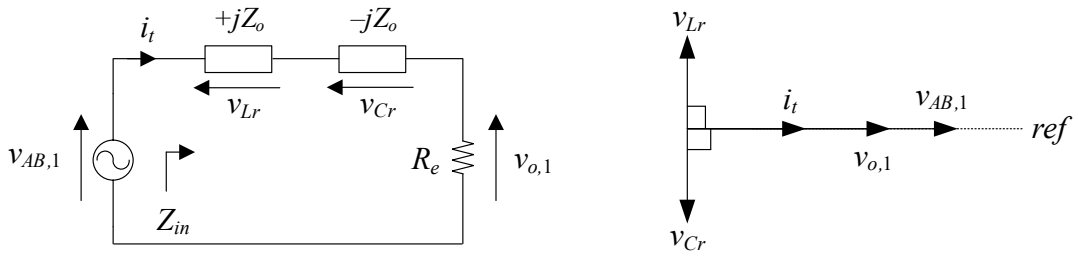
4.2.2 Component Stress

The rms values of tank signals at $F = 1$, from (4.20) and (4.21), are expressed using (4.24) as

$$I_{t,rms}|_{F=1} = \frac{\pi}{2\sqrt{2}} \frac{I_g}{\sin\left(\frac{\alpha}{2}\right)} = \frac{n\pi}{\sqrt{2}} I_{out}, \tag{4.27}$$

$$V_{Cr,rms}|_{F=1} = \frac{\pi}{2\sqrt{2}} \frac{Z_o I_g}{\sin\left(\frac{\alpha}{2}\right)} = \frac{n\pi}{\sqrt{2}} Z_o I_{out}. \tag{4.28}$$

The input impedance (Z_{in}) and power factor (PF) for the inverter are determined at $F = 1$, from (4.8) and (4.11) as



(a) (b)

Fig. 4.8: (a) AC equivalent circuit of the loaded series resonant tank and (b) its phasor diagram at $F = 1$ operating point.

$$Z_{in}|_{F=1} = R_e, \tag{4.29}$$

$$\phi_{in}|_{F=1} = 0 \quad \Rightarrow \quad PF|_{F=1} = \cos(\phi_{in})|_{F=1} = 1. \tag{4.30}$$

The AC equivalent circuit from Fig. 4.4 can be redrawn at $F = 1$ as shown in Fig. 4.8(a) and corresponding phasor diagram for the AC signals are shown in Fig. 4.8(b).

It can be seen Fig. 4.8 that at $F = 1$, the SRC becomes a pass-through converter with inverter output voltage ($v_{AB,1}$), tank current (i_t) and AC output voltage ($v_{o,1}$), all in phase. Thus, it behaves as load independent constant current drive, from a constant current source, at a given operating angle (α) for a given transformer turns ratio. Moreover, from Fig. 4.8(a), it can be seen that the tank impedance, series combination of L_r and C_r, becomes zero at $F = 1$ and thus the load independent output characteristics is ideally independent of tank components. This gives wide variety of options for designing the resonant tank components.

Using the rms value expressions from (4.27) and (4.28), the VA of the tank inductor (S_{Lr}) and tank capacitor (S_{Cr}) can be given as

$$S_{Lr} = I_{t,rms}^2 Z_o = \frac{n^2\pi^2}{2} I_{out}^2 Z_o, \tag{4.31}$$

$$S_{Cr} = \frac{V_{Cr,rms}^2}{Z_o} = \frac{n^2\pi^2}{2} I_{out}^2 Z_o. \tag{4.32}$$

Using the expression of R_e from (4.7), the quality factor of the loaded resonant tank from (4.9) can be written as

$$Q = \frac{n^2\pi^2 Z_o}{2R_L}. \tag{4.33}$$

Using (4.33) in (4.31) and (4.32), the VA of the tank elements can be expressed in the form

$$S_{Lr} = S_{Cr} = QI_{out}^2 R_L = QP_{out}, \tag{4.34}$$

where, P_{out} is the DC output power. It can be seen from (4.34) that the VA rating or the size of the tank is proportional to the quality factor (Q).

4.2.3 Resonant Tank Design

To design the converter with low component rating and size, Q should be minimized, which, from (4.33) means n and Z_o need to be minimized. Reduced transformer turns ratio also means lower rms current in the tank which means lower losses in the primary bridge ($Q_1 - Q_4$). However, there is a limit on minimizing transformer turns ratio. From the expression of I_{out} in (4.24), it can be seen that the minimum output current is achieved at $\alpha = 180°$ and this minimum value is given as

$$I_{out\_min} = \frac{I_g}{2n}, \tag{4.35}$$

which means transformer turns ratio should be higher than a minimum value (n_{min}) for output current to be regulated at I_{out_reg} which can be written in the form

$$n > n_{min} = \frac{I_g}{2I_{out\_reg}}. \tag{4.36}$$

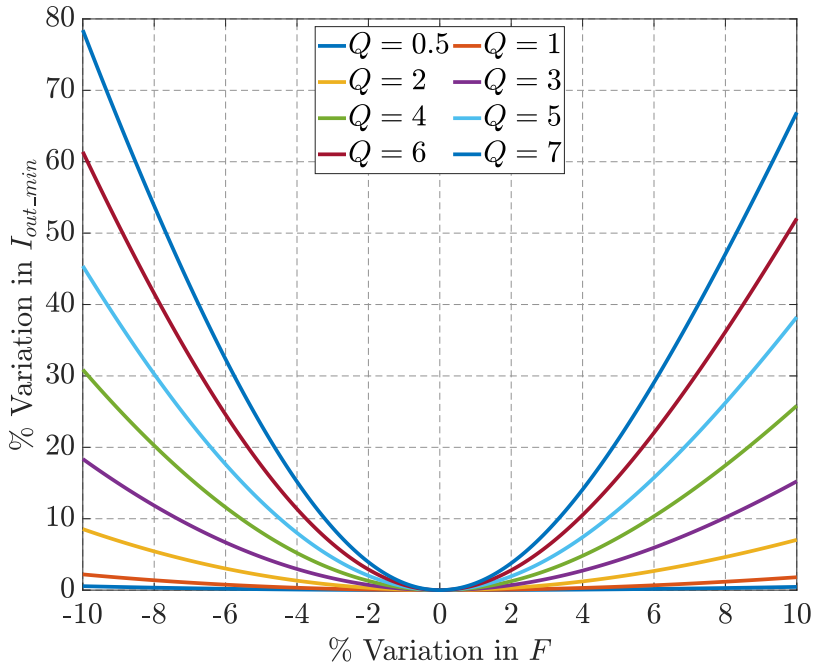


Fig. 4.9: Variation in minimum output current (I_{out_min}) v variation in normalized switching frequency (F), for different Q.

Designing the converter with $n = n_{min}$ is idealistic and leaves no room for output regulation under tank component tolerance. Using the output current expression from (4.14) with minimum output current, the tolerance on I_{out_min} can be given as

$$I_{out\_min\_tol} = \frac{\frac{I_g}{2n}\sqrt{1 + Q^2\left(F - \frac{1}{F}\right)^2} - I_{out\_min}|_{F=1}}{I_{out\_min}|_{F=1}} = \sqrt{1 + Q^2\left(F - \frac{1}{F}\right)^2} - 1. \quad (4.37)$$

In Fig. 4.9, it is shown how tolerance on components *i.e.* variation of F deviates the minimum output current, for different choice of Q. And from this plot it can be seen that higher the tolerance in F lower the Q needs to be in order to keep the variation in I_{out_min} within certain limit. Since Q is higher at lighter load, the constrain on Q should be evaluated for the minimum load (P_{out_min}) for which output is desired to be regulated controlling the primary inverter phase angle.

For any transformer turns ratio n with $n > n_{min}$, the output current limitation from (4.37) can be established as

Table 4.1: SRC design constraints parameters

Parameter	Value
I_g [A]	1
I_{out_reg} [A]	0.33
P_{out_max} [W]	1000
T_{Lr} [%]	10
T_{Cr} [%]	5

$$\frac{I_g}{2n}\sqrt{1+Q^2\left(F-\frac{1}{F}\right)^2} \leq \frac{I_g}{2n_{min}}, \tag{4.38}$$

which, under limiting case, operating at minimum load, gives

$$\frac{I_g}{2n}\sqrt{1+Q_{mL}^2\left(F-\frac{1}{F}\right)^2} = \frac{I_g}{2n_{min}} \quad \Rightarrow \quad Q_{mL} = \left|\frac{\sqrt{\frac{n^2}{n_{min}^2}-1}}{F-\frac{1}{F}}\right|, \tag{4.39}$$

where Q_{mL} is the quality factor at minimum load which needs to evaluated at the minimum and maximum value of F, under component tolerance. For a given tolerance specification on tank inductor (T_{Lr}) and tank capacitor (T_{Cr}) the minimum and maximum value of F can be determined from (4.9) as

$$F_{max} = \frac{1}{\sqrt{(1-T_{Lr})(1-T_{Cr})}}, \quad F_{min} = \frac{1}{\sqrt{(1+T_{Lr})(1+T_{Cr})}}. \tag{4.40}$$

For a resonant converter, with use of a class I ceramic capacitor (C0G, NP0), which is stable over temperature and voltage bias, the capacitance tolerance is within $\pm 5\,\%$ and the tolerance in inductor is considered to be within $\pm 10\,\%$. With these tolerance levels and other parameters listed in Table 4.1, the minimum load is considered to be $10\,\%$ of rated load for which the limitation on Q is evaluated using (4.39). The limitation on Q is plotted in Fig. 4.10 with respect to transformer turns ratio (n), for maximum and minimum value of F.

From Fig. 4.10, it can be seen that higher the n, converter can be designed with high Q which will increase size of the tank components and also have increased conduction loss due

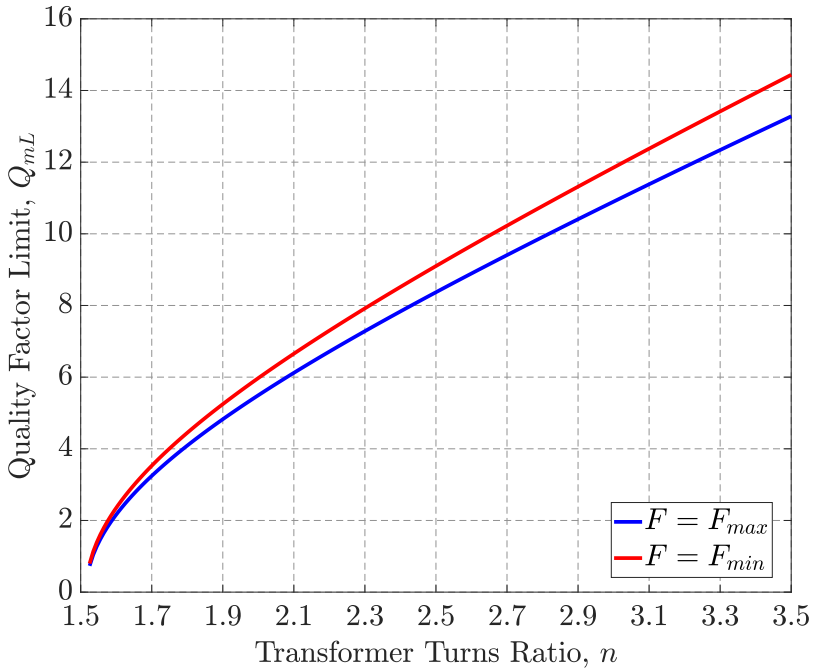


Fig. 4.10: Quality factor limit (Q_{mL}) v variation in transformer turns ratio (n), for $F = F_{max}$ (blue) and $F = F_{min}$ (red).

to higher rms current (4.27). On the other hand, for design with lower n, Q will be lower and thus size and losses can be lower. However, the limiting quality factor (Q_{mL}) shown in Fig. 4.10 is for 10 % load which means at full load, Q will be 10 times lower compared to Q_{mL} which may lead to converter operation into DCM with increased harmonics in tank current, at higher loads. Considering these trade-offs, the SRC design point is chosen for $n = 2$ and $Q_{mL} = 6$ which means the load quality factor will vary between 6 and 0.6 for 10 % to 100 % load. With this design choice, the minimum output current is $I_{out\_min} = 0.25\,\text{A}$ which gives $\approx 25\,\%$ margin from desired output current of $I_{out\_reg} = 0.33\,\text{A}$.

With the selected Q_{mL} and n, characteristics impedance (Z_o) of the tank can be found out from (4.33) with corresponding load resistance of R_{mL} and is given as

$$Z_o = \frac{2R_{mL}Q_{mL}}{n^2\pi^2}. \tag{4.41}$$

From Z_o, the resonant tank components can be evaluated from (4.9) as

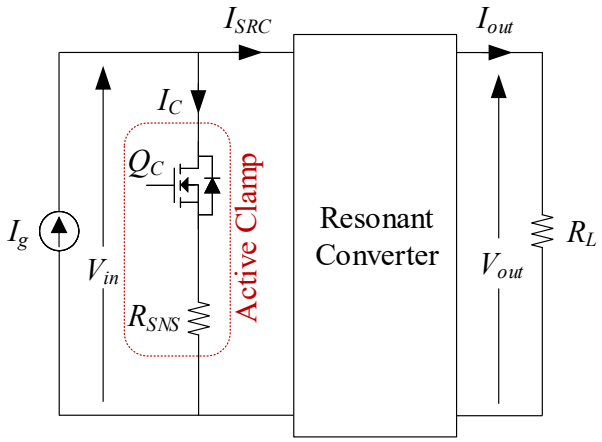


Fig. 4.11: Active clamp circuit in conjunction with SRC topology shown in Fig. 4.1.

$$L_r = \frac{Z_o}{2\pi f_o} = \frac{Z_o}{2\pi f_s}, \qquad C_r = \frac{1}{2\pi f_o Z_o} = \frac{1}{2\pi f_s Z_o}, \tag{4.42}$$

and their ratings can be found using (4.27) and (4.28). The steady state operating α can be evaluated from (4.24) as

$$\alpha = 2\sin^{-1}\left(\frac{I_g}{2nI_{out\_reg}}\right). \tag{4.43}$$

Ideally, the SRC operating with $F = 1$ can regulate its output from full load to no load (short circuit at the output). However, under non-ideal scenario with component tolerances, based on the design, the converter may lose control below 10 % load. Hence, an active clamp circuit is augmented at the front end of the SRC to bypass the source current under light loads, as shown in Fig. 4.11 and thus reduces the effective DC input current to the SRC. Under normal operating conditions, the active clamp branch will be idle and the input current to the SRC will be equal to source current *i.e.* $I_{SRC} = Ig$ and when the inverter cannot regulate I_{out} through α *i.e.* α hits the limit of 180°, active clamp circuit will shunt a part of the source current given as

$$I_{SRC} = I_g - I_C. \tag{4.44}$$

This active clamp circuit is also utilized for system start-up and shut-down and protects the converter under faults by bypassing the input current from the converter [99].

The design of resonant tank elements presented here is done considering the tolerance on components. However, there may be different other ways for designing the resonant tank components. One such way is to design by limiting the stress on the tank inductor or capacitor, as presented in [81, 100, 101].

4.2.4 ZVS Realization

With fixed frequency, phase shift modulation, switches in the lagging leg (leg B) achieves zero voltage switching (ZVS) by the tank current itself, but the leading leg (leg A) will not have ZVS. To ensure ZVS for leg A switches for the entire load range, an ZVS assisting circuit needs to be augmented to the converter leg A. Since the input DC voltage varies over wide values, proportional to load, an active ZVS assisting circuit presented in section 3.2.1 that consists of an auxiliary half bridge leg (leg Z) and ZVS assisting inductor (L_{zvs}) in series with a capacitor (C_{zvs}), as shown in Fig. 4.12, is used here to achieve ZVS turn on of the MOSFETs in leg A [102]. The amount of ZVS assistance is controlled by controlling the phase shift angle between leg A and this auxiliary leg, over the load range, as presented in chapter 3. If the converter output load range is relatively small then a passive ZVS assisting circuit can also be employed by connecting an inductor and DC blocking capacitor from switch node of leg A to DC bus return, as discussed in chapter 3.

4.3 Experimental Results

A prototype series resonant converter for 1 A input to 0.33 A output conversion, operating at 250 kHz has been developed with the parameters shown in Table 4.2, following the design method presented earlier in this chapter. The hardware setup of the converter is shown in Fig. 4.13 and is tested from short circuit (no load) to a power level of 1 kW (full load). The converter has been tested for its output current characteristics in steady state.

Steady state operating waveforms of the converter with short circuit output (no load) is shown in Fig. 4.14. The waveforms operating at $\alpha = 180°$ is shown in Fig. 4.14(a) and

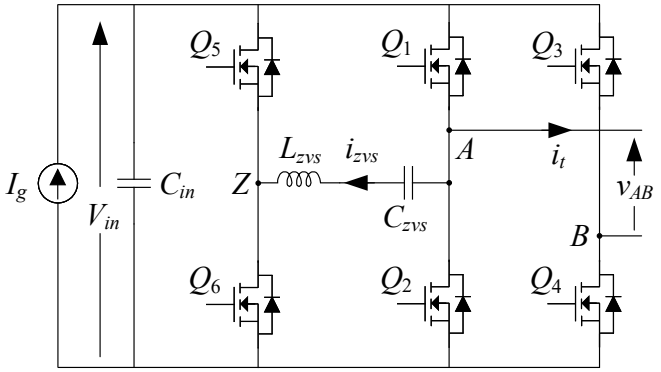


Fig. 4.12: Active ZVS assisting circuit for leg A MOSFETs.

Table 4.2: Details of the series resonant converter

Component / Parameter	Part Number / Value
I_g [A]	1
I_{out} [A]	0.33
f_s [kHz]	250
P_{out_max} [W]	1000
L_r [µH]	174.2
C_r [nF]	2.33
n	2
$Q_1 - Q_6$	C2M1000170D (2 in parallel)
$D_1 - D_4$	C4D02120E (3 in series)
C_{in} [µF]	3.9
$C_{o1} - C_{o4}$ [µF]	0.1
C_o [µF]	0.47
L_{zvs} [µH]	50

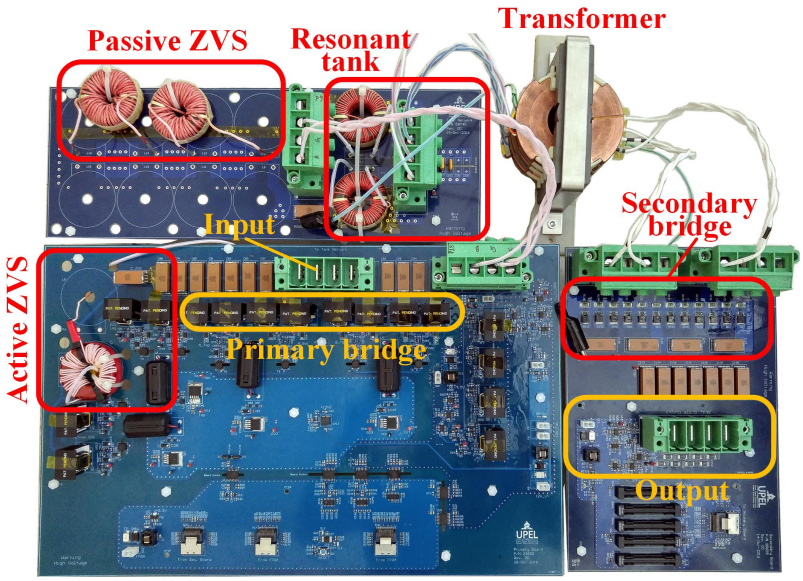
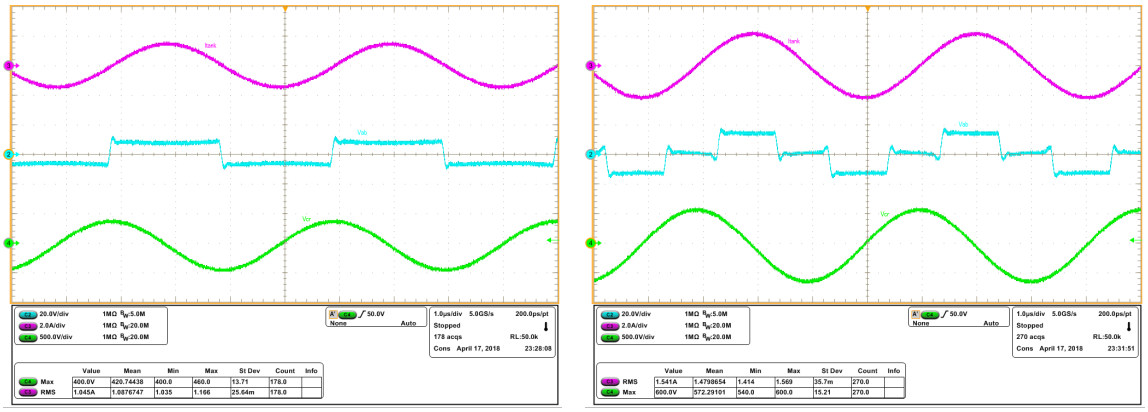


Fig. 4.13: Photograph of the test setup.



(a) (b)

Fig. 4.14: Steady state operating waveforms of the resonant tank signals with short circuit load (a) at $\alpha = 180°$ and (b) at $I_{out} = 0.33\,\text{A}$. CH2 (cyan): v_{AB}, CH3 (purple): i_t, CH4 (green): $-v_{Cr}$.

the waveforms for output regulated at $I_{out} = 0.33\,\text{A}$ is shown in Fig. 4.14(b). In Fig. 4.14, CH2 (cyan) shows inverter output voltage v_{AB}, tank current i_t is shown in CH3 (purple) and CH4 (green) presents $-v_{Cr}$. And it can be seen from these plots that the tank signals are in accordance with the phasor relationship presented in Fig. 4.8(b).

The steady state waveforms of the converter, operating at the full load of 1 kW, regulating its output current at $I_{out} = 0.33\,\text{A}$ is shown in Fig. 4.15 with CH1 (yellow) representing

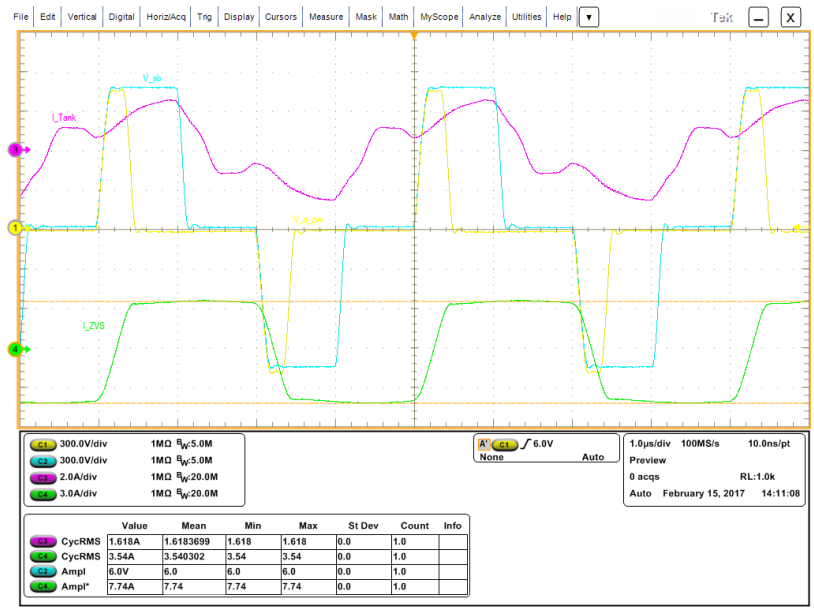


Fig. 4.15: Steady state operating waveforms of the resonant tank signals at full load of 1 kW with $I_{out} = 0.33$ A. CH1 (yellow): v_{AZ}, CH2 (cyan): v_{AB}, CH3 (purple): i_t, CH4 (green): i_{zvs}.

v_{AZ}, CH2 (cyan) showing v_{AB}, i_t presented in CH3 (purple) and CH4 (green) showing i_{zvs}. It can be seen from this plot that with active ZVS assistance, inverter MOSFETs undergo ZVS turn on. Also from the tank current waveform (i_t) presented in CH3 (purple), it can be seen that the tank current contains harmonics due to low quality factor (Q) at full load.

The output characteristics of the converter is captured in Fig. 4.16, operating with a fixed control angle of $\alpha = 180°$ for minimum output current (I_{out_min}), over the entire load resistance range. The red line in Fig. 4.16 represents the theoretically predicted result whereas, the blue line shows the experimentally measured output current. From this plot it can be observed that the output current is fairly constant over the load range with variation within $+3.18\,\%$ to $-7.24\,\%$ which is due to losses in the system and increasing amplitude of magnetizing current in the transformer with increase in output voltage as the load increases which were not considered in theoretical analysis.

The variation in control angle α, to regulate the output current at $I_{out} = 0.33$ A, is experimentally measured and plotted in Fig. 4.17, over the entire load range, by the blue curve, whereas, the red line represents the analytical value from (4.43). From this result,

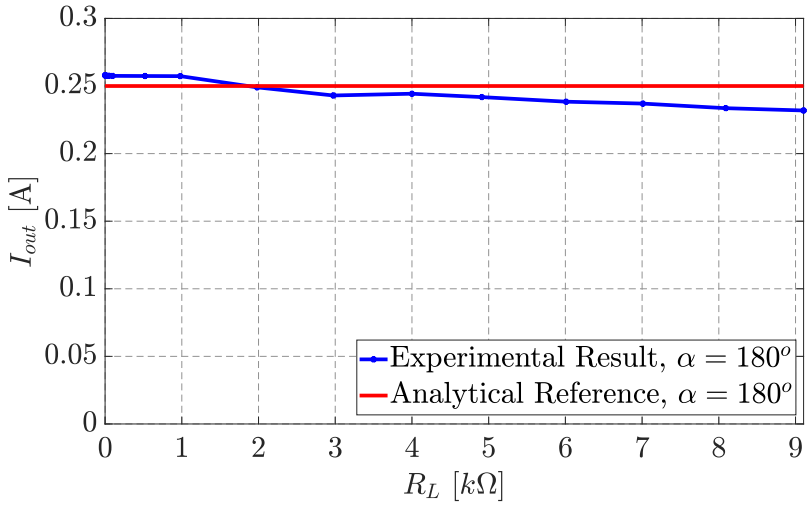


Fig. 4.16: Steady state DC output current (I_{out}) versus load resistance (R_L) with $\alpha = 180°$. Red: analytical value, blue: experimental result.

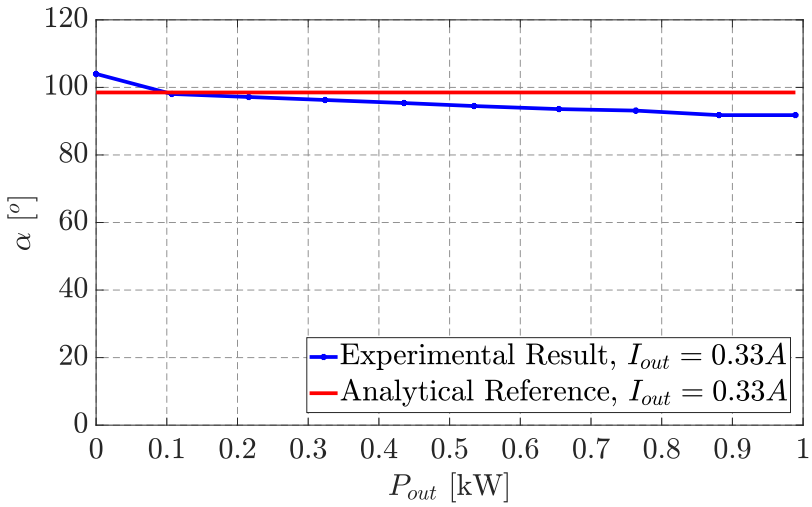


Fig. 4.17: Variation in control angle (α) over the P_{out} range of $0 - 1\,\text{kW}$, while regulating output current at 0.33 A. Red: analytical value, blue: experimental result.

it can be seen that the control effort needed to regulate the output current at the desired value varies within a small range of $\alpha = 104°$ for short circuit load to $\alpha = 91.8°$ at full load which are within $+5.58\,\%$ to $-6.81\,\%$ variation from the ideal, theoretical value.

The efficiency of power conversion from 1 A source to regulated 0.33 A output is plotted in Fig. 4.18 over the entire load range of $0 - 1\,\text{kW}$. The peak power efficiency is around $94\,\%$ with above $90\,\%$ efficiency for $20\,\%$ to $100\,\%$ load range and greater than $85\,\%$ efficiency

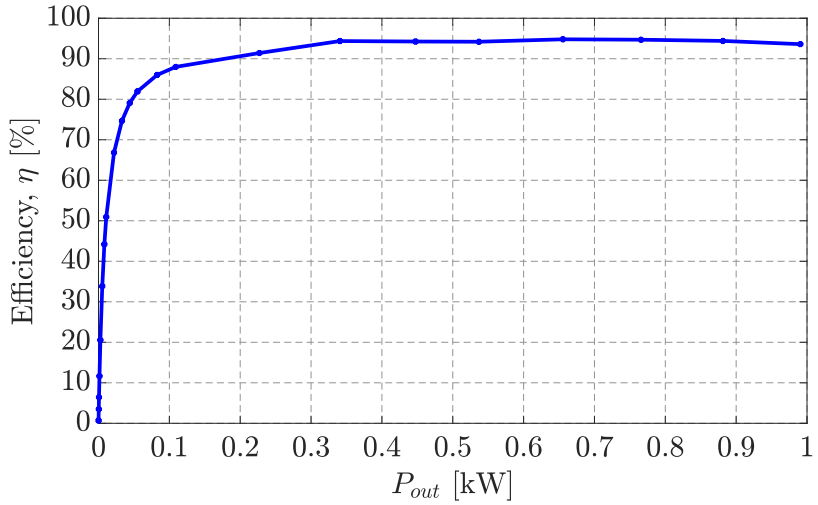


Fig. 4.18: Experimentally measured efficiency of the converter over the P_{out} range of $0 - 1\,\text{kW}$, while regulating output current at $0.33\,\text{A}$.

for load down to $10\,\%$.

Summary

In this chapter, series resonant converter is presented for constant current input to constant current output conversion in underwater DC distribution system. Steady state modeling and analysis is presented to derive the input output relationship along with stress on tank components. And from this design criteria a guideline is established for designing the converter with component tolerance in mind. Converter output control scheme under component tolerance at light loads is also presented. It is shown that with this design, the converter behaves as load independent constant current drive. Results from experimental prototype validates the analysis with operation from short circuit (no load) to a power level of $1\,\text{kW}$ (full load).

CHAPTER 5

PARALLEL RESONANT CONVERTER FOR CONSTANT VOLTAGE OUTPUT

The parallel resonant converter (PRC) is introduced and analyzed in this chapter. In underwater distribution network some converters need to feed loads which need a constant voltage source at its input. With detailed analysis it is shown how an PRC can be designed to naturally maintain constant output voltage over a wide load range, when the input is a constant current source. Steady state modeling and analysis of the converter is presented in section 5.1 to establish the DC input and output relationship. Based on this relationships, operating point and design guidelines are presented in section 5.2, along with control method, zero voltage switching realization and output filter. Experimental prototype and results are presented in section 5.3 for an PRC that regulates the output voltage to 120 V from 1 A current source for a load range of 50 W to 450 W. Then, the load independent constant output voltage characteristics of PRC is utilized to build a converter for wide output voltage range in section 5.4. A new topology incorporating parallel resonant tank with a multi-winding transformer and an output switch network that together minimize component stress and improve efficiency over the wide range of required operating conditions, is also presented with simulation and experimental results.

5.1 Steady State Modeling and Analysis

The PRC circuit topology operating from a constant current input is shown in Fig. 5.1. On the primary side of the converter, MOSFETs $Q_1 - Q_4$ form the DC-AC inverting stage, which operates with DC input voltage V_{in}, with a symmetrical phase shift modulation between leg A and leg B with phase shift angle α and produces a quasi-square wave voltage (v_{AB}) at the inverter output, as shown in Fig. 5.2. The resonant tank is formed by the inductor L_r and capacitor C_r' placed on the secondary side of an $n:1$ isolation transformer. Placing the resonant capacitor on the secondary side of the transformer absorbs the leakage

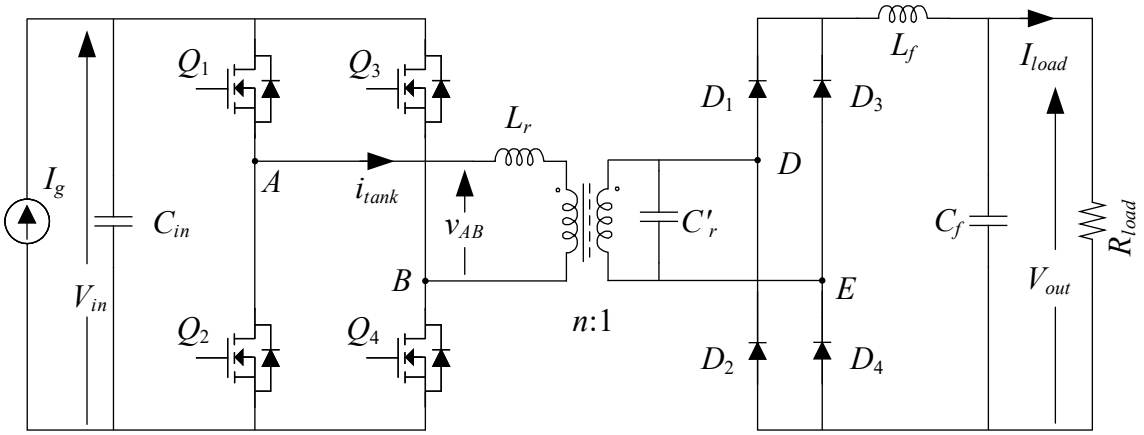


Fig. 5.1: PRC circuit topology with constant current input.

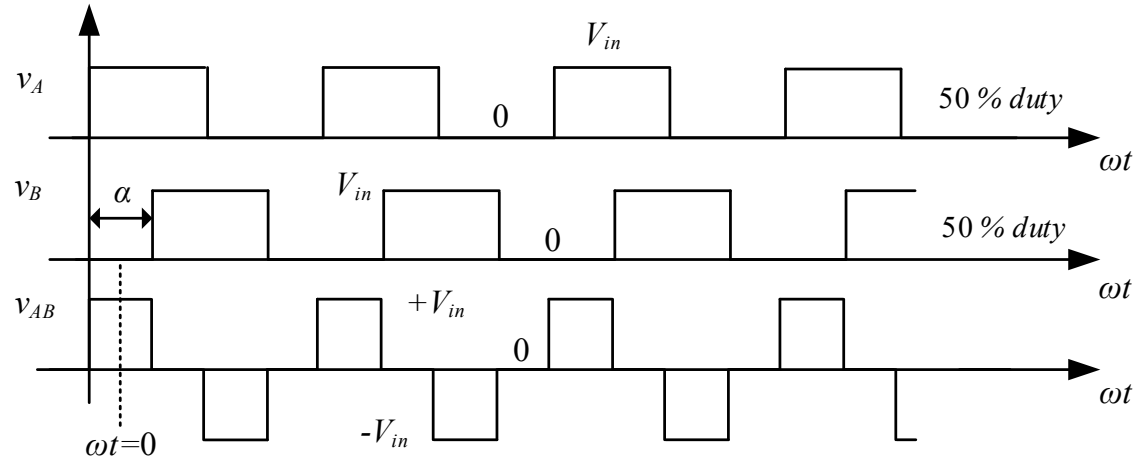


Fig. 5.2: Phase shift modulation of the inverter in PRC circuit topology of Fig. 5.1.

inductance of the high voltage isolation transformer in to the resonant inductor (L_r) and also combines the parasitic winding capacitance of the transformer in to resonant capacitor (C'_r). The voltage across the resonant capacitor is rectified and then filtered by an output filter stage formed by an inductor L_f and capacitor C_f. Input power from the constant current source I_g is processed by this converter to regulate the output voltage across the load (R_{load}) at a constant value of V_{out}.

The following analysis assumes that the converter is ideal without any loss. Also, it assumes that the loaded quality factor of the tank is high enough to filter out the harmonics generated from the inverter stage and the diode rectifier on the output stage operates un-

der continuous conduction mode (CCM). With the fundamental harmonics approximation (FHA) [67], the equivalent circuit of the AC stage in the PRC can be drawn as shown in Fig. 5.3, where the fundamental inverter output voltage $v_{AB,1}$ is given by

$$v_{AB,1}(t) = \frac{4}{\pi} V_{in} \sin\left(\frac{\alpha}{2}\right) \cos(\omega_s t), \tag{5.1}$$

In Fig. 5.3, the input current and the AC equivalent load resistance are expressed as

$$I_g = \langle i_{in} \rangle = \frac{2I_{tank}}{\pi} \sin\left(\frac{\alpha}{2}\right) \cos(\phi_{in}), \tag{5.2}$$

$$R'_e = \frac{\pi^2}{8} R_{load}, \qquad R_e = \frac{n^2\pi^2}{8} R_{load}. \tag{5.3}$$

In (5.1) – (5.3), ω_s is the angular switching frequency, average value of signal x is represented by $\langle x \rangle$, amplitude of AC side signal x_y is represented by X_y and signal or parameter x is expressed with a prime (x') on the secondary side of the transformer. In (5.2), ϕ_{in} is the angle between fundamental component of primary side inverter output voltage and current that is given as

$$\phi_{in} = \angle Z_{in}, \tag{5.4}$$

where Z_{in} is input impedance of the loaded resonant tank, seen from the primary inverter side, as depicted in Fig. 5.4. Fig. 5.4 shows the simplified AC equivalent circuit of the converter, reflected to the primary side of the transformer, which is the loaded resonant tank connected to the primary inverter.

From the circuit Fig. 5.4, the output to input voltage transfer function can be derived as

$$\frac{v_{o,1}(s)}{v_{AB,1}(s)} = \frac{1}{1 + s\frac{L_r}{R_e} + s^2 L_r C_r} = \frac{1}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}, \tag{5.5}$$

where the basic parameters for the resonant converter are given as,

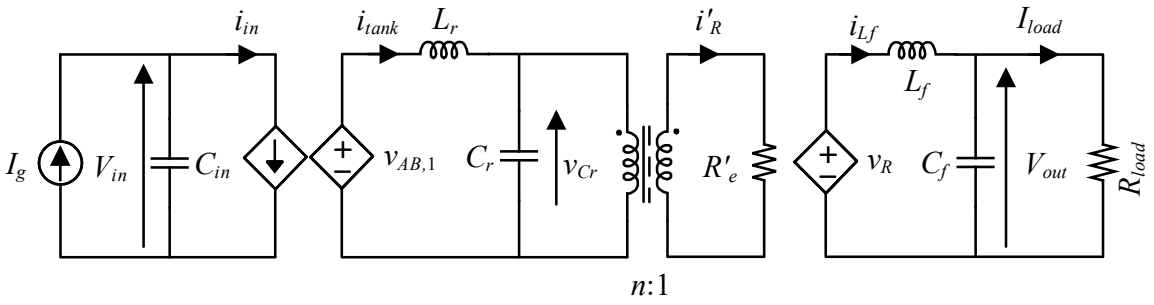


Fig. 5.3: Equivalent circuit of the PRC topology from Fig. 5.1.

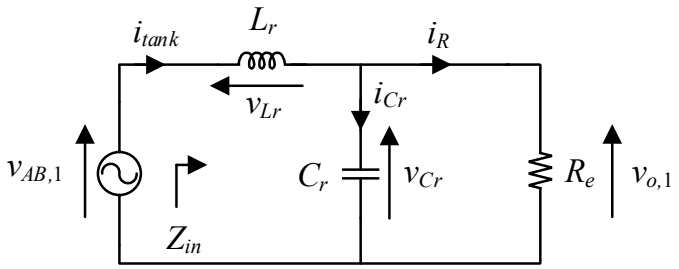


Fig. 5.4: AC equivalent circuit of the loaded parallel resonant tank.

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}, \quad Z_o = \sqrt{\frac{L_r}{C_r}}, \quad C_r = \frac{C'_r}{n^2}, \quad Q = \frac{R_e}{Z_o}, \quad F = \frac{\omega_s}{\omega_o} = \frac{f_s}{f_o}. \tag{5.6}$$

Here, f_o is the resonant frequency of L_r and C_r, ω_o is the angular resonant frequency, Z_o is the characteristic impedance of the resonant tank, Q is the loaded quality factor of the tank, f_s is the switching frequency of operation and F is the normalized switching frequency.

The AC output voltage magnitude in Fig. 5.4 can be found out from the diode rectifier output voltage v_R in the equivalent circuit shown in Fig. 5.3, transferred to transformer primary side. The output voltage V_{out} is the average value of the rectified output voltage v_R, filtered by the output filter $(L_f - C_f)$. Thus, the magnitude of AC voltages in Fig. 5.4 can be given as

$$|v_{AB,1}| = \frac{4}{\pi} V_{in} \sin\left(\frac{\alpha}{2}\right), \quad |v_{o,1}| = \frac{n\pi}{2} V_{out}. \tag{5.7}$$

For systems with constant DC voltage source, the DC output voltage can be found

using (5.5) and (5.7). The magnitude from (5.5) can be evaluated with $s = j\omega_s$ and is given as

$$\frac{|v_{AB,1}|}{|v_{o,1}|} = \frac{Q}{\sqrt{F^2 + Q^2\left(1 - F^2\right)^2}}. \tag{5.8}$$

Substituting (5.7) in (5.8), the DC output voltage can be obtained as

$$V_{out}|_{DC\_V_{in}} = \frac{8}{\pi^2}\frac{V_{in}}{n}\frac{Q\sin\left(\frac{\alpha}{2}\right)}{\sqrt{F^2 + Q^2\left(1 - F^2\right)^2}}. \tag{5.9}$$

However, for systems with DC current source, V_{in} is dependent on load and expression of V_{out} from (5.9) cannot be used as it is. The output voltage for such system is derived from the equivalent circuits shown in Fig. 5.3 and Fig. 5.4, as follows. The expression of input impedance (Z_{in}) of the loaded resonant tank can be derived from Fig. 5.4. The impedance(s) of individual tank components are given by

$$X_{Lr} = 2\pi f_s L_r = F Z_o, \qquad X_{Cr} = \frac{1}{2\pi f_s C_r} = \frac{Z_o}{F}. \tag{5.10}$$

Using 5.10, Z_{in} can be derived as

$$Z_{in} = \frac{Z_o}{1 + F^2Q^2}\left[Q + jF\left\{1 - Q^2\left(1 - F^2\right)\right\}\right]. \tag{5.11}$$

The AC active power from the source in Fig. 5.4 and the DC input and output power in Fig. 5.3 can be given as

$$P_{AC} = \frac{V_{AB,1,rms}^2}{|Z_{in}|}\cos\left(\phi_{in}\right), \quad P_{in} = V_{in}I_g, \quad P_{out} = \frac{V_{out}^2}{R_{load}}, \tag{5.12}$$

where $V_{AB,1,rms}$ is rms value of the fundamental component of inverter output voltage $v_{AB,1}$. With lossless power conversion, from (5.12), the input voltage can be expressed as

$$V_{in} = \frac{V_{out}^2}{I_g R_{load}}. \tag{5.13}$$

Equating the DC output power to the AC active power in (5.12) and using expressions from (5.7) and (5.13), the DC output voltage can be expressed as

$$V_{out} = \frac{Z_o I_g}{n \sin\left(\frac{\alpha}{2}\right)} \sqrt{\frac{Q}{\cos\left(\phi_{in}\right)} \frac{|Z_{in}|}{Z_o}}. \tag{5.14}$$

The DC output voltage expression from 5.14 can be normalized and expressed as

$$V_{out\_norm} = \sqrt{\frac{Q}{\cos\left(\phi_{in}\right)} |Z_{in\_norm}|}, \tag{5.15}$$

using a base voltage defined as

$$V_{base} = \frac{Z_o I_g}{n \sin\left(\frac{\alpha}{2}\right)}, \tag{5.16}$$

and the normalized input impedance (Z_{in_norm}) is defined as

$$Z_{in\_norm} = \frac{Z_{in}}{Z_o}. \tag{5.17}$$

The normalized output voltage from (5.15) is plotted against normalized switching frequency (F) and the result is shown for a range of load (Q) in Fig. 5.5.

As an alternate method, the DC output voltage can also be derived from 5.9, substituting V_{in} from 5.13 and is given as

$$V_{out\_Alt} = \frac{Z_o I_g}{n \sin\left(\frac{\alpha}{2}\right)} \sqrt{F^2 + Q^2 \left(1 - F^2\right)^2}. \tag{5.18}$$

which is normalized with the base voltage defined in 5.16 and the normalized expression is given by

$$V_{out\_norm\_Alt} = \sqrt{F^2 + Q^2 \left(1 - F^2\right)^2}. \tag{5.19}$$

For comparison, this normalized output voltage is plotted against normalized switching frequency (F) and the result is shown for a range of load (Q) in Fig. 5.6. It can be seen from the plots in Fig. 5.5 and Fig. 5.6, the expressions of DC output voltage from 5.14 and

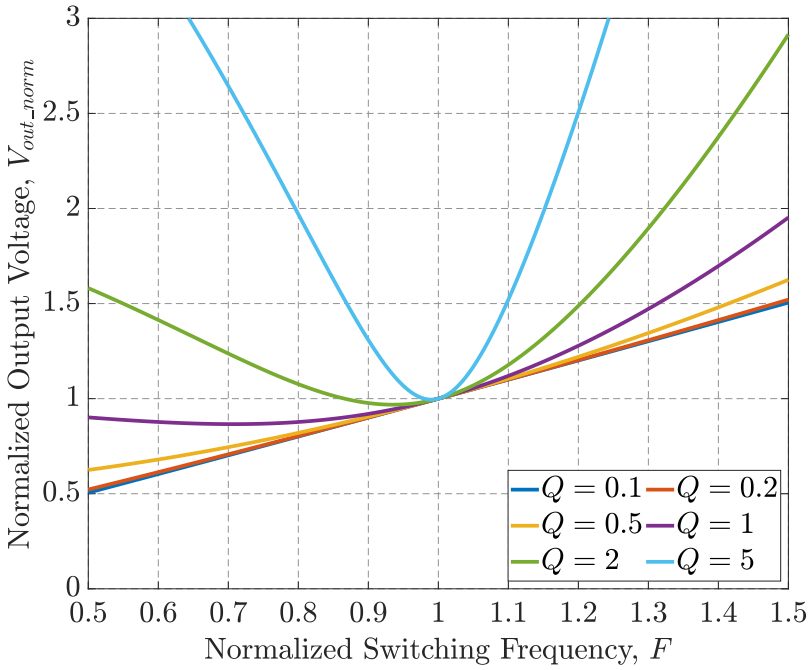


Fig. 5.5: Normalized output voltage v normalized switching frequency.

5.18 are equivalent and any one of them can be used for converter design which is discussed in the next section.

5.2 Design of Parallel Resonant Converter

Based on the derivations presented in the last section, the operating point and resonant tank elements are designed in this section. From the plot of normalized output voltage presented in Fig. 5.5, it can be observed that if the converter is operated at a switching frequency equal to its resonant frequency, *i.e.* at $F = 1$, the DC output voltage becomes independent of load and thus the output voltage from 5.14 can be expressed as

$$V_{out}|_{F=1} = \frac{Z_o I_g}{n \sin\left(\frac{\alpha}{2}\right)}. \tag{5.20}$$

The input impedance of the loaded resonant tank and power factor for the primary inverter at this operating point of $F = 1$ can be expressed as

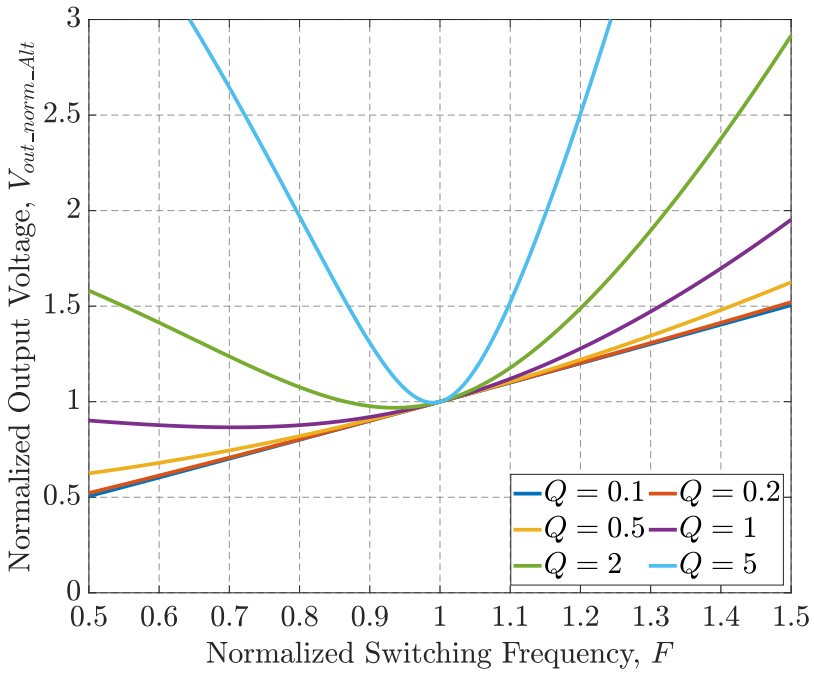


Fig. 5.6: Normalized output voltage v normalized switching frequency, from alternate expression presented in 5.19.

$$Z_{in}|_{F=1} = \frac{Z_o}{\sqrt{1+Q^2}} \angle \tan^{-1}\left(\frac{1}{Q}\right), \tag{5.21}$$

$$\cos\left(\phi_{in}\right)|_{F=1} = \frac{1}{\sqrt{1+\frac{1}{Q^2}}}. \tag{5.22}$$

From 5.21 and 5.22, it can be seen that for any load (Q), the primary inverter operates at a lagging power factor which can help the converter operate with ZVS and as the load decreases (Q increases), the inverter power factor increases and approaches unity at no load ($Q \to \infty$). Substituting 5.20 in 5.13, the input DC voltage of the converter can be derived as

$$V_{in}|_{F=1} = \frac{Z_o^2 I_g}{n^2 \sin^2\left(\frac{\alpha}{2}\right) R_{load}}. \tag{5.23}$$

5.2.1 Design of Resonant Tank Elements

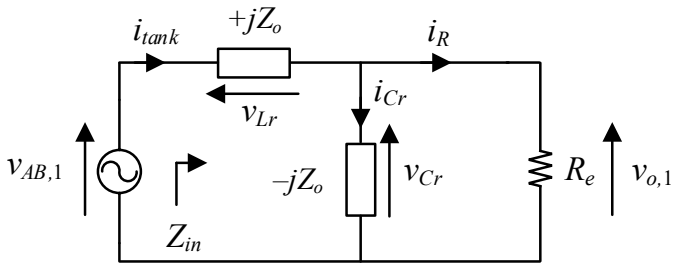


Fig. 5.7: AC equivalent circuit of the loaded parallel resonant converter operating at resonance ($F = 1$).

The design of the converter starts from the output voltage expression from 5.20, where V_{out} and I_g are given and Z_o, n and α are to be designed. The value of steady state control angle (α) is selected to be 120^o which produces lowest harmonic content at the primary inverter output without any triplen harmonics [60]. This also provides sufficient margin from the maximum possible control angle of 180^o to support transient response.

The voltage across resonant capacitor can be derived from the rectifier in the circuits shown in Fig. 5.1 and Fig. 5.3 and its rms value is given in terms of DC output voltage as

$$V'_{Cr\_rms} = \frac{\pi}{2\sqrt{2}} V_{out}, \quad V_{Cr\_rms} = \frac{n\pi}{2\sqrt{2}} V_{out}. \tag{5.24}$$

The equivalent circuit from Fig. 5.4 can be simplified at the operating point of $F = 1$ and is redrawn in Fig. 5.7. The rms current in tank inductor can be derived from this AC equivalent circuit in Fig. 5.7 and using the magnitude of Z_{in} from (5.21), which is given as

$$I_{tank\_rms} = \frac{V_{AB,1,rms}}{|Z_{in}|} = \frac{2\sqrt{2}}{\pi} \frac{V_{in}}{Z_o} \sin\left(\frac{\alpha}{2}\right) \sqrt{1+Q^2}. \tag{5.25}$$

Substituting V_{in} from (5.23) into (5.25) the expression of inductor rms current is given as

$$I_{tank\_rms} = \frac{\pi}{2\sqrt{2}} \frac{I_g}{\sin\left(\frac{\alpha}{2}\right)} \sqrt{1+\frac{1}{Q^2}}. \tag{5.26}$$

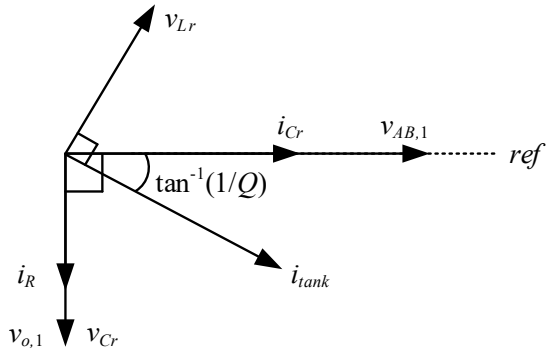


Fig. 5.8: Phasor diagram of the tank signals.

With the phase information from Z_{in} from (5.21), the tank current can be expressed as

$$i_{tank}(t) = \frac{\pi}{2}\frac{I_g}{\sin\left(\frac{\alpha}{2}\right)}\sqrt{1+\frac{1}{Q^2}}\cos\left(\omega_s t - \tan^{-1}\left(\frac{1}{Q}\right)\right). \tag{5.27}$$

From the circuit in Fig. 5.7, the current through and voltage across the resonant capacitor can be derived as

$$i_{Cr} = i_{tank}\frac{R_e}{R_e - jZ_o}, \qquad v_{Cr} = i_{tank}\frac{R_e(-jZ_o)}{R_e - jZ_o}. \tag{5.28}$$

Using the expression of $i_{tank}(t)$ from (5.27), and magnitude of capacitor voltage from (5.24), $i_{Cr}(t)$ and $v_{Cr}(t)$ can be written as

$$i_{Cr}(t) = \frac{\pi}{2}\frac{I_g}{\sin\left(\frac{\alpha}{2}\right)}\cos(\omega_s t), \qquad v_{Cr}(t) = \frac{n\pi}{2}V_{out}\cos\left(\omega_s t - \frac{\pi}{2}\right). \tag{5.29}$$

The phasor diagram for the tank signals is drawn in Fig. 5.8 using (5.27) and (5.29), with fundamental component of primary inverter output voltage as reference.

The Volt-Ampere (VA) for the inductor (S_{Lr}) and the capacitor (S_{Cr}) can be calculated from the rms current in the inductor (5.26) and rms voltage across the capacitor (5.24) as

$$S_{Lr} = I_{tank\_rms}^2 Z_o = \frac{\pi^2}{8}\frac{I_g^2 Z_o}{\sin^2\left(\frac{\alpha}{2}\right)}\left(1+\frac{1}{Q^2}\right), \tag{5.30}$$

$$S_{Cr} = \frac{V_{Cr\_rms}^2}{Z_o} = \frac{\pi^2}{8} \frac{I_g^2 Z_o}{\sin^2\left(\frac{\alpha}{2}\right)}. \tag{5.31}$$

Using the output voltage expression from (5.20) in the output power equation in (5.12), the output power (P_{out}) can be expressed as

$$P_{out} = \frac{\pi^2}{8} \frac{I_g^2 Z_o}{\sin^2\left(\frac{\alpha}{2}\right)} \frac{1}{Q}. \tag{5.32}$$

Using 5.32 in (5.30) and (5.31) the VA for the tank components can be given as

$$S_{Lr} = \left(Q + \frac{1}{Q}\right) P_{out}, \quad S_{Cr} = Q P_{out}. \tag{5.33}$$

Using (5.33), VA rating for the tank components can be found at maximum output power *i.e.*, by using $P_{out} = P_{out\_max}$. The normalized VA rating of the tank components, normalized with P_{out_max} can be calculated from (5.33) and is given as

$$S_{Lr\_norm} = \left(Q + \frac{1}{Q}\right), \quad S_{Cr\_norm} = Q. \tag{5.34}$$

The total VA rating of the tank, which is summation of the VA rating for tank inductor and capacitor, is given in normalized form from (5.34) as

$$S_{tank\_norm} = \left(2Q + \frac{1}{Q}\right). \tag{5.35}$$

From (5.35), the minimum value of S_{tank_norm} can be found out through its first and second derivative test *i.e.*

$$\frac{d}{dQ}\left(S_{tank\_norm}\right) = 0 \Rightarrow Q = \frac{1}{\sqrt{2}}, \tag{5.36}$$

$$\frac{d^2}{dQ^2}\left(S_{tank\_norm}\right)\Big|_{Q=\frac{1}{\sqrt{2}}} = 4\sqrt{2} > 0. \tag{5.37}$$

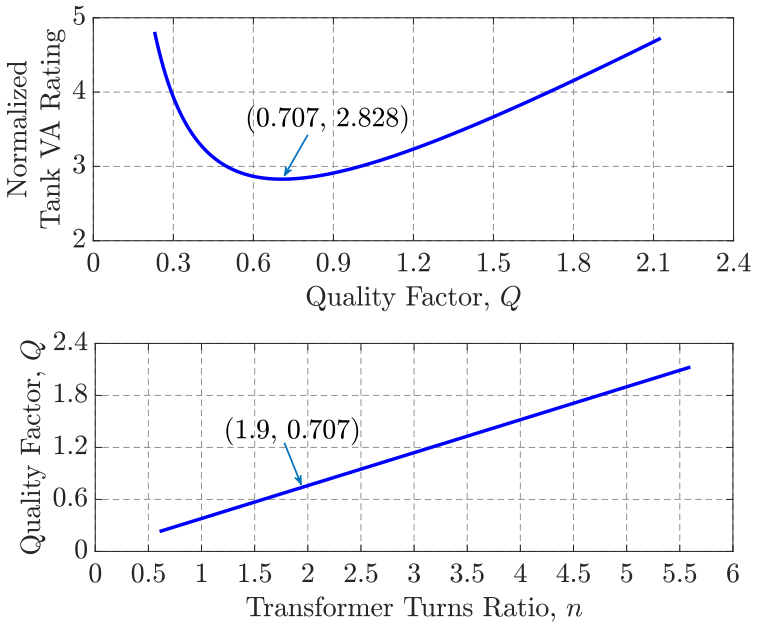


Fig. 5.9: Normalized VA rating of the tank versus quality factor of the loaded tank (top) and quality factor of the loaded tank versus transformer turns ratio (bottom).

which means that the tank VA will be minimum when full load quality factor of the loaded tank is $1/\sqrt{2}$ and its minimum value is given as

$$S_{tank\_norm\_min} = 2\sqrt{2}. \tag{5.38}$$

The normalized tank VA rating is plotted with respect to loaded quality factor of the tank that is shown by the top plot pane in Fig. 5.9, where the minimum value is pointed. In Fig. 5.9, the transformer turns ratio versus the loaded quality factor is plotted in the bottom plot pane where the values corresponding to minimum tank VA rating is pointed.

Since the energy density of a capacitor is a few orders of magnitude higher than that of an inductor, it is possible to reduce the size of the converter by designing the converter with minimum VA rating for the tank inductor. The normalized VA rating for the tank inductor and tank capacitor are plotted for different transformer turn ratio in Fig. 5.10. From the inductor VA in (5.34), it can be seen that its minimum value is 2 which occurs at $Q = 1$, as can be seen from the plot of S_{Lr_norm} in Fig. 5.10. And the corresponding transformer turns ratio (n) is 2.63 which is pointed in the top plot pane in Fig. 5.10.

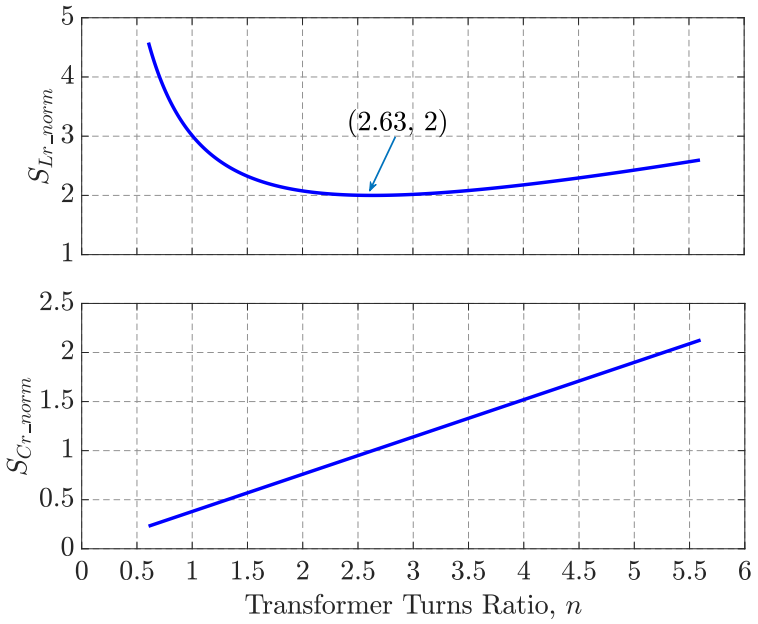


Fig. 5.10: Normalized VA for inductor (top) and normalized VA for capacitor (bottom) versus the transformer turn ratio.

From the VA rating expression of tank inductor in (5.30), with sinusoidal current in the inductor, S_{Lr} can be re-written as

$$S_{Lr} = I_{tank\_rms}^2 Z_o = \sqrt{2}\omega_o I_{tank\_rms} I_{tank\_pk} L_r, \tag{5.39}$$

where I_{tank_pk} is the peak AC current in the inductor. With fixed frequency operation, S_{Lr} from 5.39 can be seen as proportional to the product of inductance and its rms and peak current *i.e.*

$$S_{Lr} \propto L_r I_{tank\_rms} I_{tank\_pk}. \tag{5.40}$$

For an inductor, the conduction loss depends on its rms current, and the core loss depends on its maximum current, which determines the flux swing in the core material for alternating current excitation. The relationship between inductor peak current and its peak flux density (B_{pk}) within the core material can be given as

$$L_r I_{tank\_pk} = N_{Lr} B_{pk} A_c, \tag{5.41}$$

where N_{Lr} in the number of turns in the inductor and A_c is the cross sectional area of the magnetic core used. The total winding area (W_A) and core window area (A_w) can be given as

$$W_A = N_{Lr} \frac{I_{tank\_rms}}{J} \quad \Rightarrow \quad A_w = K_w W_A = K_w N_{Lr} \frac{I_{tank\_rms}}{J}, \tag{5.42}$$

where J is the current density of the conductor used in construction of L_r and K_w is the window fill factor. From (5.41) and (5.42), the area product for the inductor can be derived as

$$AP = A_c A_w = K_w \frac{L_r I_{tank\_pk} I_{tank\_rms}}{B_{pk} J}. \tag{5.43}$$

For a given core material, the core loss density depends on B_{pk}, at a given frequency of operation. Therefore, with a fixed core loss density, B_{pk} also becomes fixed. Similarly, for a given conductor material, conduction loss is proportional to the current density, J. Therefore, for a fixed conduction loss density, J becomes fixed. Thus, for a given loss density in the inductor with a given window utilization factor (K_w), the area product from (5.43) becomes proportional to the inductance and its rms and peak current and using (5.40) this relationship can be written as

$$AP \ \propto \ L_r I_{tank\_pk} I_{tank\_rms} \ \propto \ S_{Lr}. \tag{5.44}$$

For a given core geometry (*e.g.*, EE, ETD, PQ etc.), the inductor volume (V_L) is proportional to its area product raised to the power of three-fourth [103, 104], expressed as

$$V_L \ \propto \ (AP)^{\frac{3}{4}} \ \propto \ (S_{Lr})^{\frac{3}{4}}, \tag{5.45}$$

which means that inductor size will be lower with lower VA rating, with a given core and copper loss density.

From the plots of Fig. 5.9 and Fig. 5.10, the design can be established around minimum VA for the total tank or the inductor. However, from the Q v n plot in Fig. 5.9, it can be observed that the quality factor for such design(s) is low which may lead to discontinuous operation of the diode rectifier. To design the converter with higher Q, n needs to be higher. From the plot of S_{Lr_norm} in Fig. 5.10, it can be seen that S_{Lr_norm} is relatively flat over the range of $n = 2$ to $n = 4$, which means the tank can be designed with higher transformer turns ratio (or Q) without significant increase in inductor VA rating. Thus, with a trade-off between Q and inductor VA rating, finally the transformer turns ratio is selected to be $n = 4$ where $S_{Lr\_norm} = 2.18$ and $Q = 1.52$.

The rms voltage across capacitor (V_{Cr_rms}) from (5.24) is normalized with base voltage defined in (5.16) and the rms current in the inductor (I_{tank_rms}) from (5.26) is normalized with a base value defined as

$$I_{base} = \frac{V_{base}}{Z_o} = \frac{I_g}{n \sin\left(\frac{\alpha}{2}\right)}. \tag{5.46}$$

Thus, the normalized tank signals can be expressed as

$$I_{tank\_rms\_norm} = \frac{I_{tank\_rms}}{I_{base}} = \frac{n\pi}{2\sqrt{2}}\sqrt{1 + \frac{1}{Q^2}}, \tag{5.47}$$

$$V_{Cr\_rms\_norm} = \frac{V_{Cr\_rms}}{V_{base}} = \frac{n\pi}{2\sqrt{2}}. \tag{5.48}$$

The normalized rms tank inductor current ($I_{tank\_rms\_norm}$) and rms capacitor voltage ($V_{Cr\_rms\_norm}$) are plotted with respect to transformer turns ratio in Fig. 5.11, at the top and bottom plot panes, respectively. From the circuits shown in Fig. 5.1 and Fig. 5.3 the resonant capacitor voltage is constant, when normalized with a base voltage that is equal to DC output voltage. However, the normalized capacitor voltage plotted here in Fig. 5.11 is on the transformer primary side and hence it increases linearly with n.

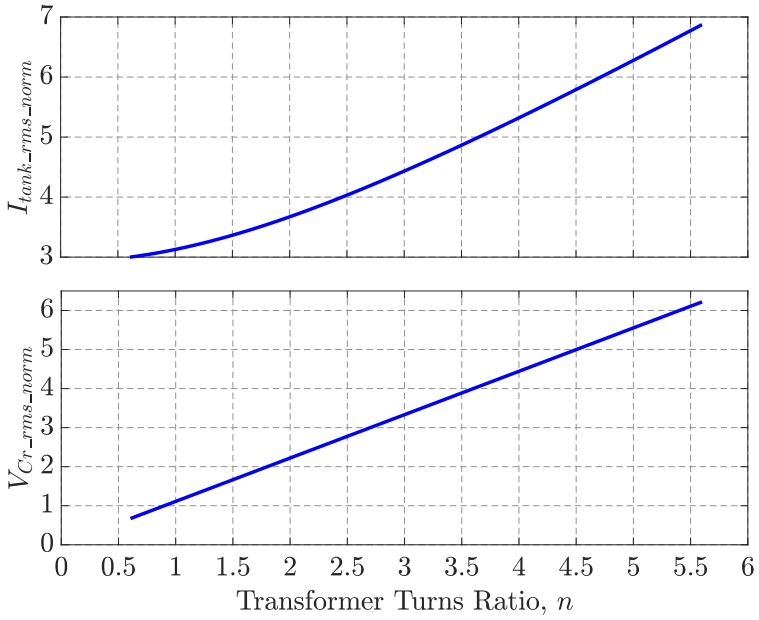


Fig. 5.11: Normalized resonant inductor rms current (top) and normalized capacitor rms voltage (bottom) versus the transformer turn ratio.

After selecting the transformer turns ratio (n), the tank characteristic impedance (Z_o) can be determined from (5.20) and is given as

$$Z_o = \frac{nV_{out}\sin\left(\frac{\alpha}{2}\right)}{I_g}, \tag{5.49}$$

and the resonant inductor and capacitor values can be calculated from (5.49), using (5.6) as

$$L_r = \frac{Z_o}{2\pi f_o} = \frac{Z_o}{2\pi f_s}, \tag{5.50}$$

$$C_r = \frac{1}{2\pi f_o Z_o} = \frac{1}{2\pi f_s Z_o} \quad \Rightarrow \quad C_r' = \frac{n^2}{2\pi f_s Z_o}. \tag{5.51}$$

The rating of the tank elements can be determined from the charts in Fig. 5.11, multiplying with their corresponding base values defined in (5.46) and (5.16).

5.2.2 Device Selection

The primary side inverter devices block voltage equal to input DC voltage (V_{in}) whose maximum value is decided based on the maximum load and efficiency (η) of the converter and can be found out by

$$V_{pri\_FET} \geq \frac{P_{out\_max}}{\eta I_g}, \tag{5.52}$$

and the rms current rating for the primary MOSFETs ($Q_1 - Q_4$) are determined by the tank inductor current which can be found out from (5.25). On the other hand, the secondary side rectifier devices see a reverse voltage equal to the peak value of voltage across resonant capacitor (C_r') and thus the voltage rating for the rectifier is given by

$$V_{sec\_rect} \geq \frac{\pi V_{out}}{2}. \tag{5.53}$$

The average value of current through the output rectifier is equal to the load current (I_{load}) which can be found out by dividing maximum load power (P_{out_max}) by DC output voltage (V_{out}).

5.2.3 Modulation for Control

It is established earlier that the PRC behaves as a natural voltage source at its output when operated at switching frequency equal to the resonant frequency and hence a control scheme that varies the switching frequency to regulate its output cannot be employed here. It can be seen from (5.20) that for the designed converter, the output voltage can be controlled by the phase shift angle (α) and hence phase shift modulation strategy is used here.

5.2.4 ZVS Realization

With fixed frequency, phase shift modulation, switches in the lagging leg (leg B) achieves zero voltage switching (ZVS) by the tank current itself, but the leading leg (leg A) may not have ZVS, depending on operating point. From the expression of input impedance

in (5.21), it can be seen that the tank current (i_{tank}) in PRC lags the fundamental component of inverter output voltage and this angle of lagging increases with the load. If the tank impedance angle is high enough so that at the instant of rising edge of v_{AB}, value of tank current is negative, switches in the leg A may have ZVS by the tank current itself. This condition can be expressed as

$$\tan^{-1}(Q) < \frac{\alpha}{2}. \tag{5.54}$$

The condition for ZVS mentioned in (5.54) is only the necessary condition, the actual ZVS occurrence is dependent on the parasitc capacitance of the switches. From (5.54), it can be seen that load range for which ZVS for leg A switches can be achieved by tank current, will be wide if α is high, as close to 180° as possible. But, operating with higher α limits the minimum output voltage and power capability, under transient conditions as well as due to tolerance on resonant tank components [81]. A value of 120° for α is a good trade-off for design considering ZVS range as well as transient and component tolerances, in addition to aforementioned low harmonic content in inverter output voltage. The range of load for which ZVS can be achieved is shown by the plot in Fig. 5.12. In Fig. 5.12, the blue line shows the angle $\tan^{-1}(Q)$ and the red and black lines show the $\frac{\alpha}{2}$ boundaries for $\alpha = 120°$ and $\alpha = 180°$ operating points, respectively. According to the condition established in (5.54), the ZVS load range for $\alpha = 120°$ operating condition is to the right of the dotted red line in the Fig. 5.12, whereas, for $\alpha = 180°$, ZVS happens for the entire load range.

To ensure ZVS for leg A switches for the entire load range, an ZVS assisting circuit needs to be augmented to the converter leg A. Since the input DC voltage varies over wide values, proportional to load, an active ZVS assisting circuit presented in section 3.2.1, consisting of an auxiliary half bridge leg (leg Z) and ZVS assisting inductor (L_{zvs}) is used here to achieve ZVS turn on of the MOSFETs in leg A [102]. The ZVS assisting circuit is shown in Fig. 5.13 with a capacitor (C_{zvs}) in series with the inductor L_{zvs}, as presented in chapter 3. The purpose of C_{zvs} is to block any DC component in voltage v_{AZ}, arising

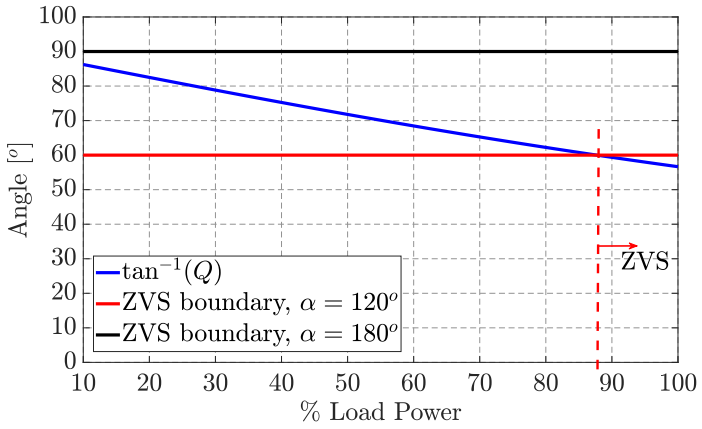


Fig. 5.12: ZVS load range for the converter at different operating point (α).

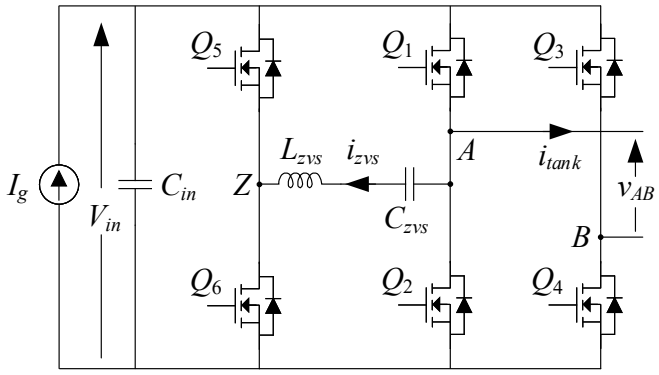


Fig. 5.13: The ZVS assisting circuit used in the converter.

due to any component mismatch between leg A and leg Z. The amount of ZVS assistance is controlled by controlling the phase shift angle between leg A and this auxiliary leg, over the load range.

5.2.5 Output Filter

The output filter components (L_f and C_f) are designed based on current ripple allowance through L_f and voltage ripple on C_f. With reference to Fig. 5.1 and Fig. 5.3, the rectifier output voltage (v_R) waveform is shown in Fig. 5.14.

Assuming the ripple content in output voltage to be very small, left side of L_f sees rectified sinusoidal voltage v_R and right side sees DC voltage V_{out} and the volt-sec product across L_f is calculated from the area indicated by A_f, hash-marked in Fig. 5.14. Thus, with

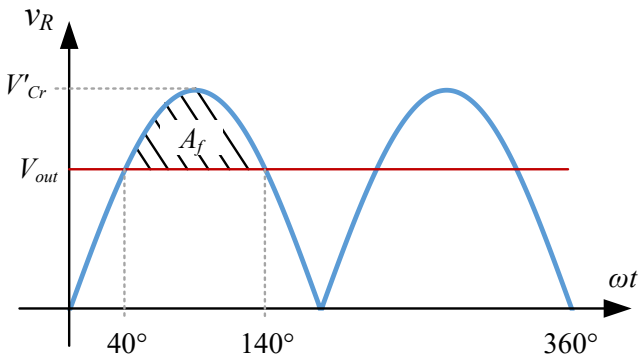


Fig. 5.14: Waveforms on the output rectifier side of the PRC.

a given inductor current ripple (Δi_{Lf}), L_f is calculated by

$$L_f = \frac{A_f}{2\Delta i_{Lf}}. \tag{5.55}$$

For calculating the output capacitor value, the current in the filter inductor L_f is approximated to be DC value equal to load current (I_{load}) plus a twice the switching frequency ($2f_s$) sinusoidal ripple of amplitude Δi_{Lf}. This sinusoidal ripple current is filtered by the output capacitor. So, by calculating the charge going into the capacitor in half of the ripple cycle, we can calculate the capacitance required for an allowable output voltage ripple (ΔV_{out}), which is given as

$$C_f = \frac{\Delta i_{Lf}}{4\pi f_s \Delta V_{out}}. \tag{5.56}$$

5.3 Experimental Results

A prototype PRC operating at 250 kHz has been developed with the parameters shown in Table 5.1, following the design method presented earlier in this chapter. The hardware setup of the PRC is shown in Fig. 5.15 which operates from a 1 A DC current source and is tested for a power level up to 450 W. The converter has been tested for its output voltage characteristics in steady state and transient conditions to verify its load independent, constant output voltage characteristics.

Table 5.1: Details of the parallel resonant converter

Component / Parameter	Part Number / Value
I_g [A]	1
V_{out} [V]	120
f_s [kHz]	250
P_{out} [W]	50 – 450
L_r [µH]	264.6
C'_r [nF]	24.5
n	4
$Q_1 - Q_6$	C2M1000170D (2 in parallel)
$D_1 - D_4$	GHXS020A060S-D1
L_f [µH]	80
C_f [µF]	2.35
L_{zvs} [µH]	55

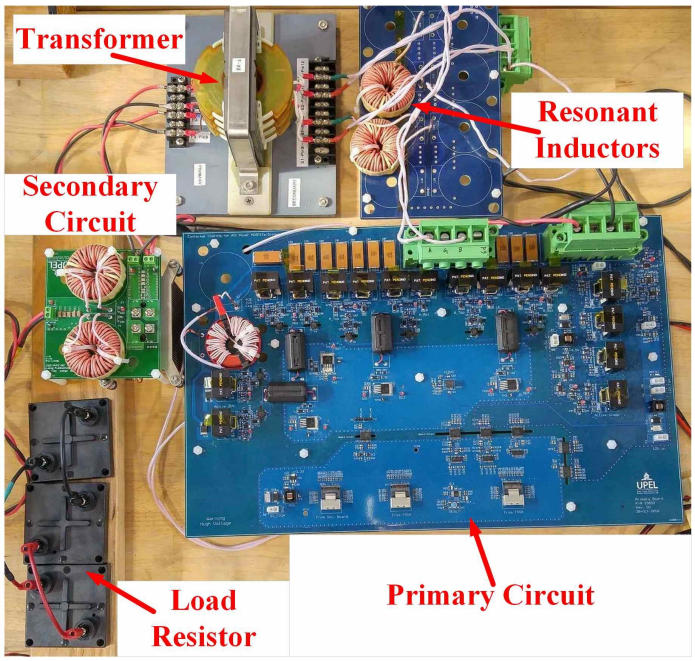
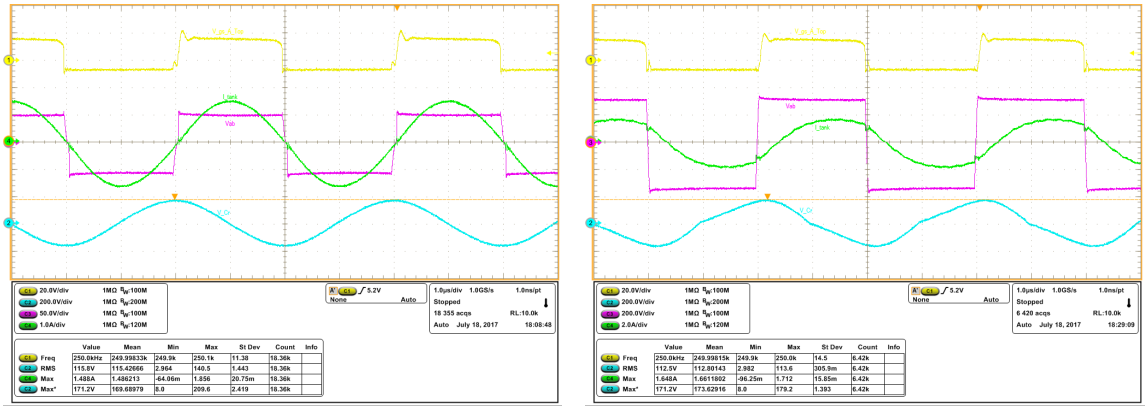


Fig. 5.15: Photograph of the test setup.

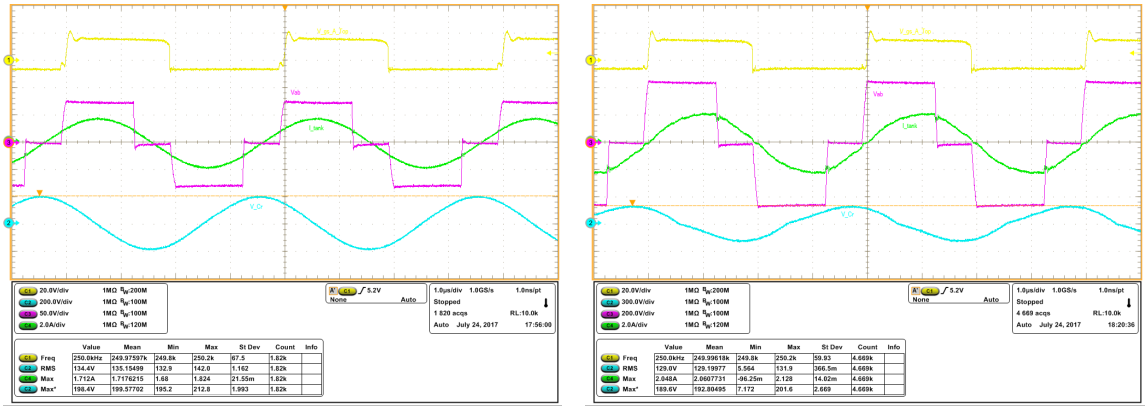


(a) (b)

Fig. 5.16: Steady state operating waveforms of PRC with $\alpha = 180°$, at (a) $R_{load} = 295\,\Omega$ and (b) at $R_{load} = 34\,\Omega$. CH1 (yellow): v_{GS_Q1}, CH2 (cyan): $-v'_{Cr}$, CH3 (purple): v_{AB}, CH4 (green): i_{tank}.

Hardware test results of the PRC during steady state operation are shown in Fig. 5.16 and Fig. 5.17. The waveforms shown in Fig. 5.16 and Fig. 5.17 are operation with $\alpha = 180°$ and $\alpha = 120°$, respectively, for $R_{load} = 295\,\Omega$ and $R_{load} = 34\,\Omega$ which corresponds to minimum and maximum load at $V_{out} = 120\,\text{V}$. In these oscilloscope captures, yellow trace (CH1) is for the gate to source voltage of top MOSFET in leg A (v_{GS_Q1}), purple (CH3) is the primary side inverter output voltage (v_{AB}), green waveform (CH4) is the current in the resonant inductor (i_{tank}) and cyan trace (CH2) is the voltage across the resonant capacitor (v'_{Cr}) placed on the secondary side of the transformer. The captured waveform of v'_{Cr} in Fig. 5.16 and Fig. 5.17 are of reverse polarity, compared to the notation used in the circuits used in analysis and that is why it appears to be 90° leading to v_{AB} as opposed to 90° lagging as established in (5.29) and in Fig. 5.8. For $\alpha = 180°$, no ZVS assisting circuit is employed, whereas, for $\alpha = 120°$, the active ZVS assisting circuit has been used as presented in Fig. 5.13 and the ZVS assisting current is adjusted so that the MOSFETs in the primary side bridge achieve ZVS.

The output characteristics of the converter is determined by testing the converter over wide range of load resistance (R_{load}), at two different control angle *viz.* minimum power operation angle ($\alpha = 180°$) and designed operating angle ($\alpha = 120°$). Figure 5.18 shows



(a) (b)

Fig. 5.17: Steady state operating waveforms of PRC with $\alpha = 120°$, at (a) $R_{load} = 295\,\Omega$ and (b) at $R_{load} = 34\,\Omega$. CH1 (yellow): v_{GS_Q1}, CH2 (cyan): $-v'_{Cr}$, CH3 (purple): v_{AB}, CH4 (green): i_{tank}.

the steady state DC output voltage (V_{out}) of the converter with respect to variation in R_{load}. In Fig. 5.18, the blue plot shows V_{out} vs R_{load} for $\alpha = 180°$ and the red plot is for $\alpha = 120°$. It can be seen from the plots in Fig. 5.18, that the output voltage remains almost constant over the range of R_{load}. This shows that the converter operates as a natural voltage source at the output with a constant input current source and variable (with load) input voltage. The small droop in the output voltage are due to series nonidealities *e.g.* ESR present in the circuit that can be easily taken care of by the closed loop controller with small variation in control angle α.

The PRC has also been tested for transient load conditions and the result is presented in Fig. 5.19. For this test, the output load current of the converter is changed from 1.7 A ($\approx$ 200 W) to 2.3 A ($\approx$ 275 W) and back to 1.7 A while the PRC has been operating in open loop with a fixed phase shift angle of $\alpha = 120°$. In Fig. 5.19, the cyan (CH2) shows the DC input voltage (V_{in}), the green waveform (CH4) is the output load current (I_{load}) and the DC output voltage (V_{out}) is shown by purple trace (CH3). It can be observed from this result that the output voltage goes through overshoot or undershoot under load change transients, but settles back to its designed value of 120 V, conforming to the load independent constant output voltage characteristics.

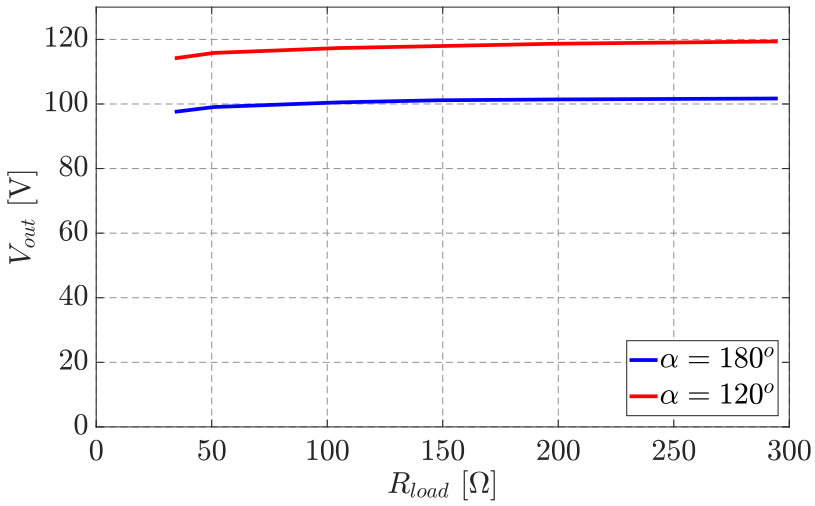


Fig. 5.18: Open loop output characteristics of PRC. Experimental V_{out} v R_{load} at $\alpha = 180°$ (blue) and $\alpha = 120°$ (red).

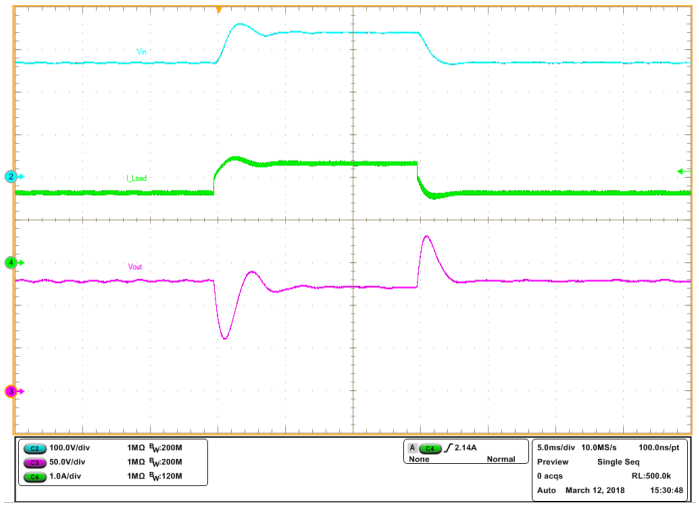


Fig. 5.19: Input and output DC signals under open loop load transient of 1.7 A (≈ 200 W) to 2.3 A (≈ 275 W) and back to 1.7 A, for the PRC operating with fixed control angle of $\alpha = 120°$. CH2 (cyan): V_{in}, CH4 (green): I_{load} and CH3 (purple): V_{out}.

5.4 PRC for Wide Voltage Output

The load independent constant output voltage characteristics of an PRC can be leveraged for designing converters requiring output voltage regulation over wide range. From the DC output voltage expression in (5.20), the output voltage can be controlled by α. However, when the desired output voltage range becomes wide, controlling V_{out} through α will result in small values of α for high values of V_{out}. This will increase the stress on resonant inductor (5.26) significantly. In addition, it will be challenging to select proper semiconductor devices which can operate efficiently at high voltage low current as well as low voltage high current. In view of these challenges, the output voltage range from the converter is split among multiple modules incorporating a multi-winding transformer and switch network that together minimize component stress and improve efficiency over the wide range of required operating conditions. A generic block diagram of such system is shown in Fig. 5.20. It should be noted that purpose of having wide voltage range at the output is to use same converter for variety of underwater sensor units which need voltage source of different magnitudes. This means that the output voltage of the converter is not needed to change while it is operational; the voltage is set for a particular unit on the seabed and the job of the converter is to regulate its output voltage over the range of load demanded by this unit. In Fig. 5.20, the primary inverter and resonant inductor on the transformer primary side are always active and processing the power. The transformer has one primary and m secondary windings one of which is selected by the changeover switch network, depending on the output voltage requirement. This selection in turn changes the effective turns ratio of the transformer and thus utilizes both n (in discrete steps) and α to control the output voltage with relatively smaller range of α. There are k numbers of rectifiers following the changeover switches which are optimized for the range of output voltage (and current) they are intended to work with.

An example converter realization based on the diagram presented in Fig. 5.20 is shown in Fig. 5.21 with $m = 4$ and $k = 2$. In Fig. 5.21, MOSFETs Q_{15} through Q_{22} work as a four-quadrant on/off switch for selection of the appropriate transformer secondary wind-

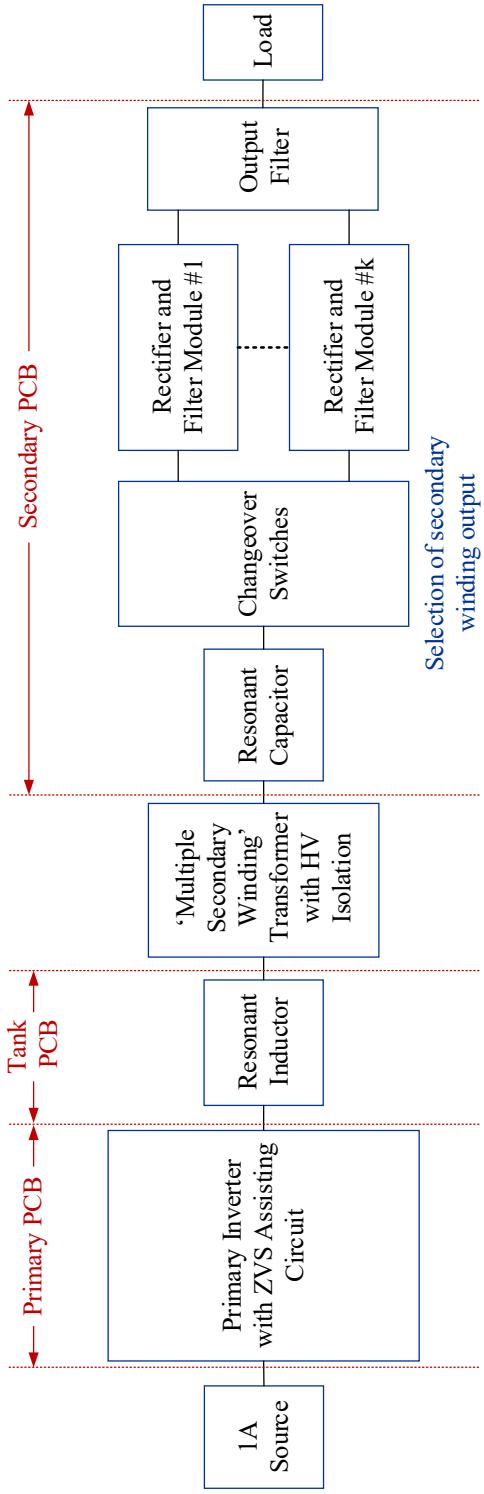


Fig. 5.20: Block diagram of the converter for wide range output.

Table 5.2: Operation modes of the PRC based wide output range converter

Mode of operation	Active switches in switch network	Active transformer windings	Output voltage range
$n1$	Q_{21}, Q_{22}	P, S_1, S_4	$V_{out\_min} - rV_{out\_min}$
$n2$	Q_{19}, Q_{20}	P, S_2, S_4	$rV_{out\_min} - r^2V_{out\_min}$
$n3$	Q_{17}, Q_{18}	P, S_3, S_4	$r^2V_{out\_min} - r^3V_{out\_min}$
$n4$	Q_{15}, Q_{16}	P, S_4	$r^3V_{out\_min} - V_{out\_max}$

ing in action and MOSFETs Q_7 through Q_{14} work as synchronous rectifier for improved conduction loss. On the primary side, the capacitor (C_{DC}) in series with resonant inductor (L_r) serves as a DC blocking capacitor to avoid transformer saturation due to any DC component coming out of inverter because of component mismatch. The transformer secondary windings are designed with turns ratio given by

$$n_1 : n_2 : n_3 : \cdots : n_m = r^0 : r^1 : r^2 : \cdots : r^{m-1}, \tag{5.57}$$

where the term r is defined as

$$r = \left(\frac{V_{out\_max}}{V_{out\_min}}\right)^{\frac{1}{m}}, \tag{5.58}$$

where V_{out_max} and V_{out_min} are the maximum and minimum DC output voltage of the converter, respectively. Based on this range of output voltage, the operating modes of the converter are listed in Table 5.2. The resonant capacitor is connected to the secondary winding S_4, however, this capacitor can be distributed among the secondary windings such that the total reflected capacitance in equivalent. The resonant capacitor being on the S_4 winding, it is operational for all the operating modes whereas, other three windings are active depending on the mode of operation based on output voltage requirement.

The design of this multi-winding PRC is carried out following the same method used in single output PRC. The design is optimized considering secondary winding S_4 in action with output voltage $r^3V_{out\_min}$ at $\alpha = 120°$ and the other transformer windings ratio are calculated using (5.57).

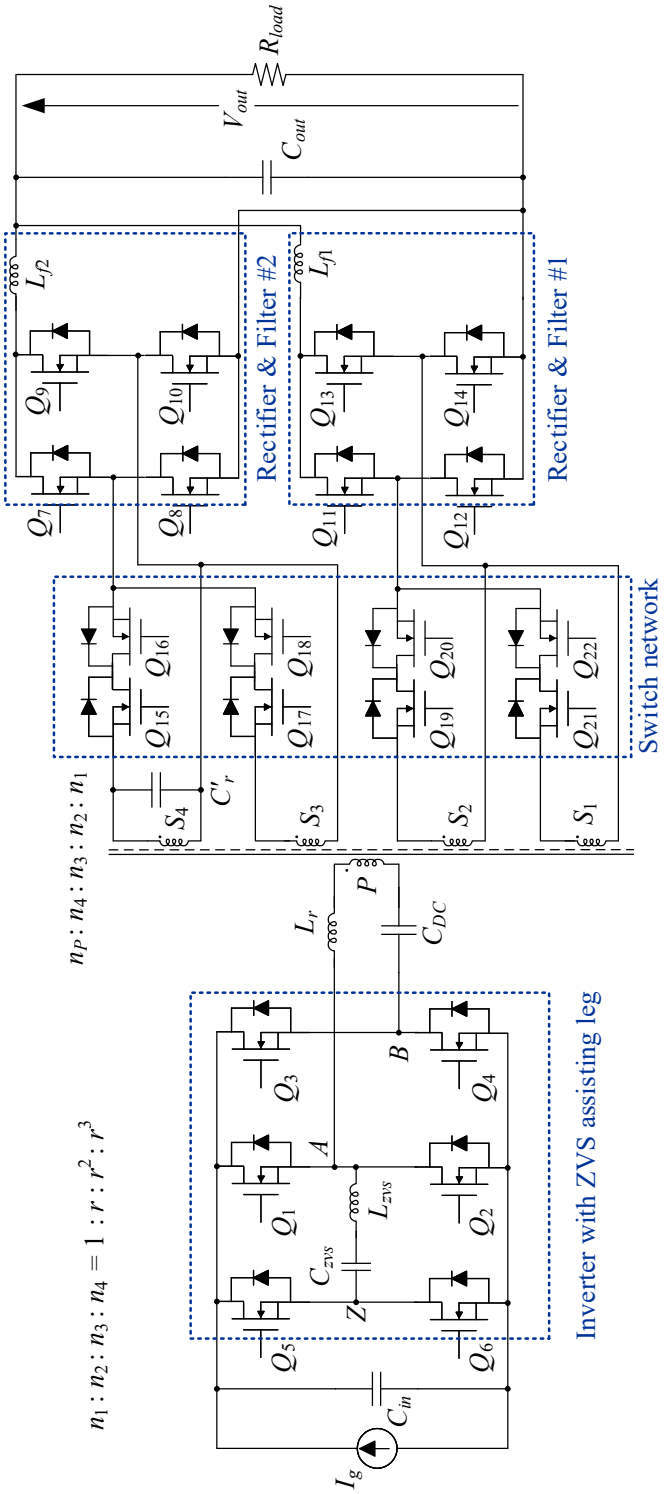


Fig. 5.21: Hardware architecture of the converter for wide range output.

Table 5.3: Details of the PRC based wide output range converter

Component / Parameter	Part Number / Value
I_g [A]	1
V_{out} [V]	24 – 250
f_s [kHz]	250
P_{out} [W]	50 – 1000
L_r [µH]	423.4
C'_r [nF]	23.5
C_{DC} [µF]	0.2
$n_P : n_1 : n_2 : n_3 : n_4$	$16 : 0.56 : 1 : 1.8 : 3.23$
$Q_1 - Q_6$	C2M1000170D (2 in parallel)
$Q_7 - Q_{10},\ Q_{15} - Q_{18}$	SCT3030ALGC11
$Q_{11} - Q_{14},\ Q_{19} - Q_{22}$	IXFX240N25X3
L_{f1} [µH]	10
L_{f2} [µH]	94
C_{out} [µF]	2.4
L_{zvs} [µH]	80
C_{zvs} [µF]	0.2

5.4.1 Simulation Results

The converter is designed for an output voltage range of 24 V to 250 V for operation up to 1 kW at any output voltage setting. The converter is simulated in MATLAB/PLECS with the parameters tabulated in Table 5.3. The simulation results are shown in Fig. 5.22 through Fig. 5.24 for operation at full load (1 kW), where the blue plot corresponds to operation in mode $n1$, red plot is for operation in mode $n2$, black plot is for operation in mode $n4$ and magenta plot is for mode $n4$.

In Fig. 5.22, the output voltage is plotted against α ranging from 180° to 60° for each mode of operation from each secondary winding of the transformer, where the solid line represents the analytical result from (5.20) and simulation results are shown by dots of corresponding color. From this plot, a range of $\alpha_{max} \approx 130°$ to $\alpha_{min} \approx 60°$ is selected to get a range of

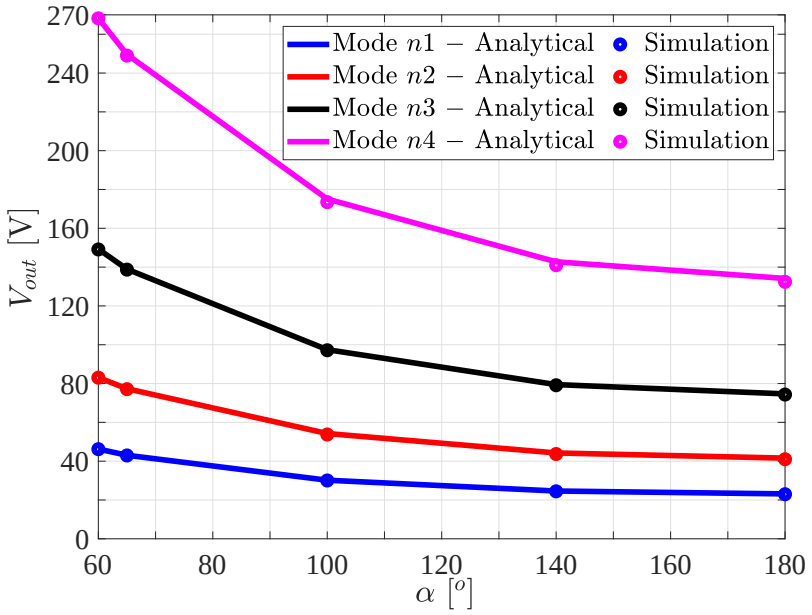


Fig. 5.22: Output voltage (V_{out}) of the converter with varying phase shift angle α, operating at full power in different modes of operation ($n1 - n4$). Solid lines are plots from analytical expression and dots correspond to the result obtained from simulation.

$$r = \frac{\sin\left(\frac{\alpha_{max}}{2}\right)}{\sin\left(\frac{\alpha_{min}}{2}\right)}, \tag{5.59}$$

which gives the required output voltage range (5.58) out of transformer secondary winding(s).

The peak current in the resonant inductor and peak voltage across the resonant capacitor, under full load operation across the different modes, are plotted in Fig. 5.23 and Fig. 5.24, respectively, against the range of output voltage. It can be seen from these results that for the entire range of operation, the stress in the resonant tank components are limited, owing to the advantage of operating in different modes using multi winding transformer.

5.4.2 Experimental Results

A hardware prototype has been built with two secondary windings on the transformer secondary and one rectifier and filter block to validate the design based on the parameters

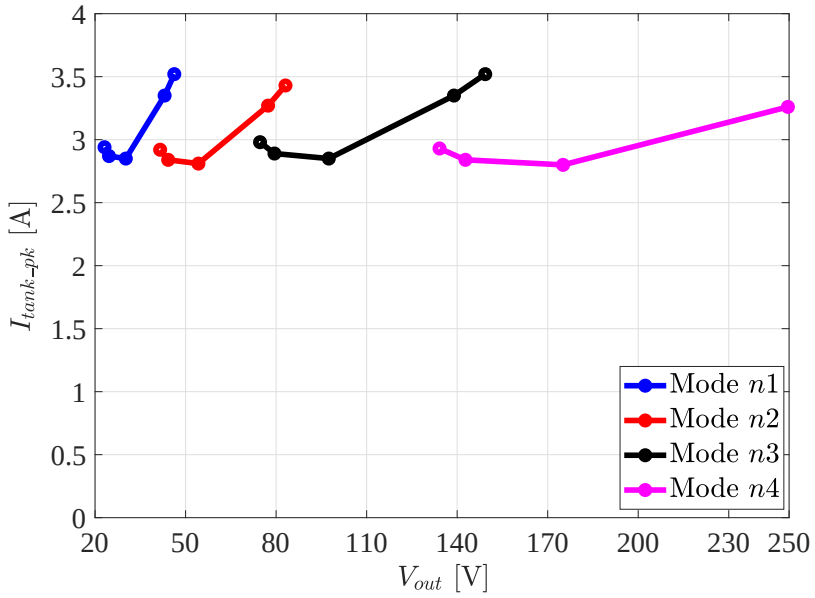


Fig. 5.23: Peak current in resonant inductor (I_{tank_pk}) of the converter at different Output voltage (V_{out}), operating at full power. Blue curve is for mode $n1$, red curve is for mode $n2$, black curve is for mode $n3$ and magenta curve is for mode $n4$.

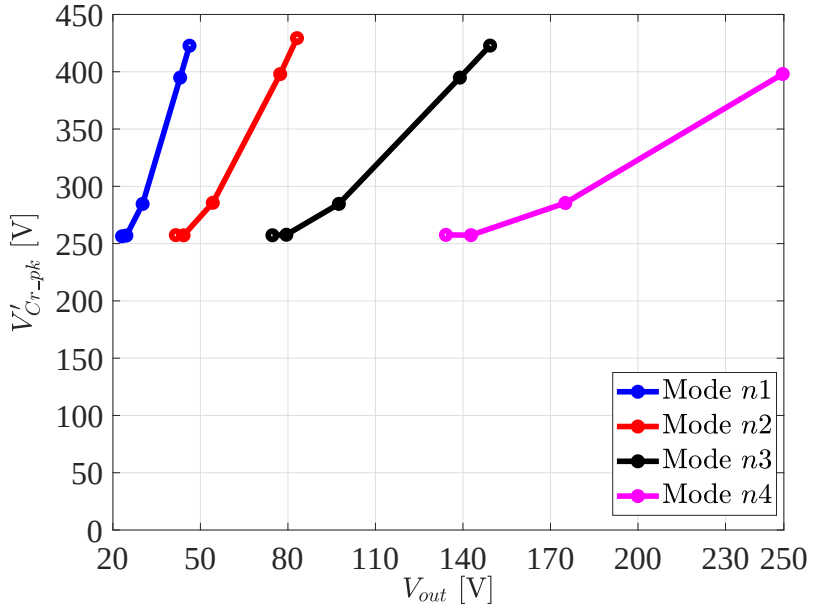


Fig. 5.24: Peak voltage across resonant capacitor (V'_{Cr_pk}) of the converter at different Output voltage (V_{out}), operating at full power. Blue curve is for mode $n1$, red curve is for mode $n2$, black curve is for mode $n3$ and magenta curve is for mode $n4$.

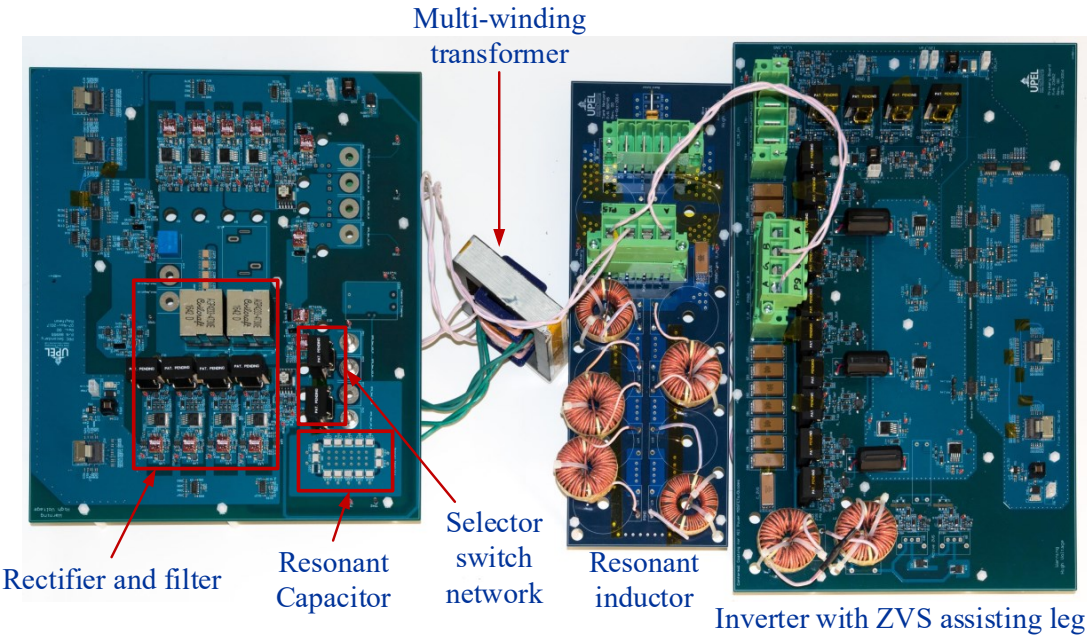
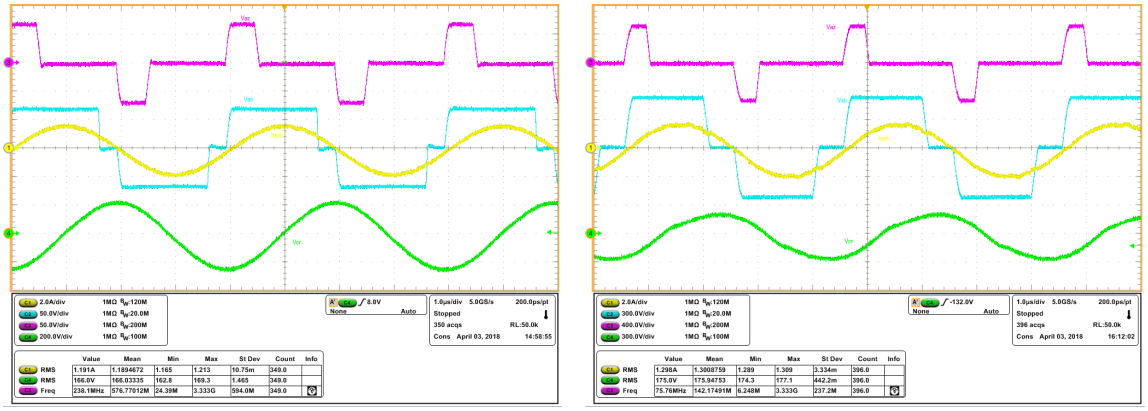


Fig. 5.25: Photograph of the converter for wide output voltage range.

presented in Table 5.3. With this prototype, the converter is operated in mode $n4$ and $n3$ with an output voltage range of 80 V to 250 V over a load range of 50 W to 500 W. The photograph of the prototype is shown in Fig. 5.25.

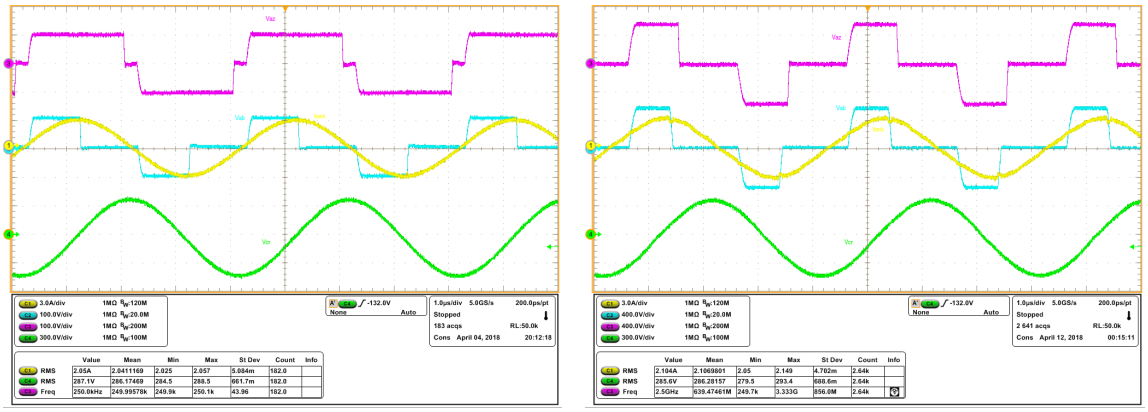
The steady state operating waveforms of the converter are shown in Fig. 5.26 and Fig. 5.27, for minimum and maximum output voltage of 80 V and 250 V, respectively at two different output power levels of 50 W and 500 W. In these plots, CH1 (yellow) is the current in the resonant inductor (i_{tank}), CH2 (cyan) is the inverter output voltage (v_{AB}), CH3 (purple) shows the voltage between inverter leading leg (leg A) and ZVS assisting leg (leg Z) (v_{AZ}) and voltage across the resonant capacitor (v'_{Cr}), on the secondary winding S_4 of transformer, is shown in CH4 (green). From these plots it can be observed that switches in both the inverter legs and the ZVS assisting leg transition through ZVS turn on for the entire range of output voltage and load.

The variation of control angle α over the range of load for minimum, maximum and intermediate voltages in both mode $n3$ and $n4$ are plotted in Fig. 5.28 and Fig. 5.29, respectively. It can be noticed that the control angle (α) stays relatively flat for the load



(a) (b)

Fig. 5.26: Converter operating waveforms for $V_{out} = 80\,\text{V}$ at (a) $P_{out} = 50\,\text{W}$ and (b) $P_{out} = 500\,\text{W}$. CH1 (yellow): i_{tank}, CH2 (cyan): v_{AB}, CH3 (purple): v_{AZ}, CH4 (green): v'_{Cr}.



(a) (b)

Fig. 5.27: Converter operating waveforms for $V_{out} = 250\,\text{V}$ at (a) $P_{out} = 50\,\text{W}$ and (b) $P_{out} = 500\,\text{W}$. CH1 (yellow): i_{tank}, CH2 (cyan): v_{AB}, CH3 (purple): v_{AZ}, CH4 (green): v'_{Cr}.

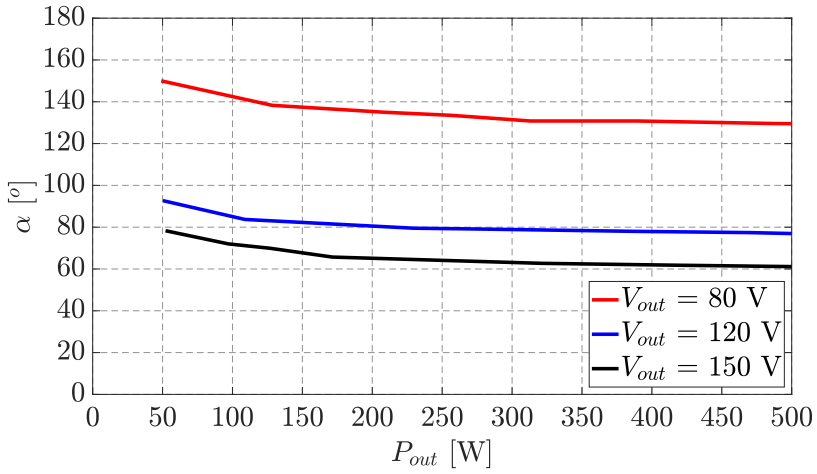


Fig. 5.28: Variation of control angle (α) over the entire load range for different output voltage(s) in operating mode $n3$.

range, at each output voltage. The slightly higher value of required α at light load is accounted for DCM operation of the output rectifier due to low current in the filter inductor (L_{f2}). In Fig. 5.30, the steady state output voltage of the converter operating at different control angle (α), at 500 W load, is shown where the red plot is for operation in mode $n4$ when the power is processed through winding S_4 and the blue plot is for operation in mode $n3$ when the power is processed through winding S_3. It can be seen from Fig. 5.30 that output voltage range of 80 V to 250 V is obtained with a relatively small variation in α ($\approx 60°$) which is possible because of utilization of the multi-winding transformer.

Efficiency of the converter is plotted against load variation for minimum, maximum and intermediate voltages in both mode $n3$ and $n4$, in Fig. 5.31 and Fig. 5.32, respectively, with peak efficiency of 94 %. The converter operates with similar efficiency profile in both modes despite different voltage outputs in two modes. Within any mode of operation, efficiency at lower output voltage is higher compared to higher output voltage, at same power. This is owing to the fact, that within a mode of operation, at higher output voltage the transformer sees a higher voltage swing and consequently higher flux swing in its magnetic core and thus results in higher core loss, irrespective of output load. With better design of the transformer, the core loss can be minimized and thus higher efficiency can be achieved.

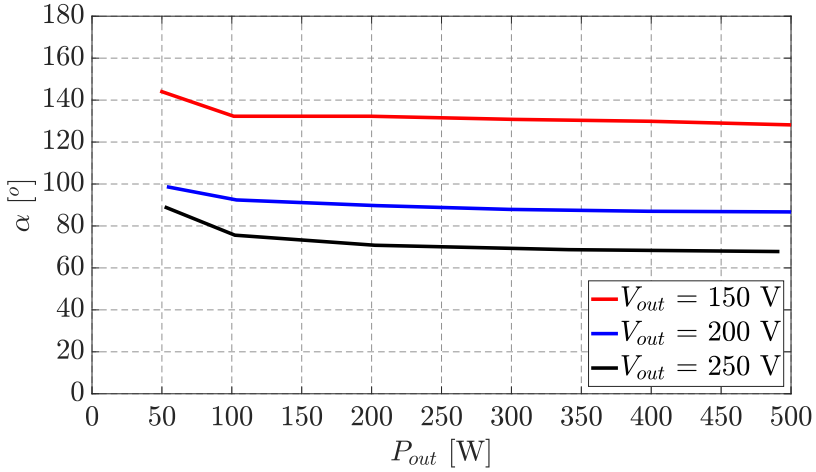


Fig. 5.29: Variation of control angle (α) over the entire load range for different output voltage(s) in operating mode $n4$.

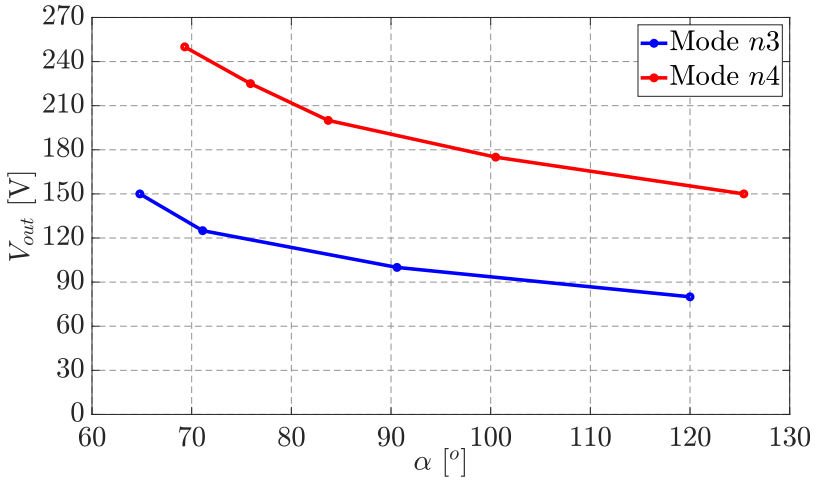


Fig. 5.30: Steady state DC output voltage of the converter at different control angle α with 500 W load. Blue plot is for operating mode $n3$ and red plot is in operating mode $n4$.

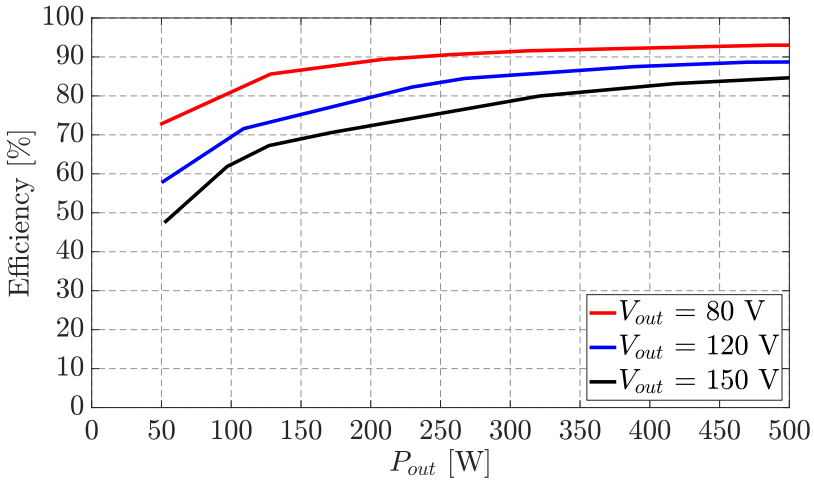


Fig. 5.31: Efficiency of the converter over the load range for different output voltage(s) in operating mode $n3$.

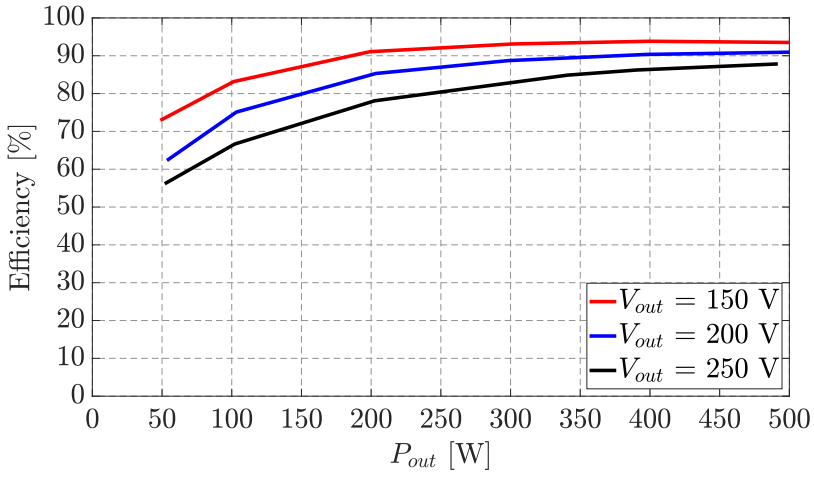


Fig. 5.32: Efficiency of the converter over the load range for different output voltage(s) in operating mode $n4$.

Summary

In this chapter, a parallel resonant tank based DC-DC converter has been analyzed for use in constant current input to constant voltage output converter. Steady state modeling of the converter is presented and the basic input output relationships are developed, with FHA. It's shown that with $F = 1$ operating point, an PRC can be operated to achieve a steady state constant voltage output characteristics across the load range, when supplied from a constant DC current source. The AC quantities within the resonant tank are derived with their phasor relationship and a design methodology, optimizing the tank and resonant inductor's VA rating, is presented. Device ratings, output filter design, control methodology and soft-switching needs are also discussed here in this chapter. A hardware prototype has been built and tested to show that the output of the converter behaves as a fairly constant voltage source at steady state, irrespective of load. Steady state operating waveforms, with ZVS of the primary side active switches, are also shown. Experimental results under load transients also confirm the constant output voltage characteristics of the converter making it suitable in constant current distribution system to get a voltage source characteristics at its output.

Designing a converter for regulated output voltage over wide range imposes a significant challenge in minimizing component stress and optimizing efficiency. A converter architecture involving a parallel resonant converter with a multi-winding transformer and switch network has been also analyzed in this chapter, showing how this converter can operate with relatively low component stress under a wide output voltage and load range in constant current DC distribution systems. Simulation results have shown how the converter operates with limited stress across the converter components under such wide range of operating points of 24 V to 250 V output voltage with full load of 1 kW, from a 1 A constant current source. Prototype hardware results are presented to demonstrate the operation of the converter in two modes, for 80 V to 250 V output range over a load range of 50 W to 500 W.

The ideal analysis of the wide output range converter, with tapping power from one of

the secondary windings, keeping resonant capacitor on another assumes that the secondary windings are tightly coupled. However, when the number of secondary windings increase, coupling among secondary windings will reduce, resulting in deviation from ideal parallel resonant converter operation. This requires a detailed modeling for multi-winding transformer [105] to be used in the analysis of this converter architecture and left as a topic of future research.

CHAPTER 6

LCL-T RESONANT CONVERTER FOR CONSTANT VOLTAGE OUTPUT

Parallel resonant converter provides load independent output voltage characteristics when power is sourced from constant current source. However, the rectifier bridge on the secondary side is fed by a sinusoidal voltage on the AC side which is the voltage across the resonant capacitor. Hence, the rectifier devices need to be rated for the peak voltage across the resonant capacitor that is at least $\frac{\pi}{2}$ times the DC output voltage. And, being voltage fed from the AC side of the rectifier, the DC side of the rectifier needs an $L-C$ filter and this output filter inductor can be bulky. These increase the overall VA rating and size of the converter. In this chapter, an LCL-T resonant network based isolated DC-DC converter is analyzed to design it as a load independent constant voltage source when supplied with constant DC current at the input. For, LCL-T resonant converter the output rectifier is current fed from the AC side and thus only capacitive filter on the DC side of the rectifier is sufficient for filtering. And the rectifier devices need to be rated for DC output voltage. Thus, LCL-T resonant converter can be designed with better VA rating than PRC. Section 6.1 introduces the modeling of the converter leading to its steady state DC input output relationship. From the steady state analysis, converter operating point, resonant tank component stress are derived in section 6.2 and a design method is established to design the converter with minimum VA rating. It is shown that use of passive rectification for this converter can limit converter operation over wide load range, which is overcome through use of active rectifier. Three angle modulation strategy for such dual active bridge (DAB) based LCL–T resonant converter is presented in section 6.3 to emulate the characteristics of diode bridge rectifier. Experimental result from a prototype converter is presented in section 6.4 for a converter regulating its output voltage at 150 V fed from a 1 A source, over load range of 50 W to 500 W proving the accuracy of the analysis. Tolerance analysis for resonant tank components and its effects on converter output is presented in

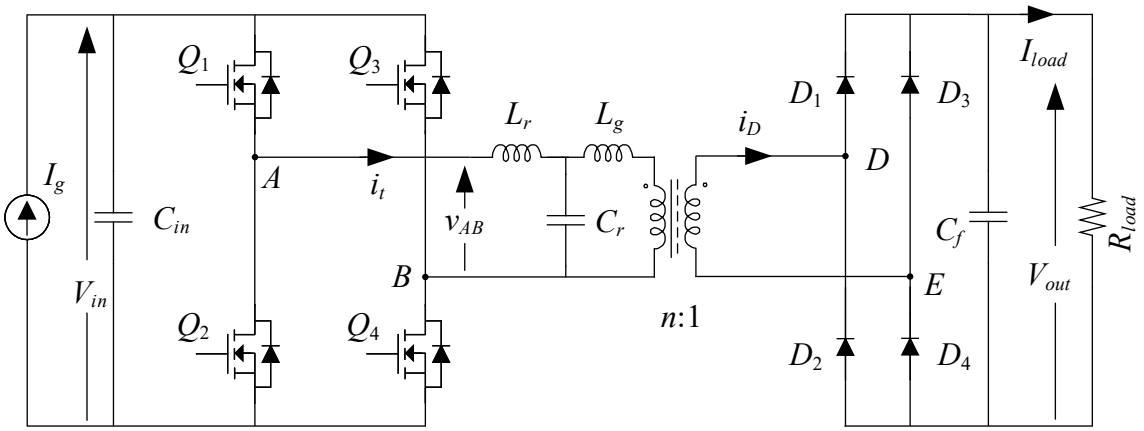


Fig. 6.1: LCL-T resonant DC-DC converter topology.

section 6.6.

6.1 Steady State Modeling and Analysis

An LCL-T resonant tank based DC-DC converter topology which converts constant DC input current to constant DC output voltage, is shown in Fig. 6.1. MOSFETs Q_1 to Q_4 form the primary side inverter which operates with symmetrical phase shift modulation with leg A leading leg B by an angle ϕ_{AB}, as shown in Fig. 6.2. The inverter converts the input DC bus voltage V_{in} to a quasi-square wave v_{AB} which drives the LCL-T resonant tank network formed by inductors L_r, L_g and capacitor C_r. The resonant tank is followed by a $n:1$ isolation transformer which is then rectified by secondary side diode bridge rectifier consisting of diodes $D_1 - D_4$. The rectified DC output is filtered through filter capacitor C_f before going to the load which is shown as a resistor R_{load}. For the analysis, it is assumed that all the components are ideal and lossless. Also, the steady state analysis is carried out with fundamental harmonic approximation (FHA) [67].

With FHA, the converter shown in Fig. 6.1 can be drawn as the equivalent circuit shown in Fig. 6.3, where

$$I_g = \langle i_{in} \rangle = \frac{2I_t}{\pi} \sin\left(\frac{\phi_{AB}}{2}\right) \cos\left(\phi_{in}\right), \tag{6.1}$$

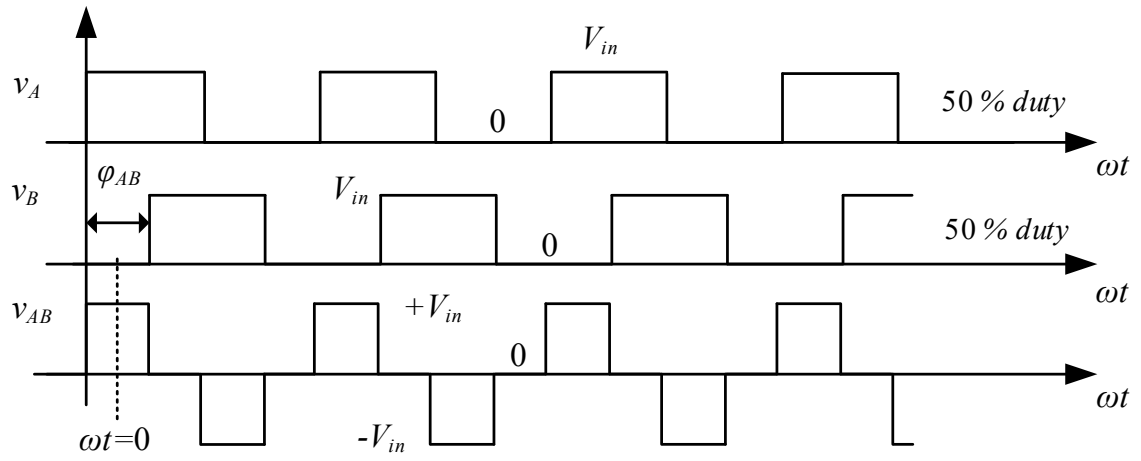


Fig. 6.2: Modulating waveform of the inverter.

$$v_{AB,1}(t) = \frac{4}{\pi} V_{in} \sin\left(\frac{\phi_{AB}}{2}\right) \cos(\omega_s t), \tag{6.2}$$

$$I_{load} = \langle i_o \rangle = \frac{2}{\pi} I'_R, \tag{6.3}$$

and the AC equivalent load resistance is given by

$$R'_e = \frac{8}{\pi^2} R_{load}, \qquad R_e = \frac{8n^2}{\pi^2} R_{load}. \tag{6.4}$$

In (6.1) – (6.4), ω_s is the angular switching frequency, average value of signal x is represented by $\langle x \rangle$, amplitude of AC side signal x_y is represented by X_y and signal or parameter x is expressed with a prime (x') on the secondary side of the transformer. In (6.1), ϕ_{in} is the angle between fundamental component of the primary side inverter output voltage and current which is given as

$$\phi_{in} = \angle Z_{in}, \tag{6.5}$$

where Z_{in} is input impedance of the loaded resonant tank, seen from the primary inverter side, as depicted in Fig. 6.4. Fig. 6.4 shows the simplified AC equivalent circuit of the converter, reflected to the primary side of the transformer.

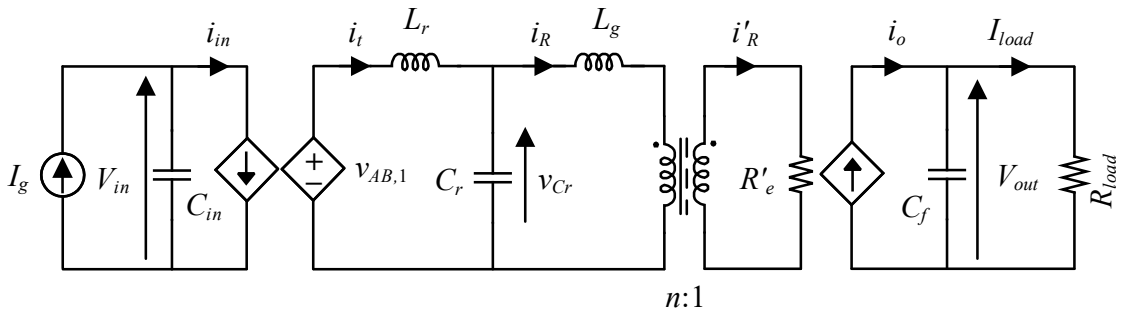


Fig. 6.3: Equivalent circuit of the LCL-T resonant converter.

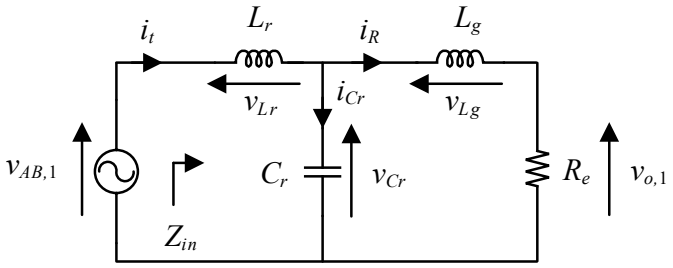


Fig. 6.4: AC equivalent circuit of the loaded LCL-T resonant tank.

From the circuit Fig. 6.4, the output to input voltage transfer function can be derived as

$$\frac{v_{o,1}(s)}{v_{AB,1}(s)} = \frac{1}{1+(1+g)\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}+g\frac{s^3}{Q\omega_o^3}}, \tag{6.6}$$

where

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}, \quad Z_o = \sqrt{\frac{L_r}{C_r}}, \quad g = \frac{L_g}{L_r}, \quad Q = \frac{R_e}{Z_o}, \quad F = \frac{\omega_s}{\omega_o} = \frac{f_s}{f_o}. \tag{6.7}$$

The amplitude of the AC voltages in Fig. 6.4 are given in terms of DC input and output voltage as

$$|v_{AB,1}| = \frac{4}{\pi} V_{in} \sin\left(\frac{\phi_{AB}}{2}\right), \quad |v_{o,1}| = \frac{4n}{\pi} V_{out}. \tag{6.8}$$

For systems with constant DC voltage source, the DC output voltage can be found using (6.6) and (6.8), evaluating the magnitude from (6.6) with $s = j\omega_s$ and is given as

$$V_{out}|_{DC\_V_{in}} = \frac{V_{in}}{n} \frac{Q \sin\left(\frac{\phi_{AB}}{2}\right)}{\sqrt{Q^2\left(1-F^2\right)^2 + \left[(1+g)F - gF^3\right]^2}}. \tag{6.9}$$

However, for systems with DC current source, V_{in} is dependent on load and expression of V_{out} from (6.9) cannot be used as it is. The output voltage for such system is derived from the equivalent circuits shown in Fig. 6.3 and Fig. 6.4.

The AC active power drawn from the inverter which equals to the DC input and output power of the lossless converter and are given as

$$P_{AC} = \frac{V_{AB,1,rms}^2}{|Z_{in}|}\cos\left(\phi_{in}\right), \quad P_{in} = V_{in}I_g, \quad P_{out} = \frac{V_{out}^2}{R_{load}}, \tag{6.10}$$

where $V_{AB,1,rms}$ is rms value of the fundamental component of inverter output voltage $v_{AB,1}$, as given in (6.2). With lossless power conversion, from (6.10), the input voltage can be expressed as

$$V_{in} = \frac{V_{out}^2}{I_g R_{load}}. \tag{6.11}$$

Equating the DC output power to the AC active power in (6.10) and using expressions from (6.1) – (6.2) and (6.11), the DC output voltage can be expressed as

$$V_{out} = \frac{\pi^2}{8n}\frac{Z_o I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)}\sqrt{\frac{Q}{\cos\left(\phi_{in}\right)}\frac{|Z_{in}|}{Z_o}}. \tag{6.12}$$

The expression of input impedance of the loaded resonant tank, in (6.12), can be derived from Fig. 6.4. The impedances of individual tank components are given by

$$X_{Lr} = 2\pi f_s L_r = FZ_o, \qquad X_{Lg} = gFZ_o, \qquad X_{Cr} = \frac{1}{2\pi f_s C_r} = \frac{Z_o}{F}. \tag{6.13}$$

Now, the tank input impedance can be derived as

$$Z_{in} = jFZ_o + \frac{-j\frac{Z_o}{F}\left(R_e + jgFZ_o\right)}{-j\frac{Z_o}{F} + \left(R_e + jgFZ_o\right)}, \tag{6.14}$$

which can be expressed in the form below as

$$Z_{in} = \frac{Z_o}{\left[\left(1 - gF^2\right)^2 + F^2Q^2\right]} \left[Z_R + jZ_I\right], \tag{6.15}$$

where the real and imaginary terms in (6.15) are defined as

$$Z_R = Q\left(1 - gF^2\right)\left(1 - F^2\right)^2 + (1+g)\,QF^2 - gQF^4, \tag{6.16}$$

$$Z_I = (1+g)\,F\left(1 - gF^2\right) - gF^3\left(1 - gF^2\right) - FQ^2\left(1 - F^2\right)^2. \tag{6.17}$$

The analysis presented in this section establishes the steady state relations between DC input and output for an LCL-T resonant converter, with its dependence on tank parameters and operating point, which is used in next section for design of the converter.

6.2 Design of LCL-T Resonant Converter

The DC output voltage of the converter, derived in (6.12), is dependent on the resonant tank parameters, load, operating frequency etc. In this section, it will be shown how the converter is designed, with proper choice of operating point, to achieve load independent output voltage from constant current input. With further analysis, a design method to optimize tank components and transformer turns ratio, is also presented in this section.

6.2.1 Operating Point Selection

From the expression of DC output voltage in (6.12), it can be normalized to be expressed as

$$V_{out\_norm} = \sqrt{\frac{Q}{\cos\left(\phi_{in}\right)}\left|Z_{in\_norm}\right|}, \tag{6.18}$$

using a base voltage defined as

$$V_{base} = \frac{\pi^2}{8n}\frac{Z_o I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)}, \tag{6.19}$$

and the normalized input impedance (Z_{in_norm}) is defined as

$$Z_{in\_norm} = \frac{Z_{in}}{Z_o}. \tag{6.20}$$

The normalized DC output voltage (V_{out_norm}) from (6.18) is plotted against normalized switching frequency (F) in Fig. 6.5, for different load (Q), with $g = 1$, where it can be seen that V_{out_norm} becomes independent of Q, if the switching frequency of operation is selected to be equal to the resonant frequency *i.e.* with $F = 1$. Under this operating condition, the expression of output voltage from (11) is now given as

$$V_{out} = \frac{\pi^2}{8n} \frac{Z_o I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)}. \tag{6.21}$$

From (6.21), it can be seen that with $F = 1$, V_{out} is also independent of g (Lg) which is shown by V_{out_norm} versus F plot in Fig. 6.6, for different Q, with an arbitrarily chosen value of $g = 0.3$. And a special case of $g = 0$ makes it parallel resonant converter achieving load independent output voltage from constant current source [106], [107], as presented in chapter 5.

From the plots in Fig. 6.5 and Fig. 6.6, it can be observed that the output voltage is load independent within $\pm 10\,\%$ of $F = 1$. So, it is possible to operate the converter with a small variation in F around 1, in addition to phase shift control. However, with a small variation limit in F, the transient response can get limited, depending on the magnitude of load transient due to low margin from steady state operating point to controller output limit. Moreover, since the converters are part of a system of converters with common source, if they are controlled though F variation then different converters will operate at different switching frequencies, depending on their individual loads, which will introduce low frequency (difference in frequency among converters) ripple component injected to the source which is challenging for filter design. Hence all the converters are designed to operate at fixed frequency and controlled through phase shift modulation.

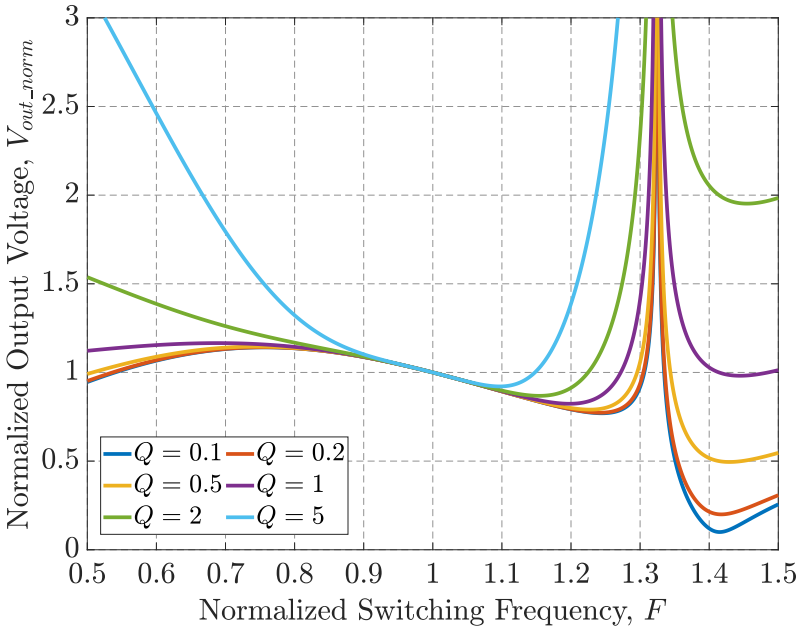


Fig. 6.5: Normalized output voltage v normalized switching frequency with $g = 1$.

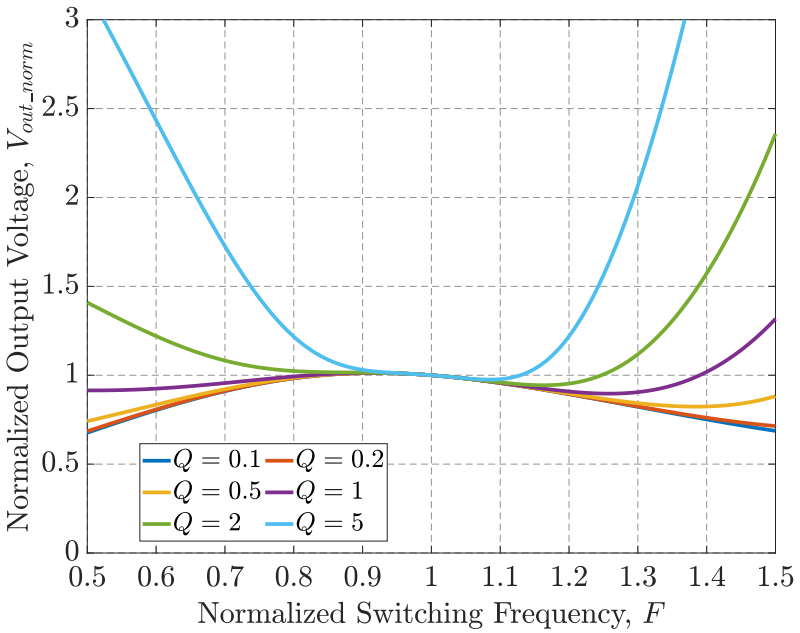


Fig. 6.6: Normalized output voltage v normalized switching frequency with $g = 0.3$.

With $F = 1$, tank's input impedance (Z_{in}) from (6.15) can be derived as

$$Z_{in}|_{F=1} = \frac{Z_o}{\sqrt{Q^2 + (1-g)^2}} \angle \tan^{-1}\left(\frac{1-g}{Q}\right). \tag{6.22}$$

From this expression of Z_{in}, if $g < 1$, ϕ_{in} is positive and thus Z_{in} becomes inductive which can help achieving ZVS for the primary side inverter switches. However, a non-zero ϕ_{in} puts a restriction on minimum power operation for which the output of the converter can be regulated [81, 100, 101], as discussed in chapter 2. Hence, g is selected to be equal to unity and with $g = 1$, Z_{in} becomes resistive, making the primary side inverter operate at unity power factor (UPF), considering FHA, and with $F = 1$ and $g = 1$, Z_{in} from (6.22) and inverter power factor, $\cos(\phi_{in})$, can be given as

$$Z_{in}|_{F=1,g=1} = \frac{Z_o^2}{R_e} \angle 0^o, \tag{6.23}$$

$$\cos(\phi_{in})\,|_{F=1,g=1} = 1. \tag{6.24}$$

6.2.2 Derivation of Tank Signals

With the selected operating point of $F = 1$ and $g = 1$, the tank AC equivalent circuit in Fig. 6.4 can be simplified and redrawn as shown in Fig. 6.7. This circuit can be solved analytically, with FHA, to derive the AC signal of the tank and the solutions are provided in this section. The phasor diagram of the AC quantities from Fig. 6.7 is drawn in Fig. 6.8 considering the fundamental component of v_{AB} as reference.

The expressions of tank signals can be derived from the equivalent circuits shown in Fig. 6.3 and Fig. 6.7. The input current (i_t) from the inverter to the resonant tank is shown in Fig. 6.9 and its rectified DC side current (i_{in}) is shown on the right hand side of the same figure. Since the average value of i_{in} comes from the DC source (I_g), the amplitude of i_t can be found out through

$$I_g = \langle i_{in} \rangle = \frac{2}{\pi} I_t \sin\left(\frac{\phi_{AB}}{2}\right). \tag{6.25}$$

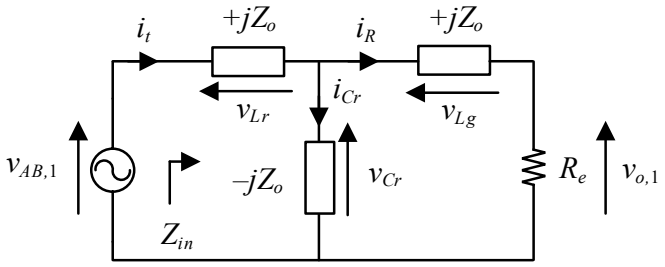


Fig. 6.7: AC equivalent circuit of the loaded LCL-T resonant tank, operating at $F = 1$ and $g = 1$.

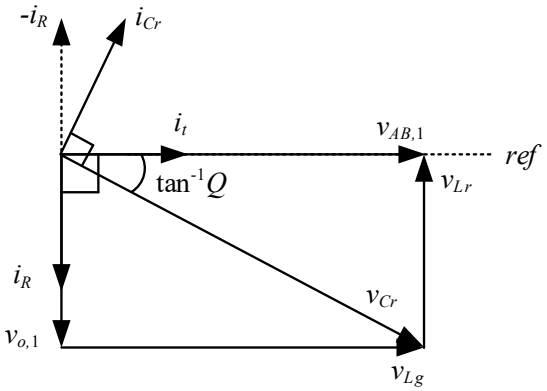


Fig. 6.8: Phasor diagram for the circuit shown in 6.7.

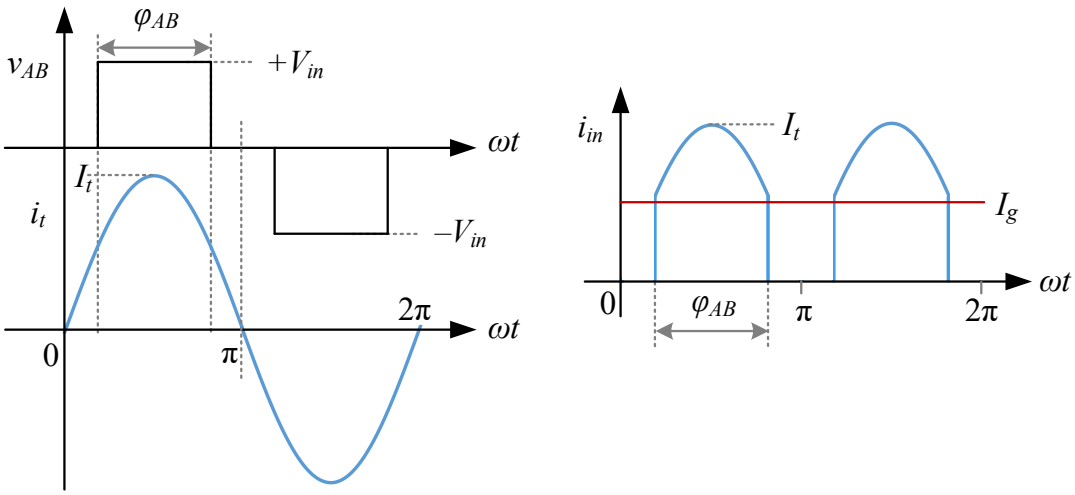


Fig. 6.9: Primary side inverter's output voltage and current waveform (left) and DC side input current waveform (right).

Since the converter is operating at $F = 1$ and $g = 1$, $v_{AB,1}$ and i_t are in phase and thus, using (6.25), the current in the resonant inductor L_r can be expressed as

$$i_t(t) = I_t \cos(\omega_s t) = \frac{\pi}{2} \frac{I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)} \cos(\omega_s t)\,. \tag{6.26}$$

The amplitude of load side resonant inductor current (i_R) is evaluated from the circuit in Fig. 6.7 with amplitude of $v_{o,1}$ from (6.8) and is given as

$$I_R = \frac{|v_{o,1}|}{R_e} = \frac{\frac{4n}{\pi} V_{out}}{\frac{8n^2}{\pi^2} R_{load}} = \frac{\pi}{2n} I_{load}. \tag{6.27}$$

Now, from the circuit of Fig. 6.7, i_R can be expressed in terms of i_t as

$$i_R = i_t \frac{-jZ_o}{-jZ_o + R_e + jZ_o} = -j\frac{Z_o}{R_e} i_t, \tag{6.28}$$

which means that i_R lags i_t by 90° and thus, using (6.27), $i_R(t)$ can be expressed as

$$i_R(t) = I_R \cos\left(\omega_s t - \frac{\pi}{2}\right) = \frac{\pi}{2n} I_{load} \cos\left(\omega_s t - \frac{\pi}{2}\right). \tag{6.29}$$

The voltage across the resonant capacitor can be found from Fig. 6.7 as well and is given by

$$v_{Cr} = i_R \left(R_e + jZ_o\right) = \frac{4n}{\pi} V_{out} \sqrt{1 + \frac{1}{Q^2}} \angle \left[-\frac{\pi}{2} + \tan^{-1}\left(\frac{1}{Q}\right)\right]. \tag{6.30}$$

Using trigonometric identity, it can be shown that

$$\tan^{-1} Q = \frac{\pi}{2} - \tan^{-1}\left(\frac{1}{Q}\right). \tag{6.31}$$

Hence, from (6.30), the resonant capacitor voltage is given as

$$v_{Cr}(t) = \frac{4n}{\pi} V_{out} \sqrt{1 + \frac{1}{Q^2}} \cos\left(\omega_s t - \tan^{-1} Q\right). \tag{6.32}$$

The current through C_r is evaluated as

$$i_{Cr} = \frac{v_{Cr}}{-jZ_o} = \frac{4n}{\pi} \frac{V_{out}}{Z_o} \sqrt{1 + \frac{1}{Q^2}} \angle \left(\frac{\pi}{2} - \tan^{-1} Q\right). \tag{6.33}$$

Using the identity shown in (6.31), current in the resonant capacitor is expressed as

$$i_{Cr}(t) = \frac{4n}{\pi} \frac{V_{out}}{Z_o} \sqrt{1 + \frac{1}{Q^2}} \cos\left[\omega_s t + \tan^{-1}\left(\frac{1}{Q}\right)\right]. \tag{6.34}$$

6.2.3 RMS Values and VA Rating of Tank Components

From the derivation of tank signals presented in (6.26), (6.29), (6.32) and (6.34), the rms values of the tank signals can be found as

$$I_{t,rms} = \frac{\pi}{2\sqrt{2}} \frac{I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)}, \tag{6.35}$$

$$I_{R,rms} = \frac{\pi}{2\sqrt{2}n} I_{load}, \tag{6.36}$$

$$V_{Cr,rms} = \frac{2\sqrt{2}n}{\pi} V_{out} \sqrt{1 + \frac{1}{Q^2}}, \tag{6.37}$$

$$I_{Cr,rms} = \frac{2\sqrt{2}n}{\pi} \frac{V_{out}}{Z_o} \sqrt{1 + \frac{1}{Q^2}}. \tag{6.38}$$

From (6.35) – (6.38), it can be observed that for a given converter operating condition $(I_g, V_{out}, \phi_{AB})$, rms current of source side resonant inductor (L_r) is constant and independent of load whereas, rms current in load side resonant inductor (L_g) is directly proportional to load (I_{load}). RMS voltage and current of the resonant capacitor is also dependent on the load (Q).

The Volt-Ampere (VA) of L_r (S_{Lr}) is evaluated as

$$S_{Lr} = I_{t,rms}^2 Z_o = \left(\frac{\pi}{2\sqrt{2}}\right)^2 \left(\frac{I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)}\right)^2 Z_o. \tag{6.39}$$

Using the expression of V_{out} from (6.21), (6.39) can be written as

$$S_{Lr} = \frac{8n^2}{\pi^2 Z_o} R_{load} \frac{V_{out}^2}{R_{load}} = \frac{R_e}{Z_o} P_{out} = Q P_{out}. \tag{6.40}$$

VA of L_g (S_{Lg}) is evaluated as

$$S_{Lg} = I_{R,rms}^2 Z_o = \left(\frac{\pi}{2\sqrt{2}n} I_{load}\right)^2 Z_o = \frac{\pi^2}{8n^2} \left(\frac{V_{out}}{R_{load}}\right)^2 Z_o = \frac{P_{out}}{Q}. \tag{6.41}$$

The VA of the resonant capacitor (S_{Cr}) can be expressed as

$$S_{Cr} = I_{Cr,rms}^2 Z_o. \tag{6.42}$$

Now, from the phasor diagram of Fig. 6.8, it can be seen that i_t and i_R in quadrature and i_{Cr} is the phasor subtraction of i_t and i_R. Hence, (6.38) can also be expressed as

$$I_{Cr,rms} = \sqrt{I_{t,rms}^2 + I_{R,rms}^2}, \tag{6.43}$$

and using (6.43), (6.42) can be written as

$$S_{Cr} = \left(I_{t,rms}^2 + I_{R,rms}^2\right) Z_o = \left(Q + \frac{1}{Q}\right) P_{out}. \tag{6.44}$$

It can be seen from (6.40), (6.41) and (6.44) that the VA of the tank capacitor is the sum of VA of the tank inductors. The total VA of the tank is calculated by summing up (6.40), (6.41) and (6.44) and is given by

$$S_{tank} = 2\left(Q + \frac{1}{Q}\right) P_{out}. \tag{6.45}$$

6.2.4 Design of Resonant Tank

To find the VA rating of the resonant tank, (6.45) needs to be evaluated at maximum output power (P_{out_max}). The normalized VA rating (S_{tank_norm}), with respect to P_{out_max} can be given from (6.45) as

$$S_{tank\_norm} = 2\left(Q_{Pout\_max} + \frac{1}{Q_{Pout\_max}}\right), \tag{6.46}$$

where Q_{Pout_max} is the quality factor at maximum output power. It can be seen that the minimum value of S_{tank_norm} from (6.46) is attained at

$$Q_{Pout\_max} = \frac{1}{Q_{Pout\_max}} = 1, \tag{6.47}$$

and the minimum value of total tank VA rating is found out using (6.45) and (6.47) and it is given as

$$S_{tank\_min} = 4P_{out\_max}. \tag{6.48}$$

Since, the total VA rating of resonant inductors is equal to the VA rating of resonant capacitor, designing the tank with minimum VA rating means design with minimum inductor VA rating. And, as discussed in section 5.2.1, through (5.44) and (5.45), design with minimum inductor VA rating will result in minimizing the size of the resonant tank.

In order to design the individual tank elements, we need to start at (6.21) where V_{out} and I_g are known, but, n, Z_o and ϕ_{AB} are to be decided on. From the expression of Q in

(6.7) and P_{out} from (6.10), the characteristic impedance of the tank can be written as

$$Z_o = \frac{8n^2}{\pi^2}\frac{V_{out}^2}{P_{out}Q}, \tag{6.49}$$

and substituting Z_o from (6.49) into (6.21), the transformer turns ratio can be expressed as

$$n = \frac{P_{out}Q\sin\left(\frac{\phi_{AB}}{2}\right)}{I_g V_{out}}. \tag{6.50}$$

In order to achieve minimum VA rating for the tank, the optimum value of transformer turn ratio (n_{min_VA}) can be found out by substituting $Q = Q_{Pout\_max} = 1$ from (6.47) into (6.50) and is given by

$$n_{min\_VA} = \frac{P_{out\_max}\sin\left(\frac{\phi_{AB}}{2}\right)}{I_g V_{out}}. \tag{6.51}$$

The value of ϕ_{AB} is selected to be 120^o which produces least harmonic content at the output of the inverter with no triplen harmonics [60]. This also provides decent margin from maximum possible control angle of 180^o, for transient response. After determining the transformer turn ratio from (6.51), Z_o is evaluated from (6.49) as

$$Z_o = \frac{8n_{min\_VA}^2}{\pi^2}\frac{V_{out}^2}{P_{out\_max}}, \tag{6.52}$$

and from (6.7), the tank element values can be calculated as

$$L_r = \frac{Z_o}{2\pi f_o} = \frac{Z_o}{2\pi f_s}, \tag{6.53}$$

$$C_r = \frac{1}{2\pi f_o Z_o} = \frac{1}{2\pi f_s Z_o}, \tag{6.54}$$

$$L_g = L_r = \frac{Z_o}{2\pi f_s}. \tag{6.55}$$

And the ratings of the resonant elements are given in (6.35) – (6.38).

6.3 Dual Active Bridge LCL-T Resonant Converter

Table 6.1: LCL-T resonant tank parameters

L_r [µH]	C_r [pF]	L_g [µH]	n
194.4	2085	194.4	2.9

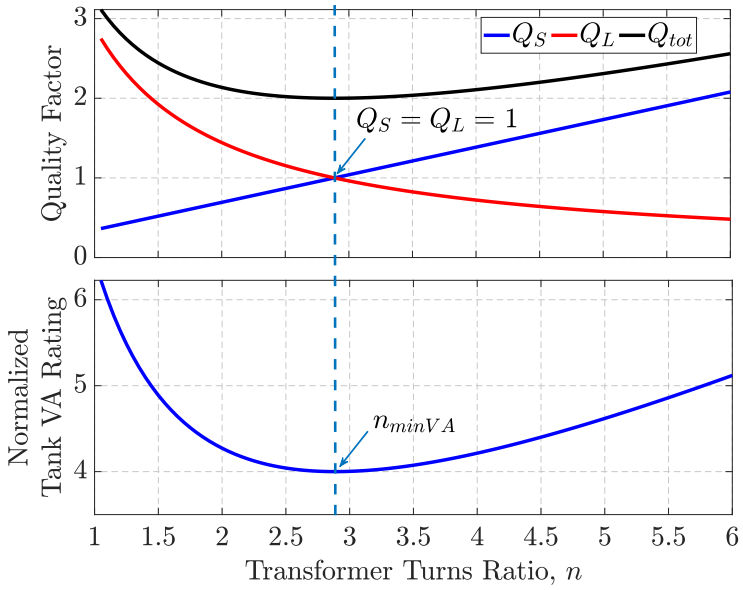


Fig. 6.10: Quality factor of the tank elements (top) and normalized VA rating of the tank (bottom) with respect to transformer turns ratio.

With the design method from Section 6.2, the converter is designed for a system with 1 A input and 150 V output with a load range of 50 W to 500 W. The designed parameters are shown in Table 6.1. The plot of quality factor and normalized tank VA rating for various transformer turns ratio is presented in Fig. 6.10. It can be seen that the tank VA is minimum at $n = n_{min\_VA}$, as per (6.51). In Fig. 6.10, the quantities Q_S, Q_L and Q_{tot} are defined as follow.

From the definition of quality factors from [108], the quality factor of the load side resonant inductor L_g is derived as

$$Q_L = 2\pi \frac{E_{Lg\_pk} f_o}{P_{out}}, \tag{6.56}$$

where E_{Lg_pk} is the peak energy stored in L_g and is given as

$$E_{Lg\_pk} = \frac{1}{2} L_g \left(\sqrt{2} I_{R,rms}\right)^2 = L_g I_{R,rms}^2, \tag{6.57}$$

and from the equivalent circuit of Fig. 6.7, P_{out} can be given as

$$P_{out} = I_{R,rms}^2 R_e. \tag{6.58}$$

Substituting, (6.57) and (6.58) into (6.56) and using definition of ω_o, Z_o and Q from (6.7), Q_L can be expressed as

$$Q_L = 2\pi f_o \frac{L_g}{R_e} = \frac{Z_o}{R_e} = \frac{1}{Q}. \tag{6.59}$$

Similarly, the quality factor of the source side resonant inductor L_r can be derived as

$$Q_S = 2\pi \frac{E_{Lr\_pk} f_o}{P_{out}}, \tag{6.60}$$

where E_{Lr_pk} is the peak energy stored in L_r and is given as

$$E_{Lr\_pk} = \frac{1}{2} L_r \left(\sqrt{2} I_{t,rms}\right)^2 = L_r I_{t,rms}^2. \tag{6.61}$$

Using the relationship between i_t and i_R from (6.28) and using (6.61) and (6.7), (6.60) can be further expressed as

$$Q_S = 2\pi f_o \frac{L_r}{R_e} \left(\frac{R_e}{Z_o}\right)^2 = \frac{R_e}{Z_o} = Q. \tag{6.62}$$

It can be observed from (6.59) and (6.62) that Q_S and Q_L are inverse of each other which means if source side inductor current is more sinusoidal (less in harmonic content) the load side inductor current will be more non-sinusoidal (more harmonic content) and

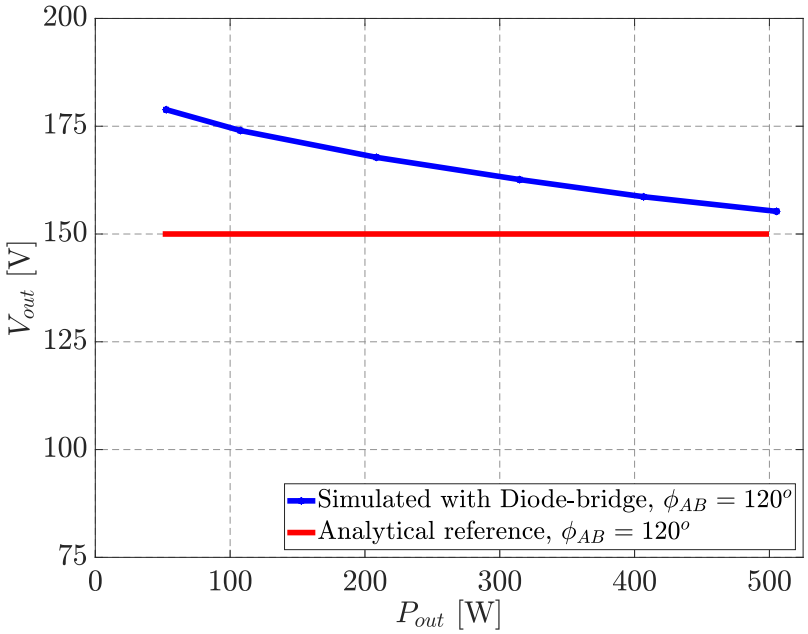


Fig. 6.11: Steady state DC output voltage (V_{out}) versus load power (P_{out}); Red: result from analysis, Blue: simulation result with diode-bridge.

vice versa. The term Q_{tot} is given as

$$Q_{tot} = Q + \frac{1}{Q}. \tag{6.63}$$

6.3.1 Limitation with Diode-bridge Rectifier

With the tank parameters listed in Table 6.1, the converter of Fig. 6.1 is simulated in MATLAB/PLECS and the steady state DC output voltage at various load is plotted in Fig. 6.11.

It can be seen from the blue plot in Fig. 6.11, that the output voltage with secondary side diode bridge rectifier does not stay constant, independent of load and increases in value as the load reduces. Since the tank is designed for minimum VA, the diodes operate in discontinuous conduction mode (DCM) due to low quality factor. This increase in V_{out} at light load will demand the control angle (ϕ_{AB}) to go towards its limit of 180° in order to keep the output voltage at its desired value. This can potentially hinder the load range of operation for which the converter can regulate its output. In order to keep the diodes

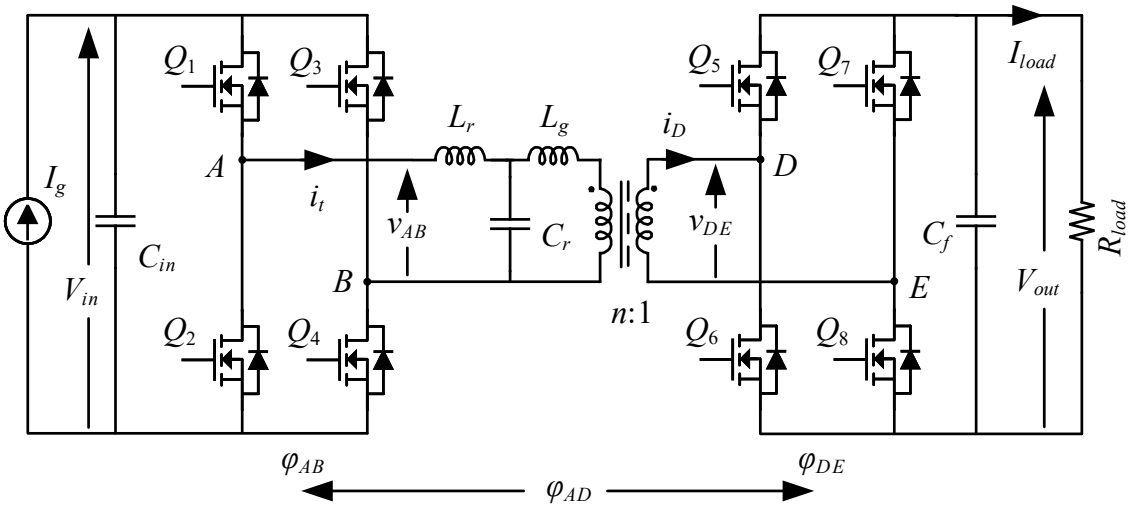


Fig. 6.12: DAB LCL-T resonant DC-DC converter topology.

in continuous conduction mode (CCM) over a load range, the tank components have to be designed with higher VA rating which will increase the size of the converter. Alternately, the converter can be designed with lower nominal value of ϕ_{AB}, considering the load range and margin for component tolerances, but this will lead to higher component stress (6.35 – 6.38) and losses.

6.3.2 Secondary Side Active Rectification

To operate the converter with wide range load regulation, it is essential to keep the secondary bridge in CCM. This is done employing an active bridge on the secondary side, as shown in Fig. 6.12. The modulation scheme for both primary and secondary bridges are depicted in Fig. 6.13 where ϕ_{DE} is the control angle between leg D and leg E of secondary bridge and ϕ_{AD} is the angle between leg A and leg D.

With secondary active bridge, current in L_g as well as in transformer secondary will be in CCM. To operate the secondary bridge at unity power factor (with FHA) in order to emulate the behavior of diode rectifier, the secondary bridge modulation angle ϕ_{DE} should be equal to 180° and from the phasor diagram shown in Fig. 6.8, the relationship among

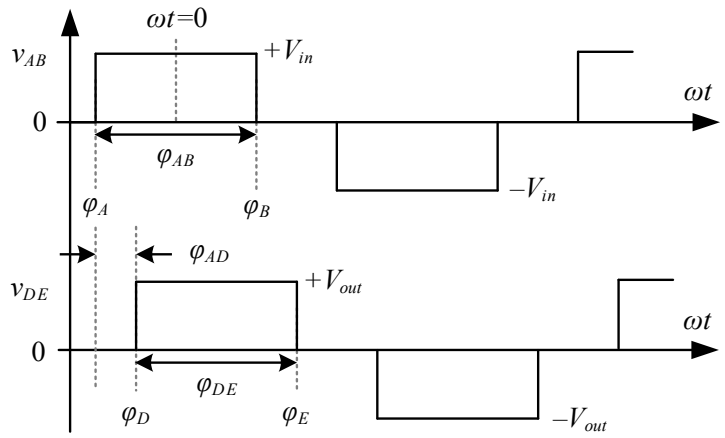


Fig. 6.13: Modulation waveform of DAB LCL-T resonant DC-DC converter topology.

the three modulation angles [ϕ_{AB}, ϕ_{AD}, ϕ_{DE}] can be given as

$$\phi_{AD} = \frac{\phi_{AB}}{2} + \frac{\pi}{2} - \frac{\phi_{DE}}{2}, \tag{6.64}$$

which, with $\phi_{DE} = 180°$, becomes

$$\phi_{AD} = \frac{\phi_{AB}}{2}. \tag{6.65}$$

The DAB LCL-T resonant converter is also simulated in MATLAB/PLECS, with the tank parameters presented in Table 6.1 and the steady state DC output voltage over the load range is plotted in black in Fig. 6.14. This is also compared with result achieved with diode-bridge on the secondary side and is shown by blue graph in the same plot. From the black plot in Fig. 6.14, it can be seen that the steady state DC output voltage remains constant, independent of load, as derived in (6.21), matching analytical reference shown in red.

6.4 Experimental Verification

A prototype hardware has been built to verify the analysis presented so far with the tank parameters mentioned in Table 6.1 and additional details presented in Table 6.2. The photograph of the test setup is shown in Fig. 6.15. On the primary side inverter leg B

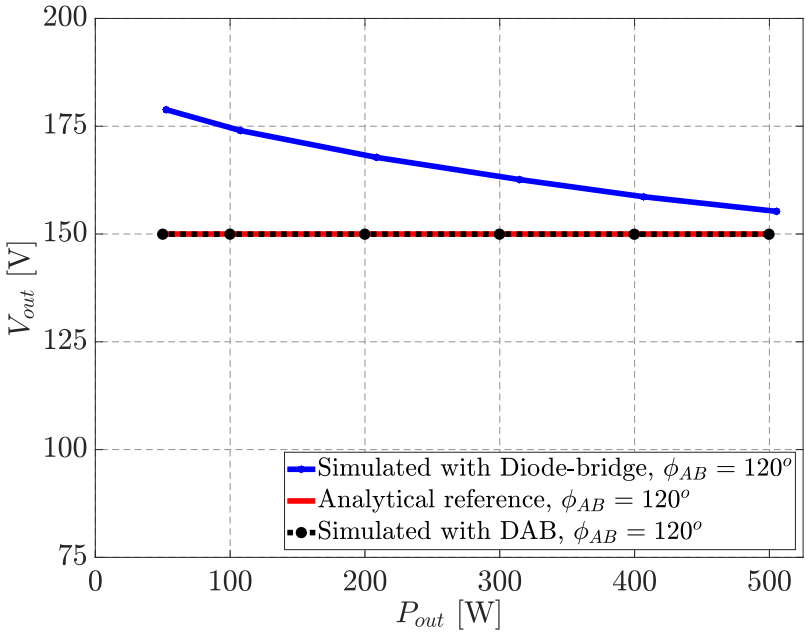


Fig. 6.14: Steady state DC output voltage (V_{out}) versus load power (P_{out}); Red: result from analysis, Blue: simulation result with diode-bridge, Black: simulation result with DAB.

MOSFETs go through ZVS by tank current and an active ZVS assisting circuit, presented in section 3.2.1, is used for leg A [102]. Since the secondary side bridge operates at unity power factor with fixed DC output voltage, a fixed, passive inductor (L_{zvs_sec}) based ZVS assisting circuit, as presented in section 3.1, is used across the secondary H-bridge for ZVS [82] of secondary side MOSFETs. DC blocking capacitors (C_{DC_pri} and C_{DC_sec}) are used in both primary and secondary side H-bridges to block any DC component of voltage arriving out of the inverters due to any component non-idealities. The values of C_{DC_pri} and C_{DC_sec} are selected such that the resonance frequency between C_{DC_pri} and L_r and between C_{DC_sec} and L'_g are an order lower than the main tank resonant frequency f_o.

First, the converter is tested with a diode bridge rectifier and the results are shown in Fig. 6.16 for 50 W and 500 W operation with $\phi_{AB} = 120°$. It can be seen from the v_{DE} (purple) and i_D (green) plot in Fig. 6.16(a) that the diode bridge operates in DCM mode.

Then, before performing power transfer test through the converter with DAB, the PWM and gate to source signals for the legs of the primary and secondary H-bridges are tested to check for delays and synchronization between primary and secondary and the captured

Table 6.2: Details of the LCL-T resonant converter

Component / Parameter	Part Number / Value
I_g [A]	1
V_{out} [V]	150
f_s [kHz]	250
P_{out} [W]	50 – 500
$Q_1 - Q_4$	C2M1000170D (2 in parallel)
C_{DC_pri} [µF]	0.23
L_{zvs_pri} [µH]	50
$D_1 - D_4$	FFSH2065B-F085
$Q_5 - Q_8$	IXFQ72N20X3
C_{DC_sec} [µF]	6.4
L_{zvs_sec} [µH]	60

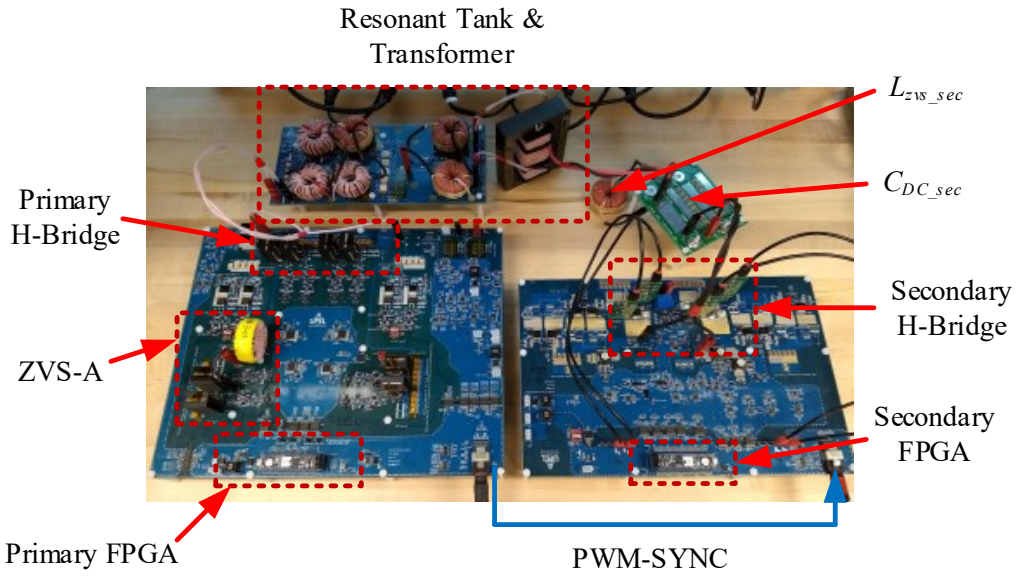
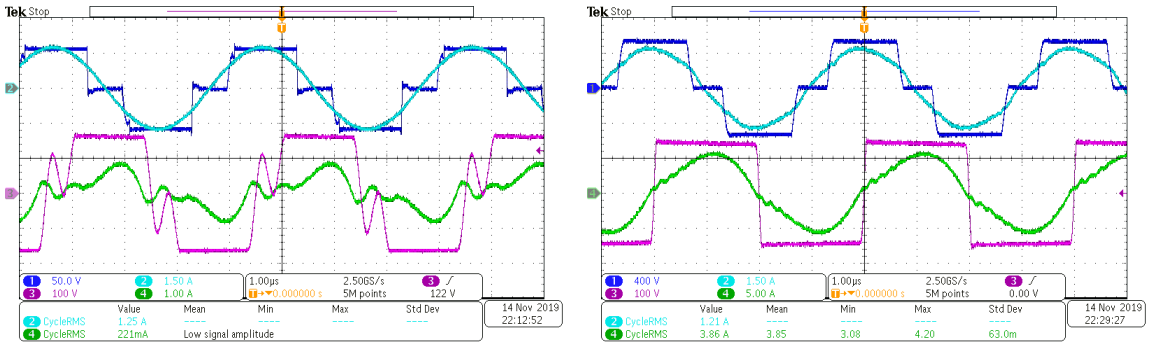


Fig. 6.15: Photograph of the hardware test setup.



(a) (b)

Fig. 6.16: Steady state operating waveforms with diode-bridge on the secondary side with $\phi_{AB} = 120°$, (a) at 50 W and (b) at 500 W load. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v_{DE}, CH4 (green): i_D.

results are shown in Fig. 6.17. The delay between PWM signal for leg A bottom device (P_{A_Bot}) and corresponding gate to source voltage ($v_{GS\_A\_Bot}$) is shown in Fig. 6.17(a). Similar delay between PWM signal for leg D bottom device (P_{D_Bot}) and corresponding gate to source voltage ($v_{GS\_D\_Bot}$) is shown in Fig. 6.17(b). These two waveforms show same delay (≈70 ns) between PWM and gate to source voltage for all the switches and hence the commanded ϕ_{AD} between PWM for leg A and leg D is preserved across the gate to source signals for leg A and leg D, which is shown by the waveforms presented in Fig. 6.17(c) and Fig. 6.17(d).

With this synchronization between primary and secondary bridges, the commanded ϕ_{AD} is expected to be followed at the output voltage of the primary and secondary H-bridges, as long as switches in all the legs of the primary and secondary bridges go through ZVS or all of them go through hard switching. However, from the initial test results with DAB LCL-T, the output voltage(s) of the H-bridges are found to be not following the commanded modulation angle, even though all the MOSFETs underwent ZVS transition, which is shown in Fig. 6.18. From the waveform of v_{AB} (deep blue) and v_{DE} (purple) in Fig. 6.18(a) and Fig. 6.18(b), it can be observed that the positive rising edge of v_{DE} is not center-aligned with v_{AB}, which is expected for the chosen modulation strategy (6.65). This is primarily due to the highly non-linear output capacitance of the selected secondary side MOSFETs, which makes the ZVS transition instances in v_{DE} to take a non-linear, sigmoid

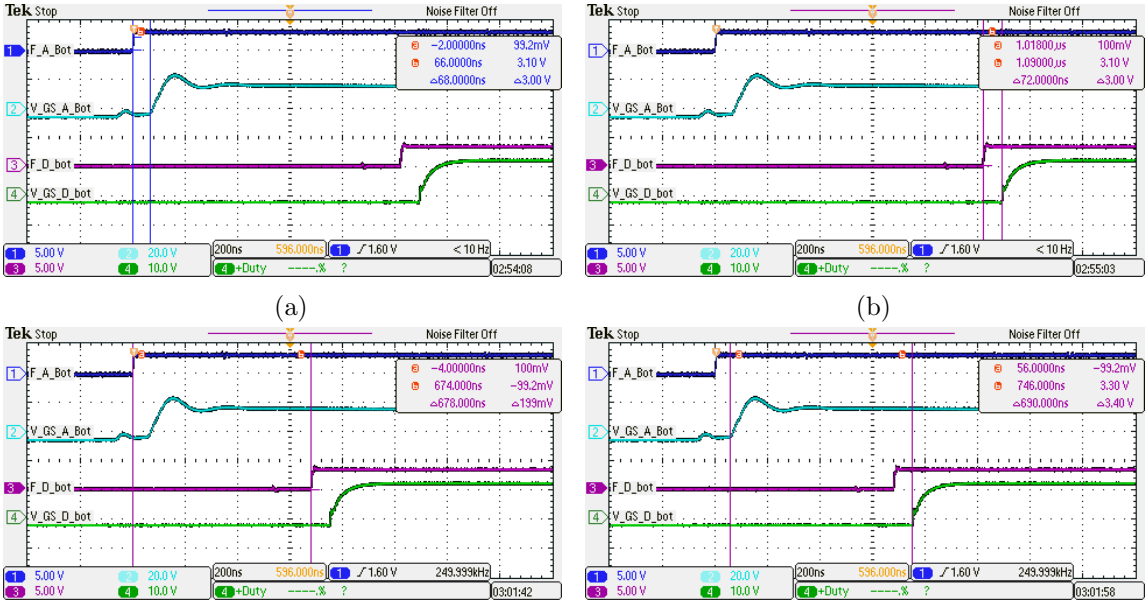


Fig. 6.17: PWM and gate to source signals for bottom MOSFETs in leg A and leg D showing various time differences. CH1 (deep blue): P_{A_Bot}, CH2 (cyan): $v_{GS\_A\_Bot}$, CH3 (purple): P_{D_Bot}, CH4 (green): $v_{GS\_D\_Bot}$.

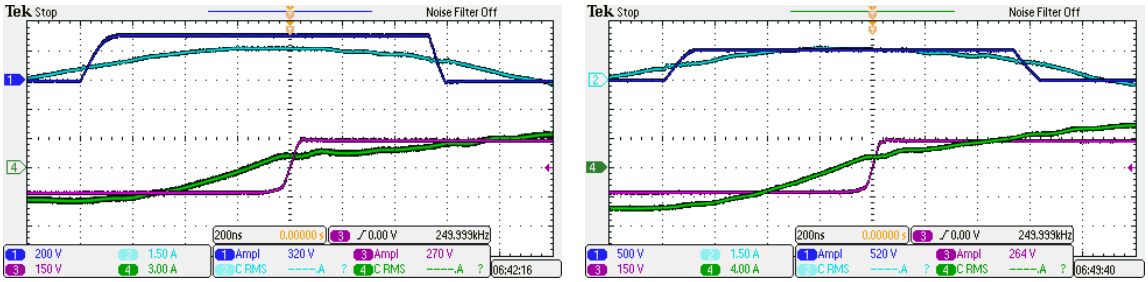
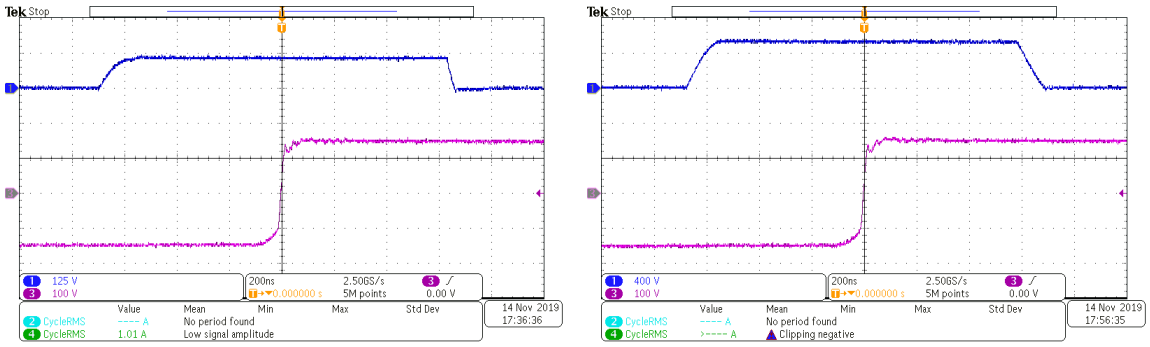


Fig. 6.18: Zoomed in steady state operating waveforms of the H-bridges with commanded $\phi_{AB} = 120°$, $\phi_{DE} = 180°$, and $\phi_{AD} = 60°$, (a) at 300 W and (b) at 500 W load. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v_{DE}, CH4 (green): i_D.

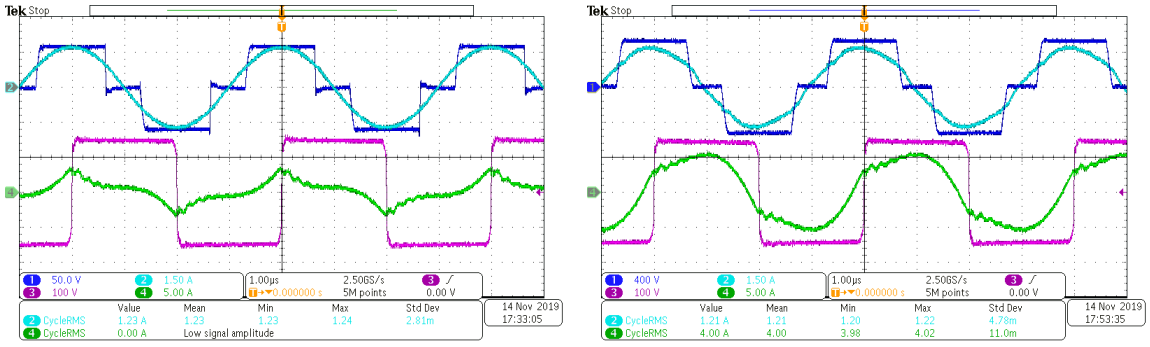
shape. And this in turn shifts the mid point of the positive transitioning edge of v_{DE} to move to the right of mid point of flat top region of v_{AB}, as shown by the asymmetry in Fig. 6.18. This has been rectified by adjusting the commanded ϕ_{AD} from the FPGA by a fixed reduction of 84 ns and the results for v_{AB} (deep blue) and v_{DE} (purple) are shown in Fig. 6.19(a) and Fig. 6.19(b) at 100 W and 500 W load, respectively.

After correcting the commanded ϕ_{AD} from the FPGA controller, the converter is tested



(a) (b)

Fig. 6.19: Zoomed in steady state operating waveforms of the H-bridges with adjusted ϕ_{AD}, with $\phi_{AB} = 120°$, $\phi_{DE} = 180°$, and $\phi_{AD} = 60°$, (a) at 100 W and (b) at 500 W load. CH1 (deep blue): v_{AB}, CH3 (purple): v_{DE}.



(a) (b)

Fig. 6.20: Steady state operating waveforms with active bridge on the secondary side with $\phi_{AB} = 120°$, $\phi_{DE} = 180°$, and $\phi_{AD} = 60°$, (a) at 50 W and (b) at 500 W load. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v_{DE}, CH4 (green): i_D.

with active rectifier (DAB) and the steady state operating waveforms are shown in Fig. 6.20 for 50 W and 500 W operation with $\phi_{AB} = 120°$, keeping $\phi_{DE} = 180°$ and $\phi_{AD} = 60°$. In the oscilloscope captures shown in Fig. 6.16 and Fig. 6.20, v_{AB} is shown in CH1 (deep blue), i_t in CH2 (cyan), v_{DE} in CH3 (purple) and i_D in CH4 (green).

The steady state DC output voltage results with both a diode bridge and an active bridge secondary are plotted in Fig. 6.21, versus the load power at fixed $\phi_{AB} = 120°$. In 6.21, the red plot is the analytical reference (150 V) and the blue and black traces represent the results with a diode rectifier and an active rectifier, respectively. It can be seen that the output voltage is not load independent for a diode bridge, whereas, with an active

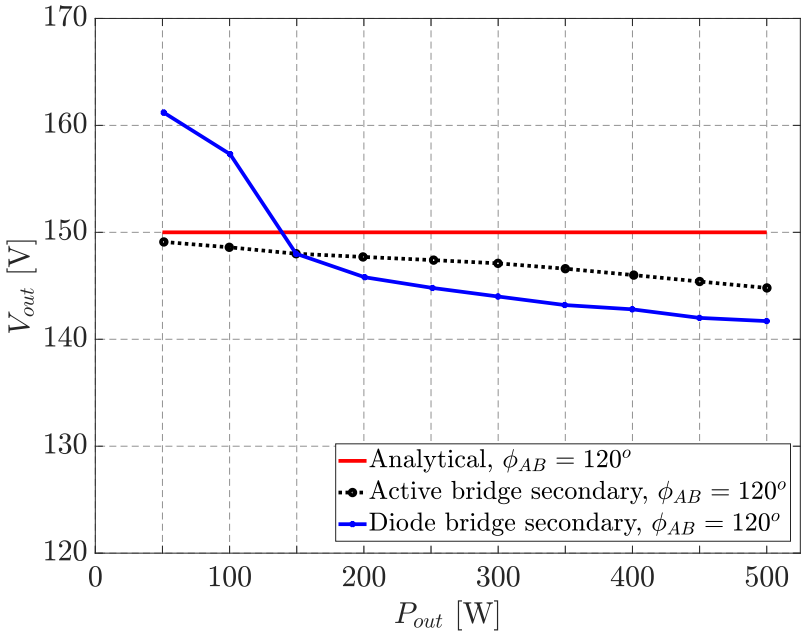


Fig. 6.21: Steady state DC output voltage (V_{out}) versus load power with $\phi_{AB} = 120°$. Red: result from analysis, blue: experimental result with diode-bridge on the secondary, black: experimental result with active bridge on the secondary.

secondary bridge, the output voltage is relatively constant over a 10:1 load range. The variation in V_{out} with an active secondary is between 149.1 V and 144.8 V, which is a drop only about 2.9 %. The variation is due to non-idealities such as ESR of components. From the hardware results, the variation of V_{out} with a diode bridge is lower than predicted by simulation, which is attributed to the parasitic capacitance of the diodes. Once the diode turns off, the diode capacitance resonates with L_g, which can be seen from v_{DE} (purple) and i_D (green) plot in Fig. 6.16(a).

The variation of control angle (ϕ_{AB}) needed to keep the output voltage regulated at 150 V is plotted in Fig. 6.22, where again the red line shows the analytical prediction and the blue and black traces represent the results with a diode rectifier and an active rectifier, respectively. It can be seen from these plots that variation in ϕ_{AB} is quite large for operation with a diode bridge, whereas, with active bridge on the secondary the variation is only 5.4° over the 10:1 load range.

The DAB LCL-T resonant converter is also tested with load transient at its output

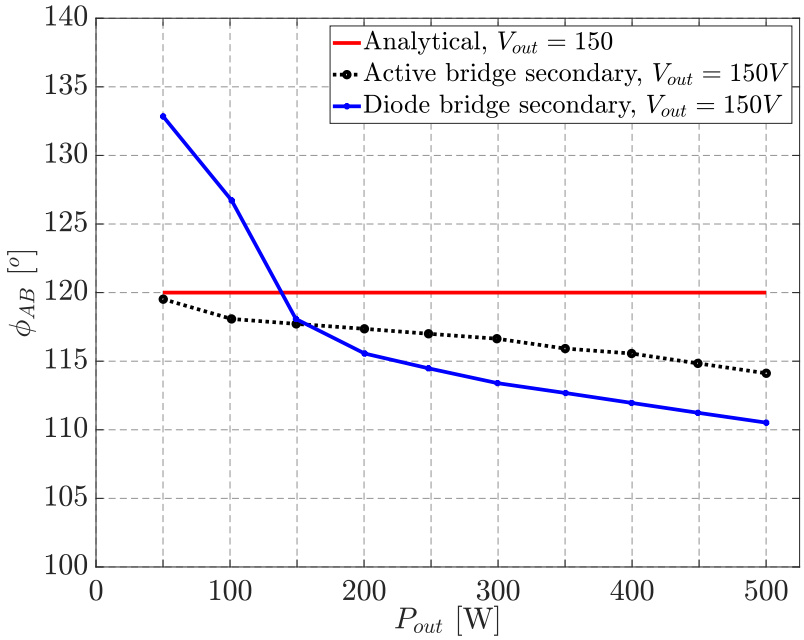


Fig. 6.22: Variation in control angle ϕ_{AB} to regulate V_{out} at a fixed value of 150 V, versus load power. Red: result from analysis, blue: experimental result with diode-bridge on the secondary, black: experimental result with active bridge on the secondary.

with a fixed control angle ($\phi_{AB} = 115°$) and the result is shown in Fig. 6.23. The output load is varied from 350 W to 400 W and then back to 350 W. In Fig. 6.23, the input DC voltage (V_{in}) is captured by CH2 (cyan), output current (I_{load}) is captured by CH1 (yellow) and the output voltage (V_{out}) is captured by CH4 (green). It can be observed from this result that even under load transient the output voltage returns to the same value at steady state.

The DAB LCL-T resonant converter's tank current and voltage signals are captured and shown in Fig. 6.24(a) and Fig. 6.24(b), for 50 W and 500 W, respectively with $\phi_{AB} = 120°$, keeping $\phi_{DE} = 180°$ and $\phi_{AD} = 60°$. From these plots in Fig. 6.24, it can be observed that the phasor relationship among the tank AC signals follow the diagram shown in Fig. 6.8. The rms values of tank inductor current and capacitor voltages are measured from the oscilloscope captures at different loads and are compared with the analytical value(s) derived in (6.35) – (6.37). The comparison is shown in Fig. 6.25, where analytical values are plotted in solid lines and the measured values are shown in corresponding circles of the same color.

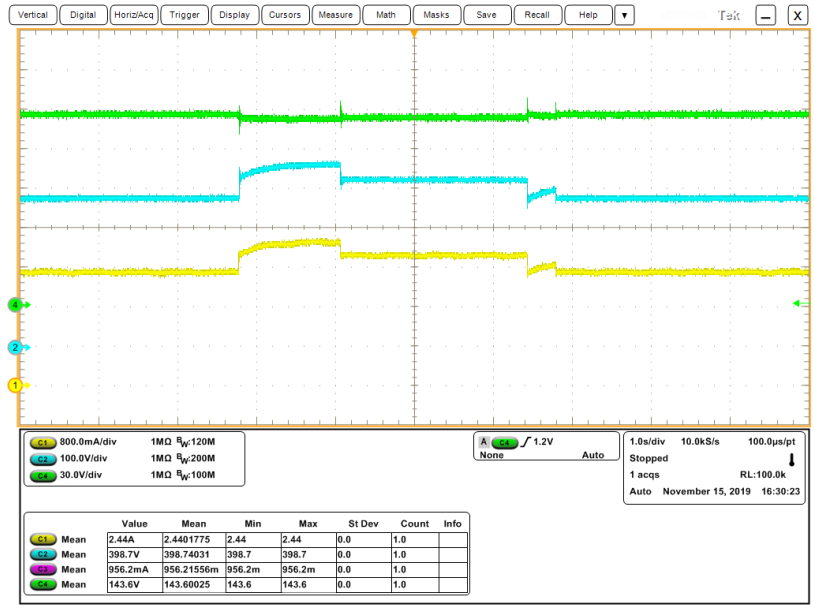
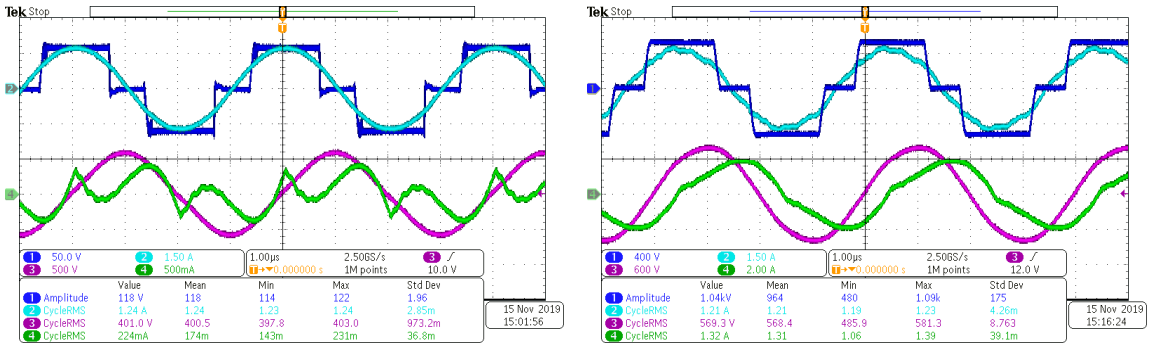


Fig. 6.23: DAB LCL-T operation under load transient from 350 W to 400 W and back to 350 W load with fixed $\phi_{AB} = 115°$. CH1 (yellow): output current, CH2 (cyan): input voltage and CH4 (green): output voltage.



(a) (b)

Fig. 6.24: Steady state operating waveforms of the resonant tank signals with $\phi_{AB} = 120°$, $\phi_{DE} = 180°$ and $\phi_{AD} = 60°$, (a) at 50 W and (b) at 500 W load. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v_{Cr}, CH4 (green): i_R.

The top plot in Fig. 6.25 compares the rms current in the tank inductors and the bottom plot compares the resonant capacitor voltage. The result depicts a good match between experimental result and analysis.

The analytically evaluated power loss in different components of the DAB LCL-T converter is presented in Fig. 6.26, at full load operating condition. These losses are used

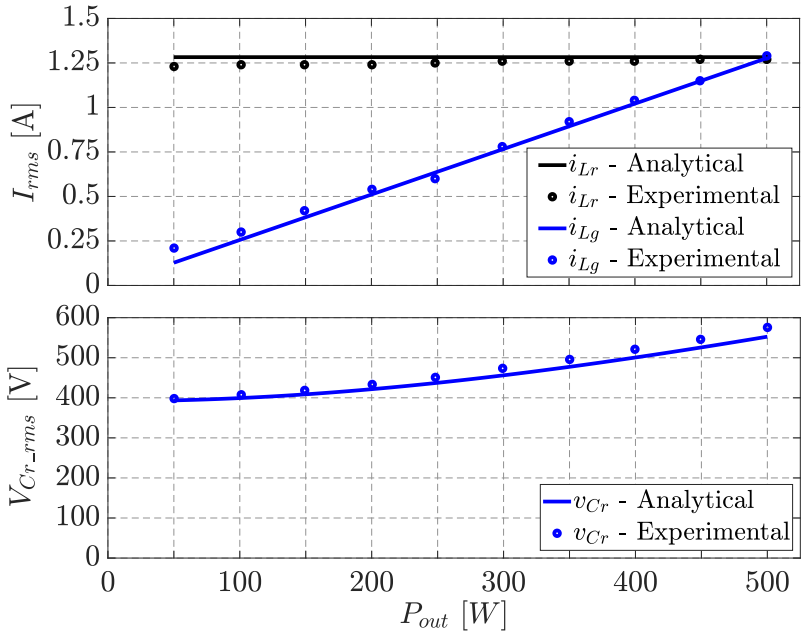


Fig. 6.25: Comparison of analytical and experimentally measured rms values of tank signals of the DAB LCL-T converter over the load range. Top plot pane: black line is for $I_{t,rms}$ and blue line is for $I_{R,rms}$; bottom plot pane: blue line shows the values for $V_{Cr,rms}$. Solid lines are for analytical and dots are for experimental results.

for components and heat sink design with natural cooling. The efficiency of the converter, operating at fixed control angle of $\phi_{AB} = 120°$, with active and passive bridges on the secondary side, is shown in Fig. 6.27 in blue and red, respectively. It can be seen that the converter operates with a higher efficiency with an active secondary bridge due to the lower conduction loss. The peak efficiency is approximately 96 %.

6.5 Comarison of LCL-T Resonant Converter with PRC

DAB LCL-T and PRC (5) both can provide load independent DC output voltage from constant DC current source. However, depending on application, one of them would be beneficial over the other. Hence a comparison is made between these two topologies, in terms of their major component ratings, in Table 6.3. It can be seen from Table 6.3 that even though there are more resonant inductors in LCL-T compared to PRC, the total VA rating (size) of the inductors are same. The transformer and secondary side devices in PRC would see higher voltage than LCL-T topology, for same operating output DC voltage. In

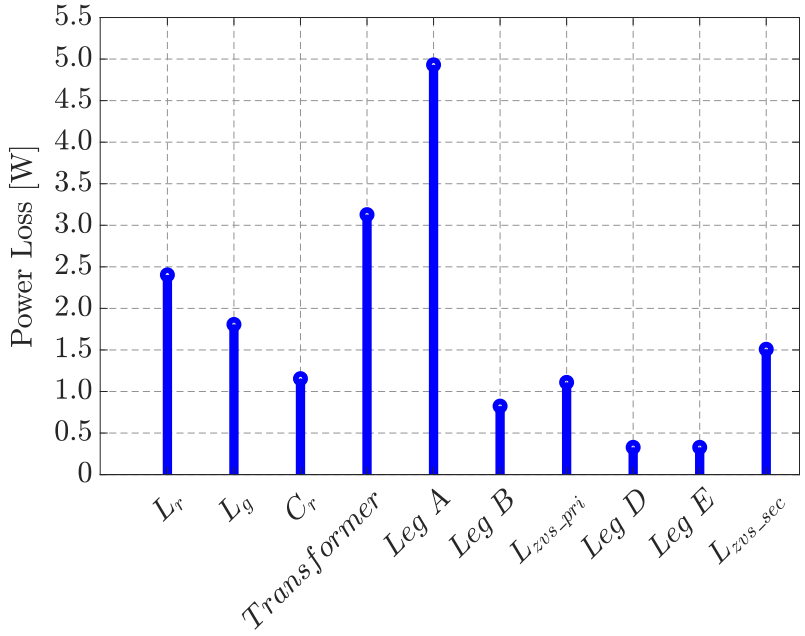


Fig. 6.26: Power loss distribution among the components of DAB LCL-T converter at full load (500 W).

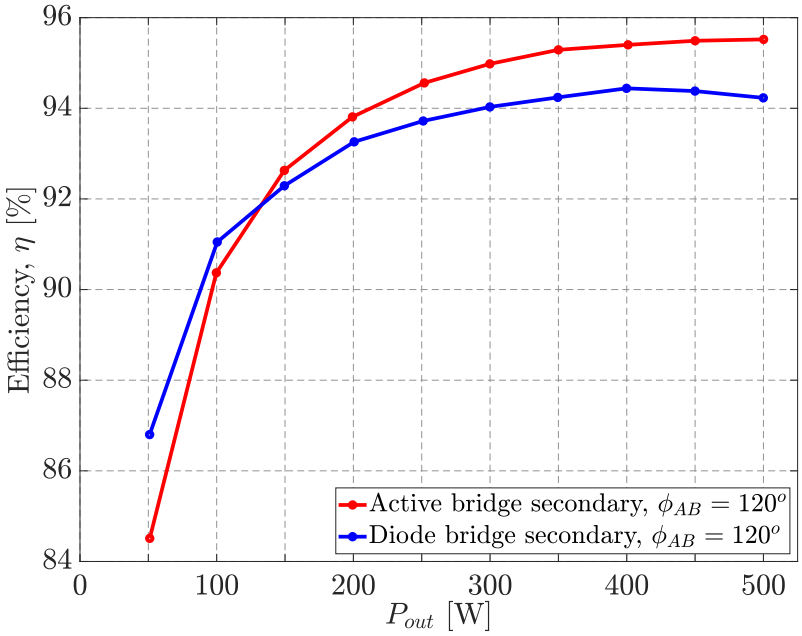


Fig. 6.27: Efficiency of the converter over the load range, operating at fixed control angle $\phi_{AB} = 120°$. Blue: experimental result with diode-bridge on the secondary, red: experimental result with active bridge on the secondary.

Table 6.3: Comparison between PRC and LCL-T resonant converter

Parameter	PRC	LCL-T RC
Inductor VA rating	$S_{Lr} = \left(Q + \frac{1}{Q}\right) P_{out}$	$S_{Lr} + S_{Lg} = \left(Q + \frac{1}{Q}\right) P_{out}$
Peak transformer voltage	$\frac{\pi}{2} V_{out}$	V_{out}
Secondary device voltage	$\frac{\pi}{2} V_{out}$	V_{out}
Output filter	L_f and C_f	C_f
PWM synchronization	Not required	Required

addition, the output filtering stage in PRC contains additional inductor (L_f) which makes the size of passive components in PRC higher compared to LCL-T RC. And, because of the presence of this filter inductor, PRC will operate with current fed bridge in reverse direction of power flow, if it is used as a bi-directional power converter, which would increase the device counts on the secondary side. Whereas, DAB LCL-T can operate as bi-directional power converter with voltage fed H-bridges on either side, which is analysed in next chapter (chapter 7).

However, if only unidirectional power flow is required with a fixed or narrow range of output load, PRC can be designed to operate with ZVS of primary side inverter switches without any assisting ciruit and without any active switches on the secondary side. This will eliminate the need of gate driver on the secondary side and PWM communication between primary and secondary bridges, which is required for LCL-T RC. And, thus in such scenario, PRC would be a better choice compared to LCL-T RC, in terms of overall cost and size.

6.6 Tolerance Analysis

The variation of output voltage due to tolerances in tank component values are shown in Fig. 6.28 using the analytical expression of V_{out} from (6.12) and Z_{in} from (6.15). In Fig. 6.28, the analytical percentage variation in V_{out} is plotted in solid lines for variation in L_r (blue), C_r (red) and L_g (black), with one of them varied at a time, keeping the remaining

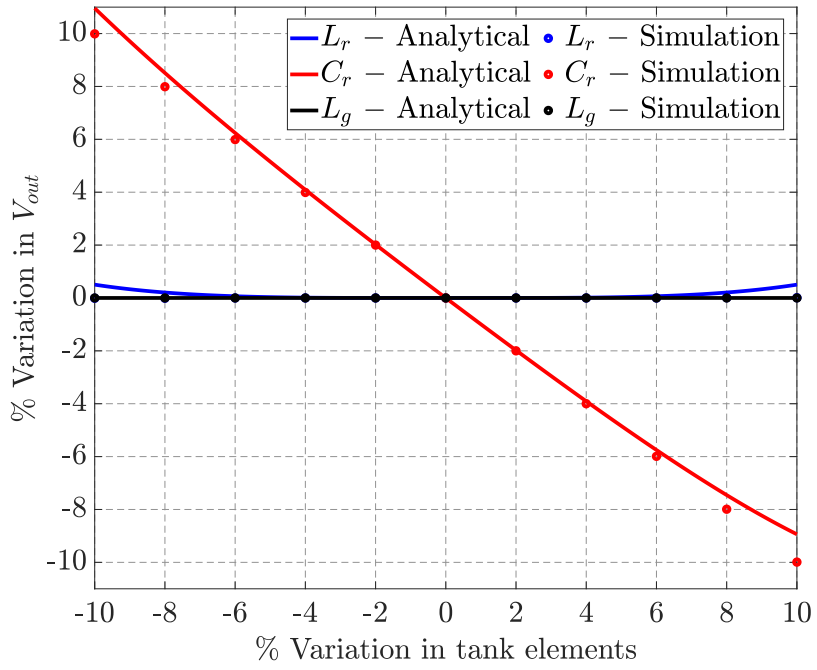


Fig. 6.28: Percentage variation in DC output voltage (V_{out}) for variation in tank elements. Blue: for variation in L_r, red: for variation in C_r, black: for variation in L_g. Solid lines are for analytical and dots are for simulation results.

two fixed at their nominal value. The tolerance results obtained from MATLAB-PLECS simulation is also shown in the same plot, using dots of corresponding color. It can be seen from this plot in Fig. 6.28 that there is a little variation in output voltage for variation in tank inductors. However, variation in resonant capacitor has a dominant effect on variation in V_{out}. The results plotted in Fig. 6.28 are for the lowest load of $P_{out} = 50\,\text{W}$, where the value of Q is maximum and has highest influence on V_{out} due to component mismatch. With use of a class I ceramic capacitor (C0G, NP0), which is stable over temperature and voltage bias, the capacitance tolerance is within $\pm 5\,\%$ which translates to variation in V_{out} within $\pm 6\,\%$, from the result plotted in Fig. 6.28. This can be taken care of by margin in modulation angle of ϕ_{AB} (120° to 180°). Further, since the tolerance is prominent at light loads, active shunt current control circuit [99] can also be utilized at the input source with slight drop of light load efficiency.

Summary

In this chapter, an LCL-T resonant tank based DC-DC converter is introduced and analyzed to be used as load independent constant output voltage source from constant DC current source. Detailed modeling, analysis and design are presented for this converter. With analysis, simulation and hardware results, it is shown that diode bridge rectification on the output side of the converter imposes a challenge on low Q (VA rating) design and the use of active bridge overcomes this limitation. A modulation scheme for the DAB LCL-T resonant converter is presented to emulate the behavior of diode bridge rectification on the secondary. And design method is established for overall operation of the converter with minimum VA rating for the tank components, the isolation transformer, and the H-bridges. ZVS requirements for all the MOSFETs are identified and suitable passive/active ZVS assisting circuits are employed to ensure ZVS turn on of all the devices. Experimental results verify the load independent output voltage characteristics with good match for tank AC signal(s) in terms of their analytical estimate(s) and experimentally measured value(s). The DAB LCL-T resonant converter is capable of bidirectional power flow and thus can be used in application requiring DC current source to DC voltage source conversion and vice versa which is explored in next chapter.

CHAPTER 7

BIDIRECTIONAL LCL-T RESONANT CONVERTER FOR CRITICAL LOADS

The converters used in the constant DC current distribution typically are unidirectional *i.e.* delivering power from the trunk cable to the load. However, in the event of any cable fault, the downstream converters lose power. But, there are few critical loads on the seabed which needs uninterrupted power for its functioning and are supplied with auxiliary power sources. A system level block diagram of the string of converters are shown in Fig. 7.1, similar to the one presented in Fig. 1.5, where multiple converters or power branching units (PBUs) are connected in series to tap power from the DC current feed to deliver required voltage or current to their respective loads.

Some of these PBUs deliver power to critical loads where redundant, identical DC-DC power converter modules are used within a PBU, as shown in Fig.7.2. The DC-DC converters within a PBU are connected to the input/output of the PBU through relay networks to select appropriate converter modules for seamless power delivery to the critical load. In addition, there is an auxiliary source housed within the PBU(s) for uninterrupted power for the critical loads. As shown in Fig. 7.3, under normal conditions, power flows from the constant current source to the load through one of the DC-DC converter modules to provide constant voltage to the load, while the other module is bypassed and kept idle. In case of fault in the line, the relay networks reconfigure the PBU with a connection shown in Fig. 7.4 where the second DC-DC module converts the power from auxiliary voltage source to a constant current drive feeding the first converter which then delivers power to the load, regulating its output voltage. Hence the power converter modules need to be capable of converting a current source to a voltage source in forward direction of power flow and a voltage source to a current drive in reverse direction of power flow.

Bidirectional dual active bridge (DAB) LCL-T resonant converter, tuned to the switching frequency, fits well in this type of application where there is a need of current to voltage

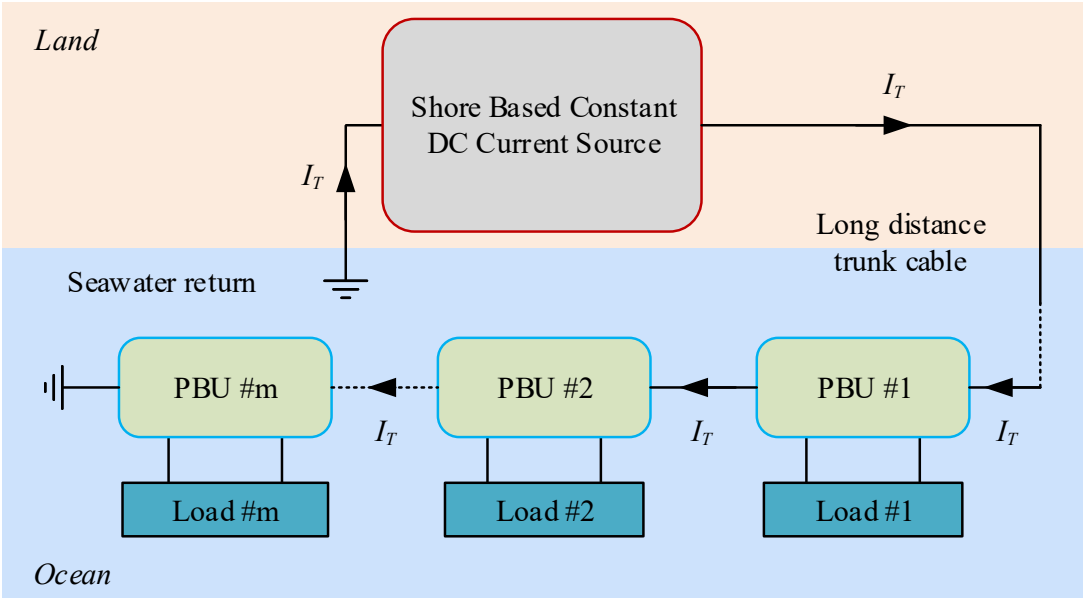


Fig. 7.1: System level block diagram of undersea DC constant current distribution network.

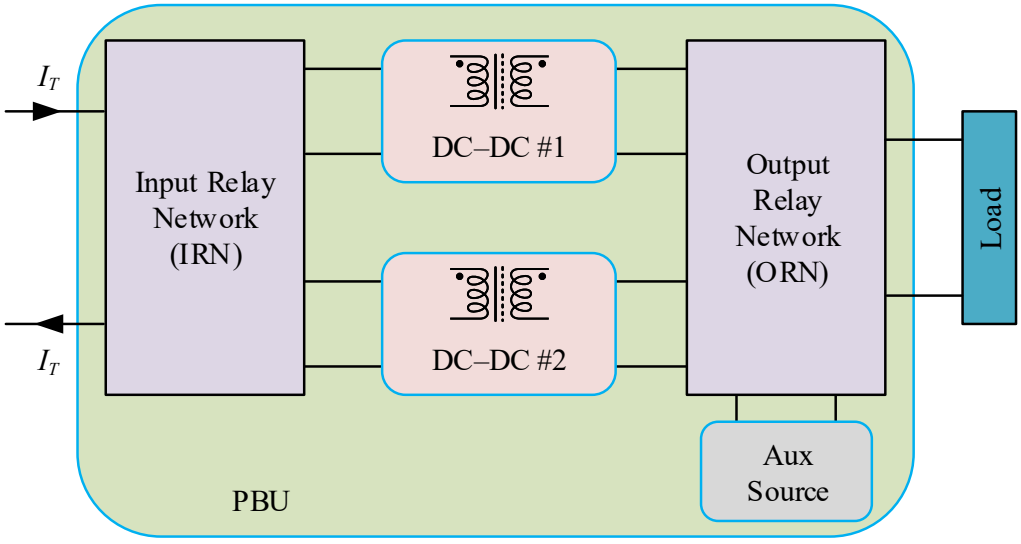


Fig. 7.2: Constituents within a PBU catering to critical loads.

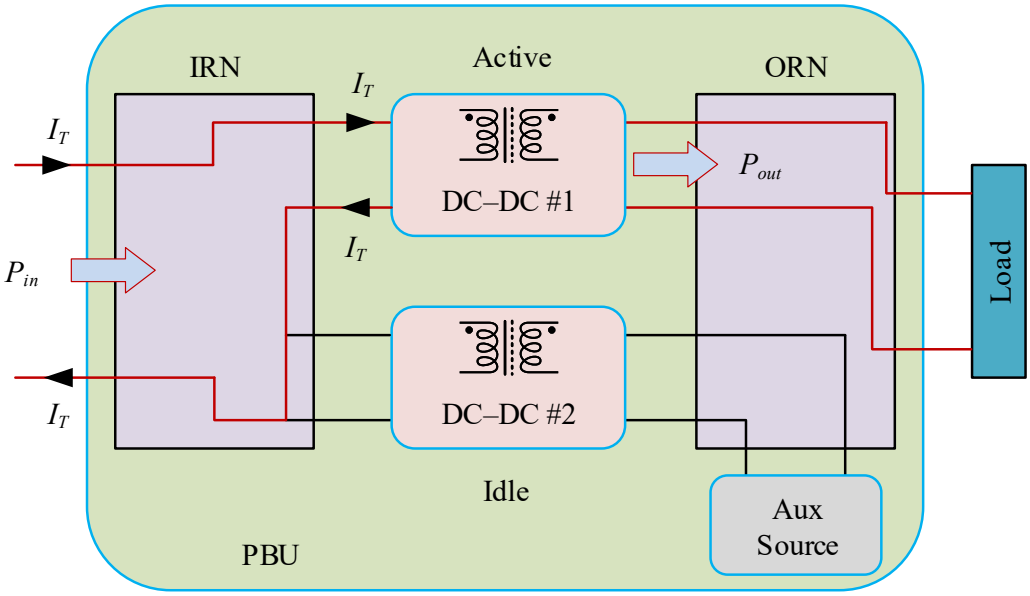


Fig. 7.3: Power flow through PBU from trunk cable to the load, under normal operating condition.

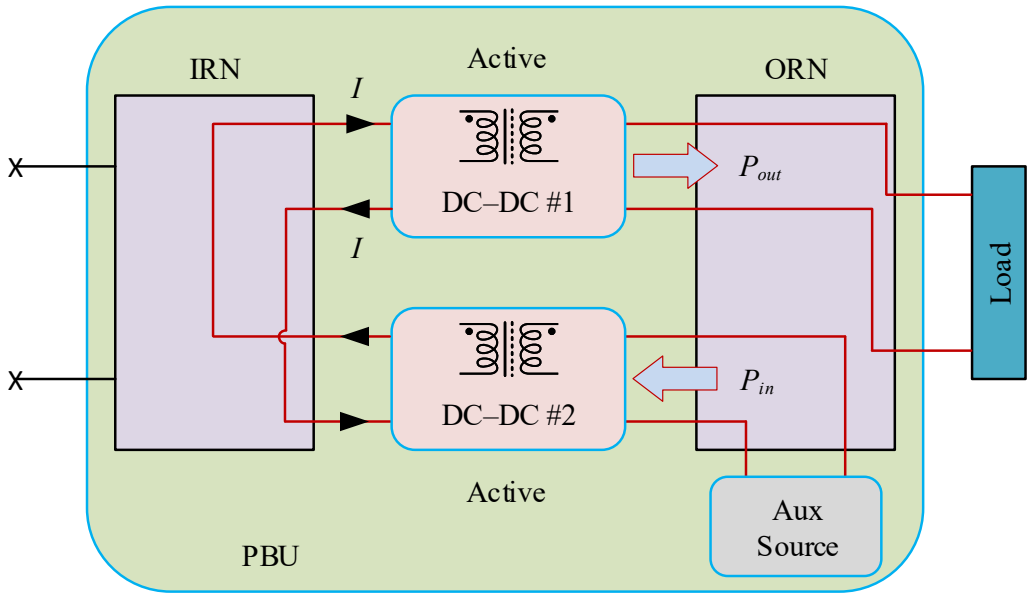


Fig. 7.4: Power flow through PBU from auxiliary source to the load, under cable fault.

conversion and vice versa [49]. In this chapter, a detailed analysis is presented for an isolated DAB LCL-T resonant converter with generalized three angle modulation for the active bridges, having current source input in forward power flow and voltage source input in reverse power flow. It has been shown how the modulation angle need to be set for converters used in constant current distribution systems and how the resonant tank and transformer turn ratio need to be designed for minimization of VA ratings of the converter components. Steady state modeling and analysis is presented in section 7.1 with detailed derivation for AC circuit analysis with generalized three angle modulated DAB LCL-T resonant converter to establish the DC input output relationship, in either direction of power flow. The converter design guideline is established in section 7.2 with modulation strategy, component stress and ZVS requirements. The experimental prototype developed is presented in section 7.3 with results showing pretty good match between analysis and experimentally obtained data. Effect of resonant tank component tolerance on DC output(s), in either direction of power flow, is presented in section 7.4. The load independent output characteristics of DAB LCL-T resonant converter is expanded in section 7.5 to design converter for wide voltage range, with multi-winding transformer and switch network, together minimizing component stress and improving efficiency. Simulation results are presented showing bidirectional operation of this converter over a range of voltage and load.

7.1 Steady State Modeling and Analysis

The DAB LCL-T converter topology is detailed in Fig. 7.5. In forward direction of power flow, power is transferred from DC current source I_g to load R_{L2}, to regulate converter's output DC voltage V_2, as highlighted in blue in Fig. 7.5. Whereas, in reverse direction of power flow, power from DC voltage source V_g flows to R_{L1}, regulating DC current I_1 as its output which is highlighted in brown in Fig. 7.5. In Fig. 7.5, MOSFETs $Q_1 - Q_4$ forms primary side H-bridge which translates DC voltage V_1 into an AC quasi-square wave v_{AB} through symmetrical phase shift modulation, with leg A leading leg B by an angle ϕ_{AB} as shown in Fig. 7.6. Similarly, MOSFETs $Q_5 - Q_8$ forms secondary side H-bridge between DC voltage V_2 and AC quasi-square wave v'_{DE}, modulated by angle ϕ_{DE},

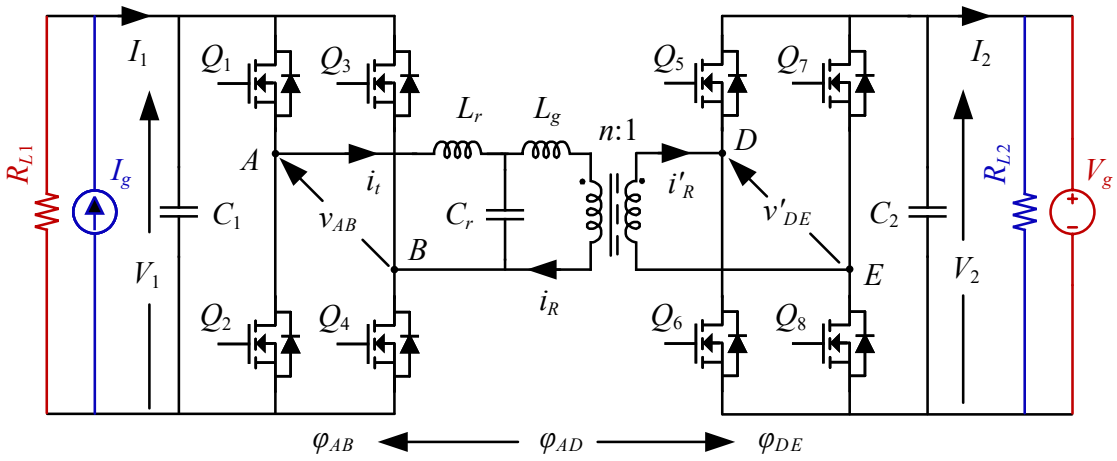


Fig. 7.5: DAB LCL-T resonant DC-DC converter topology.

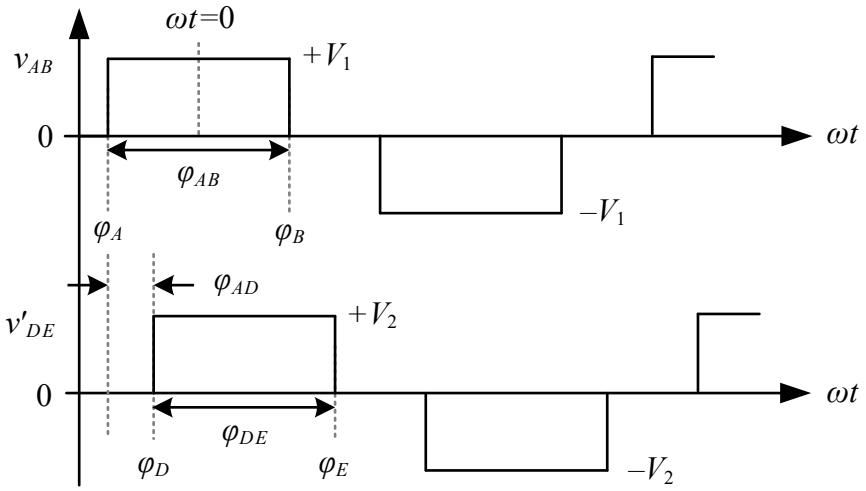


Fig. 7.6: Modulation waveforms of DAB LCL-T resonant converter.

with leg D leading leg E whose time domain waveform is also shown in Fig. 7.6. As shown in Fig. 7.6, the two H-bridges are separated by angle ϕ_{AD}, which is the angular distance between positive rising edge of v_{AB} and v'_{DE}. With reference to the modulation waveform presented in Fig. 7.6, any angle (ϕ_{XY}) used in the analysis is defined as

$$\phi_{XY} = \phi_Y - \phi_X. \tag{7.1}$$

The resonant tank is formed by capacitor C_r and two equal valued inductors L_r and

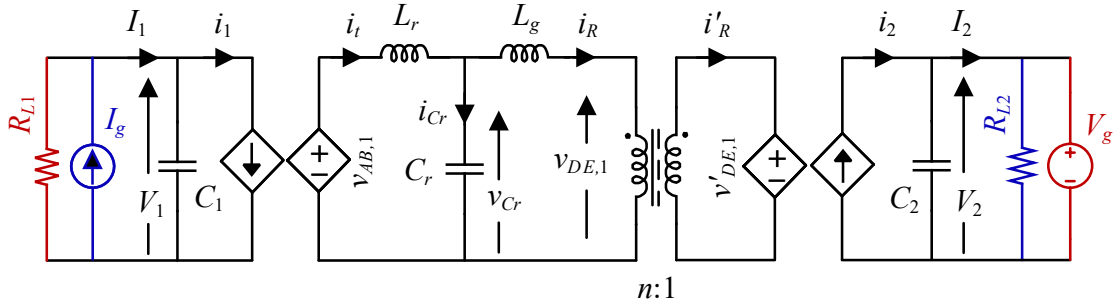


Fig. 7.7: Equivalent circuit of DAB LCL-T resonant converter topology using FHA.

L_g, transferring power between the two H-bridges through a $n:1$ isolation transformer. Capacitors C_1 and C_2 filter out high frequency signals at the DC side of the H-bridges. With fundamental harmonics approximation (FHA) [67], the converter shown in Fig. 7.5 can be redrawn, as the equivalent circuit shown in Fig. 7.7, for the steady state analysis and it is assumed that all the components are ideal and lossless. In the analysis to follow, average value of signal x is represented by $\langle x \rangle$, amplitude of AC side signal x_y is represented by X_y and signal or parameter x is expressed with a prime (x') on the secondary side of the transformer.

7.1.1 AC Equivalent Circuit Analysis

The fundamental AC equivalent circuit of the loaded LCL-T resonant tank, reflected to transformer primary side, is shown in Fig. 7.8 where v_S and i_S represent the source side fundamental AC voltage and current, respectively and v_L and i_L represent load side fundamental AC voltage and current, respectively. In the circuit shown in Fig. 7.8, the load side impedance Z_e is the equivalent complex impedance seen at the AC side of the H-bridge and is derived as follows.

An H-bridge controlled through phase shift modulation angle ϕ_I is shown in Fig. 7.9 whose voltage and current signals on the DC side are V_{DC}, I_{DC} and v_{AC}, i_{AC} on the AC side. The voltage and current waveforms of this H-bridge are also shown in Fig. 7.9 with $v_{AC,1}$ being the fundamental component of v_{AC}. With $v_{AC,1}$ as reference, the AC side quantities of the H-bridge are expressed as

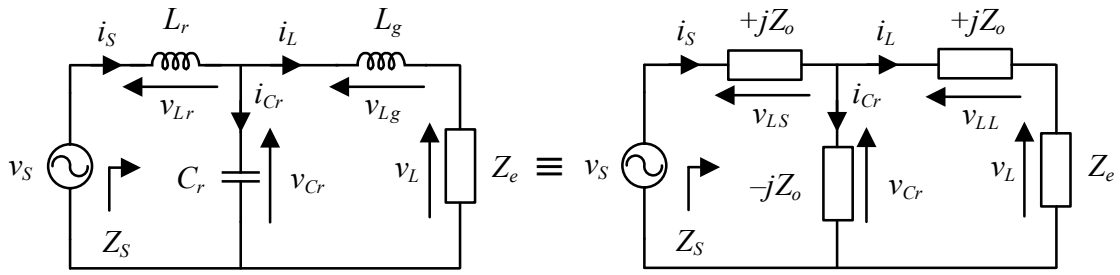


Fig. 7.8: AC equivalent circuit of the loaded resonant tank of DAB LCL-T resonant converter.

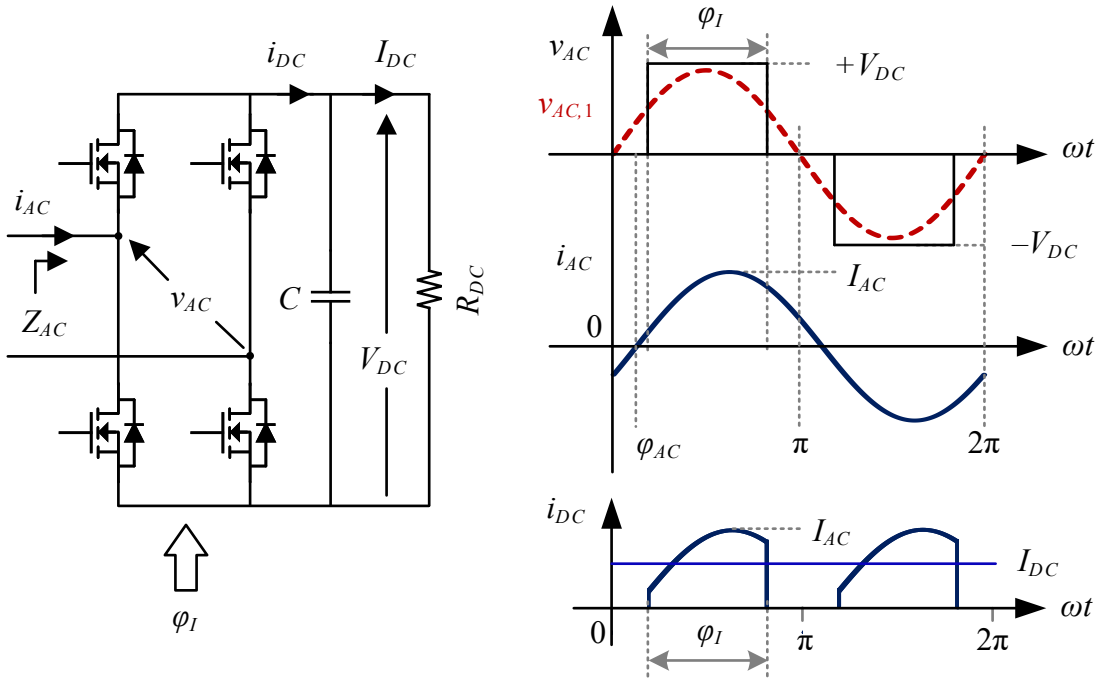


Fig. 7.9: H-bridge with capacitive filter on DC side and its AC and DC side voltage and current waveforms.

$$v_{AC,1}(t) = \frac{4}{\pi} V_{DC} \sin\left(\frac{\phi_I}{2}\right) \sin(\omega_s t), \tag{7.2}$$

$$i_{AC}(t) = I_{AC} \sin(\omega_s t - \phi_{AC}), \tag{7.3}$$

where ϕ_{AC} is the phase shift angle between $v_{AC,1}$ and i_{AC} and I_{AC} is the amplitude of i_{AC} and ω_s is the angular switching frequency of operation. The DC side current I_{DC} can be evaluated from the AC side current as

$$I_{DC} = \frac{1}{\frac{\pi}{\omega_s}} \int_{\frac{\pi}{2}-\frac{\phi_I}{2}}^{\frac{\pi}{2}+\frac{\phi_I}{2}} i_{AC}(t)\, dt = \frac{2}{\pi} I_{AC} \sin\left(\frac{\phi_I}{2}\right) \cos\left(\phi_{AC}\right). \tag{7.4}$$

The impedance seen from the AC side of the H-bridge is expressed as

$$Z_{AC} = |Z_{AC}| \angle \phi_{AC}, \tag{7.5}$$

where $|Z_{AC}|$ is calculated using (7.2) and (7.4) as

$$|Z_{AC}| = \frac{|v_{AC,1}|}{|i_{AC}|} = \frac{8}{\pi^2} R_{DC} \cos\left(\phi_{AC}\right) \sin^2\left(\frac{\phi_I}{2}\right), \tag{7.6}$$

where R_{DC} is the resistance on the DC side of the H-bridge. The impedance in (7.5) can also be expressed in the form given as

$$Z_{AC} = R_{AC} + jX_{AC}, \tag{7.7}$$

where R_{AC} and X_{AC} are the real and imaginary part of Z_{AC}, respectively and are defined as

$$R_{AC} = |Z_{AC}| \cos\left(\phi_{AC}\right), \qquad X_{AC} = |Z_{AC}| \sin\left(\phi_{AC}\right). \tag{7.8}$$

Now, going back to the AC equivalent circuit in Fig. 7.8, the load side AC impedance can be represented as

$$Z_e = |Z_e| \angle \phi_e, \tag{7.9}$$

where ϕ_e is the angle between v_L and i_L. Since the converter's switching frequency (f_s) is same as its resonant frequency (f_o), the circuit in Fig. 7.8 is symmetric and can be analyzed

irrespective of power flow direction from I_g to R_{L2} or from V_g to R_{L1}. The circuit quantities used in the analysis are defined as

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}}, \quad L_g = L_r, \quad Z_o = \sqrt{\frac{L_r}{C_r}}, \quad F = \frac{f_s}{f_o} = 1. \tag{7.10}$$

From the equivalent circuit of Fig. 7.8, the input impedance of the loaded tank, seen from the source side can be derived as

$$Z_S = jZ_o + \frac{-jZ_o\left(Z_e + jZ_o\right)}{-jZ_o + Z_e + jZ_o} = \frac{Z_o^2}{|Z_e|}\angle\left(-\phi_e\right). \tag{7.11}$$

Using Z_S from (7.11), the AC source current i_S can be found as

$$i_S = \frac{v_S}{Z_S} = V_S\frac{|Z_e|}{Z_o^2}\angle\phi_e, \tag{7.12}$$

where V_S is the amplitude of v_S, which is also taken as the reference AC voltage. The load side AC current i_L can be derived as

$$i_L = \frac{V_S}{Z_o}\angle\left(-\frac{\pi}{2}\right). \tag{7.13}$$

The voltage across and current through resonant capacitor C_r can be derived as

$$v_{Cr} = V_L\cos\left(\phi_e\right)\sqrt{1+\frac{1}{Q_z^2}}\angle\left(-\tan^{-1}Q_z\right), \tag{7.14}$$

$$i_{Cr} = \frac{V_L}{Z_o}\cos\left(\phi_e\right)\sqrt{1+\frac{1}{Q_z^2}}\angle\tan^{-1}\left(\frac{1}{Q_z}\right), \tag{7.15}$$

where V_L is the amplitude of v_L and Q_z is defined as

$$Q_z = \frac{|Z_e|\cos\left(\phi_e\right)}{Z_o + |Z_e|\sin\left(\phi_e\right)}. \tag{7.16}$$

From the derivations in (7.12) – (7.15), the phasor diagram of the AC equivalent circuit in Fig. 7.8 can be drawn as shown in Fig. 7.10, with v_S taken as reference and ϕ_{SL} defined

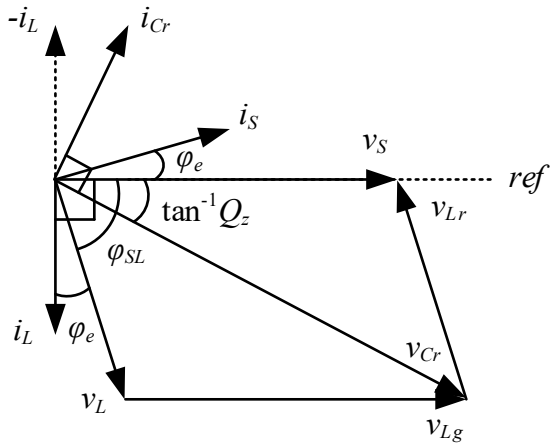


Fig. 7.10: Phasor diagram for the AC signals from this equivalent circuit of Fig. 7.8.

as the phase angle between v_S and v_L and is related to ϕ_e by

$$\phi_e = \frac{\pi}{2} - \phi_{SL}. \tag{7.17}$$

The source and load active power in the circuit of Fig. 7.8 are expressed as

$$P_S = \frac{V_S^2}{2}\frac{|Z_e|}{Z_o^2}\cos(\phi_e), \tag{7.18}$$

$$P_L = \frac{V_L^2}{2|Z_e|}\cos(\phi_e). \tag{7.19}$$

The power transfer from source to load, through the resonant tank, in terms of source and load side AC voltages can be given as

$$P_T = \frac{V_S V_L}{2Z_o}\cos(\phi_e). \tag{7.20}$$

From (7.20), the maximum power transfer for a given resonant tank will occur with maximum values of V_S and V_L and at $\phi_e = 0$ and this value can be given in terms of DC voltage(s) V_1 and V_2 as

$$|P_{max}| = \frac{8n}{\pi^2}\frac{V_1 V_2}{Z_o}, \tag{7.21}$$

and the set of modulation angle(s) at which maximum power transfer occurs is given as

$$\phi_{AB} = \pi, \quad \phi_{DE} = \pi, \quad \left|\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right| = \frac{\pi}{2}. \tag{7.22}$$

From the analysis and phasor diagram of the AC equivalent circuit presented in this section, the following key properties of LCL-T resonant tank can be observed

1. For power transfer from the source to the load, source voltage (v_S) will lead the load voltage (v_L).
2. The load current (i_L) always lags source voltage (v_S) by 90°, for any load impedance.
3. An inductive impedance on the load side (i_L lagging v_L) will reflect as capacitive on the source side (i_S leading v_S) and vice versa.

7.1.2 DC Input – Output Relationship

From the analysis of the AC resonant circuit established in previous section, the relationship of input – output DC quantities can now be derived from the equivalent circuit modeled in Fig. 7.7, starting with the forward power transfer. The amplitude of the fundamental component of AC voltage(s) from the two H-bridges are given as

$$V_{AB,1} = \frac{4}{\pi} V_1 \sin\left(\frac{\phi_{AB}}{2}\right), \tag{7.23}$$

$$V_{DE,1} = \frac{4n}{\pi} V_2 \sin\left(\frac{\phi_{DE}}{2}\right). \tag{7.24}$$

For forward power flow, substituting (7.23) and (7.24) in to (7.18) and (7.19) and equating the source and load side power the following relationship is established

$$\frac{V_1 \sin\left(\frac{\phi_{AB}}{2}\right)}{nV_2 \sin\left(\frac{\phi_{DE}}{2}\right)} = \frac{Z_o}{|Z_e|}. \tag{7.25}$$

Using (7.6), the magnitude of AC load impedance is given as

$$|Z_e| = \frac{8n^2}{\pi^2} R_{L2} \cos(\phi_e) \sin^2\left(\frac{\phi_{DE}}{2}\right), \tag{7.26}$$

where R_{L2} is the load resistance on the DC output side. From the circuit in Fig. 7.7, the DC power input (P_{in}) and DC power output (P_{out}) can be given as

$$P_{in} = V_1 I_1, \qquad P_{out} = \frac{V_2^2}{R_{L2}}. \tag{7.27}$$

With lossless power conversion, equating the input and output DC power from (7.27), the input DC voltage can be expressed as

$$V_1 = \frac{V_2^2}{I_1 R_{L2}}. \tag{7.28}$$

Substituting V_1 from (7.28) and $|Ze|$ from (7.26) into (7.25), the expression of V_2 for forward power flow can be derived as

$$V_2 = \frac{\pi^2}{8n} \frac{I_1 Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right) \sin\left(\frac{\phi_{DE}}{2}\right) \cos(\phi_e)}. \tag{7.29}$$

The value of ϕ_e can be found from (7.17) with ϕ_{SL} evaluated for forward power (ϕ_{SL_F}), from the modulation waveform in Fig. 7.17 and is given as

$$\phi_{SL\_F} = \phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}. \tag{7.30}$$

Finally, substituting (7.30) and (7.17) into (7.29), the DC output voltage V_2 can be expressed as

$$V_2 = \frac{\pi^2}{8n} \frac{I_1 Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right) \sin\left(\frac{\phi_{DE}}{2}\right) \sin\left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)}. \tag{7.31}$$

From (7.31), it can be observed that with $I_1 = I_g$ *i.e.* with constant DC current source, the output DC voltage of the converter becomes independent of load. The input voltage, however, will be dependent on load and is found out by plugging in V_2 from (7.31) in (7.28) and is given by

$$V_1 = \frac{I_1}{R_{L2}} \left[\frac{\pi^2}{8n} \frac{Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right) \sin\left(\frac{\phi_{DE}}{2}\right) \sin\left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)} \right]^2. \tag{7.32}$$

The DC input current to the converter (I_1) and AC input current to the resonant tank (i_t) are related through the primary side H-bridge by

$$I_1 = \langle i_1 \rangle = \frac{2I_t}{\pi} \sin\left(\frac{\phi_{AB}}{2}\right) \cos\left(\phi_e\right), \tag{7.33}$$

where I_t is the amplitude of i_t and average value of current i_1 is represented by $\langle i_1 \rangle$. For forward power flow, $I_1 = I_g$ and thus the tank input current can be written from (7.33) and using (7.12) as

$$i_t = \frac{\pi}{2} \frac{I_g}{\sin\left(\frac{\phi_{AB}}{2}\right) \cos\left(\phi_e\right)} \angle \phi_e. \tag{7.34}$$

Similarly, the load side tank AC current i_R can be expressed, using the phase information from (7.13), as

$$i_R = \frac{\pi}{2n} \frac{V_2}{R_{L2} \sin\left(\frac{\phi_{AB}}{2}\right) \cos\left(\phi_e\right)} \angle \left(-\frac{\pi}{2}\right). \tag{7.35}$$

Following similar approach, the equations of signals for reverse power flow can be derived which are tabulated in Table 7.1 and Table 7.2, along with the equations for forward power flow. The phasor diagram for the tank AC signals are presented in Fig. 7.11, for both forward and reverse power flow, taking $v_{AB,1}$ and $v_{DE,1}$ taken as reference, respectively.

Table 7.1: DAB LCL-T resonant converter – DC quantities

Quantity	Forward Power	Reverse Power
Source	I_g	V_g
Load (R_L)	R_{L2}	R_{L1}
V_1	$\frac{I_g}{R_{L2}}\left[\frac{\pi^2}{8n}\frac{Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right)\sin\left(\frac{\phi_{DE}}{2}\right)\sin\left(\phi_{AD}-\frac{\phi_{AB}}{2}+\frac{\phi_{DE}}{2}\right)}\right]^2$	$\lvert I_1\rvert R_{L1}$
I_1	I_g	$\frac{8}{\pi^2}\frac{nV_g}{Z_o}\sin\left(\frac{\phi_{AB}}{2}\right)\sin\left(\frac{\phi_{DE}}{2}\right)\sin\left(\phi_{AD}-\frac{\phi_{AB}}{2}+\frac{\phi_{DE}}{2}\right)$
V_2	$\frac{\pi^2}{8n}\frac{I_g Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right)\sin\left(\frac{\phi_{DE}}{2}\right)\sin\left(\phi_{AD}-\frac{\phi_{AB}}{2}+\frac{\phi_{DE}}{2}\right)}$	V_g
I_2	$\frac{V_2}{R_{L2}}$	$-R_{L1}V_g\left[\frac{8n}{\pi^2 Z_o}\sin\left(\frac{\phi_{AB}}{2}\right)\sin\left(\frac{\phi_{DE}}{2}\right)\sin\left(\phi_{AD}-\frac{\phi_{AB}}{2}+\frac{\phi_{DE}}{2}\right)\right]^2$

Table 7.2: DAB LCL-T resonant converter – AC quantities

Quantity	Forward Power	Reverse Power
ϕ_e	$\frac{\pi}{2} - \left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)$	$\frac{\pi}{2} + \left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)$
Z_e	$\frac{8n^2}{\pi^2} R_{L2} \cos(\phi_e) \sin^2\left(\frac{\phi_{DE}}{2}\right) \angle \phi_e$	$\frac{8}{\pi^2} R_{L1} \cos(\phi_e) \sin^2\left(\frac{\phi_{AB}}{2}\right) \angle \phi_e$
v_S	$v_{AB,1} = \frac{4}{\pi} V_1 \sin\left(\frac{\phi_{AB}}{2}\right) \angle 0$	$v_{DE,1} = \frac{4n}{\pi} V_g \sin\left(\frac{\phi_{DE}}{2}\right) \angle 0$
v_L	$v_{DE,1} = \frac{4n}{\pi} V_2 \sin\left(\frac{\phi_{DE}}{2}\right) \angle -\left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)$	$v_{AB,1} = \frac{4}{\pi} V_1 \sin\left(\frac{\phi_{AB}}{2}\right) \angle \left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)$
i_S	$i_t = \frac{\pi}{2} \frac{I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)\cos(\phi_e)} \angle \phi_e$	$i_R = \frac{4}{\pi} \lvert I_1 \rvert \frac{R_{L1}}{Z_o} \sin\left(\frac{\phi_{AB}}{2}\right) \angle (\pi + \phi_e)$
i_L	$i_R = \frac{\pi}{2n} \frac{V_2}{R_{L2} \sin\left(\frac{\phi_{DE}}{2}\right)\cos(\phi_e)} \angle -\frac{\pi}{2}$	$i_t = \frac{4n}{\pi} \frac{V_g}{Z_o} \sin\left(\frac{\phi_{DE}}{2}\right) \angle \frac{\pi}{2}$
v_{Cr}	$\frac{4n}{\pi} V_2 \sin\left(\frac{\phi_{DE}}{2}\right) \cos(\phi_e) \sqrt{1 + \frac{1}{Q_z^2}} \angle \left(-\tan^{-1} Q_z\right)$	$\frac{4}{\pi} \lvert I_1 \rvert R_{L1} \sin\left(\frac{\phi_{AB}}{2}\right) \cos(\phi_e) \sqrt{1 + \frac{1}{Q_z^2}} \angle \left(-\tan^{-1} Q_z\right)$
i_{Cr}	$\frac{4n}{\pi} \frac{V_2}{Z_o} \sin\left(\frac{\phi_{DE}}{2}\right) \cos(\phi_e) \sqrt{1 + \frac{1}{Q_z^2}} \angle \tan^{-1}\left(\frac{1}{Q_z}\right)$	$\frac{4}{\pi} \lvert I_1 \rvert \frac{R_{L1}}{Z_o} \sin\left(\frac{\phi_{AB}}{2}\right) \cos(\phi_e) \sqrt{1 + \frac{1}{Q_z^2}} \angle \tan^{-1}\left(\frac{1}{Q_z}\right)$

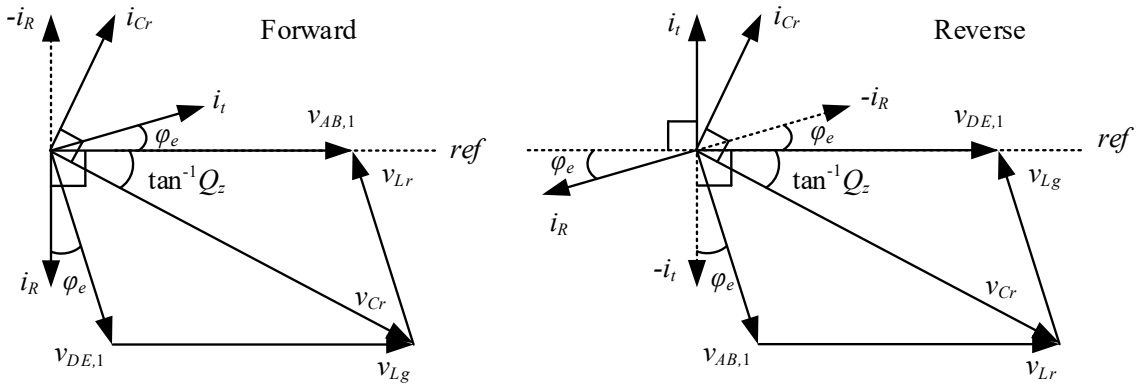


Fig. 7.11: Phasor diagram for the AC signals for forward and reverse power flow.

The power flow direction from primary to secondary and vice versa is dependent of the phase angle (ϕ_{PS}) between $v_{AB,1}$ and $v_{DE,1}$, which can be found out from the modulating waveform shown in Fig. 7.6 and is given by

$$\phi_{PS} = \phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}. \tag{7.36}$$

For forward power flow, where I_1 and I_2 are positive, ϕ_{PS} is within the range $[0,\ \pi]$ and in reverse power flow, where I_1 and I_2 are both negative, ϕ_{PS} is within the range $[-\pi,\ 0]$. Thus, the relationship between ϕ_{SL} and ϕ_{PS} is given by

$$\phi_{SL} = |\phi_{PS}| = \left|\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right|, \tag{7.37}$$

and from (7.17) the relationship between ϕ_e and modulation angles is given by

$$\phi_e = \frac{\pi}{2} - |\phi_{PS}| = \frac{\pi}{2} - \left|\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right|. \tag{7.38}$$

The variation of ϕ_{SL} and ϕ_e are plotted against ϕ_{PS} in Fig. 7.12 along with the variation in normalized power (P_{PS_norm}) from primary to secondary, normalized using (7.21), for $\phi_{AB} = \phi_{DE} = \pi$, which is defined as

$$P_{PS\_norm} = \sin(\phi_{PS}). \tag{7.39}$$

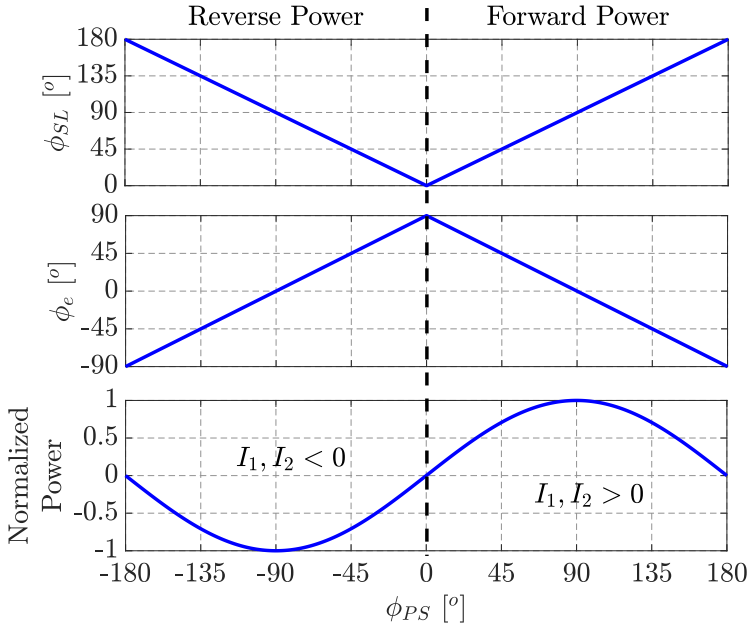


Fig. 7.12: Variation of ϕ_{SL}, ϕ_e and normalized power (P_{PS_norm}) over the range of ϕ_{PS}, for forward and reverse power flow.

7.2 Design of the Converter

From the analysis presented in the previous section, converter gain for forward (G_F) and reverse (G_R) power flow are expressed as

$$G_F = \frac{V_2}{I_g} = \frac{\frac{\pi^2}{8n} Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right) \sin\left(\frac{\phi_{DE}}{2}\right) \sin\left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)}, \tag{7.40}$$

$$G_R = \frac{I_1}{V_g} = \frac{\sin\left(\frac{\phi_{AB}}{2}\right) \sin\left(\frac{\phi_{DE}}{2}\right) \sin\left(\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right)}{\frac{\pi^2}{8n} Z_o}. \tag{7.41}$$

It can be observed from (7.40) and (7.41) that the magnitude(s) of the gain(s) are reciprocal to each other, *i.e.*

$$|G_F| = \left|\frac{1}{G_R}\right|, \tag{7.42}$$

which means that for a given resonant tank (Z_o) and transformer (n) the input to output ratio can be achieved with same set of modulation angle $\left[\phi_{AB}, \phi_{DE}, \left|\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right|\right]$,

with source AC voltage leading the load side voltage. And thus, with a designed modulation angle set, the tank and transformer can be designed irrespective of power flow direction.

7.2.1 Modulation Angle

In forward power flow, when the converter is fed from a DC current source, a non-zero ϕ_e makes the input impedance seen by the source H-bridge either inductive or capacitive. This brings in a restriction on minimum power operation of the converter for which the output can be regulated [81], [100]. So, to eliminate such limitation, ϕ_e is made to be zero which, from (7.38) gives

$$\left|\phi_{AD} - \frac{\phi_{AB}}{2} + \frac{\phi_{DE}}{2}\right| = \frac{\pi}{2}. \tag{7.43}$$

Now, with the condition established in (7.43), control of output can be done through ϕ_{AB} or ϕ_{DE}. Since the secondary side of this converter has higher current compared to the primary side, in this application, ϕ_{DE} is set to its maximum value of 180° to keep the device current stress low for the secondary H-bridge and control of the converter is done through ϕ_{AB}.

Finally, the nominal operating value of ϕ_{AB} is chosen to be 120° which eliminates any triplen harmonic content out of the primary H-bridge [60]. This also keeps good margin from maximum possible value of ϕ_{AB} as 180°, for transients. With known ϕ_{AB} and ϕ_{DE}, ϕ_{AD} is found out using (7.43) and the set of modulation angles for forward power is given as

$$\phi_{AB} = 120°, \qquad \phi_{DE} = 180°, \qquad \phi_{AD} = \frac{\phi_{AB}}{2}, \tag{7.44}$$

whereas, for reverse power, it is given by

$$\phi_{AB} = 120°, \qquad \phi_{DE} = 180°, \qquad \phi_{AD} = \frac{\phi_{AB}}{2} - 180°. \tag{7.45}$$

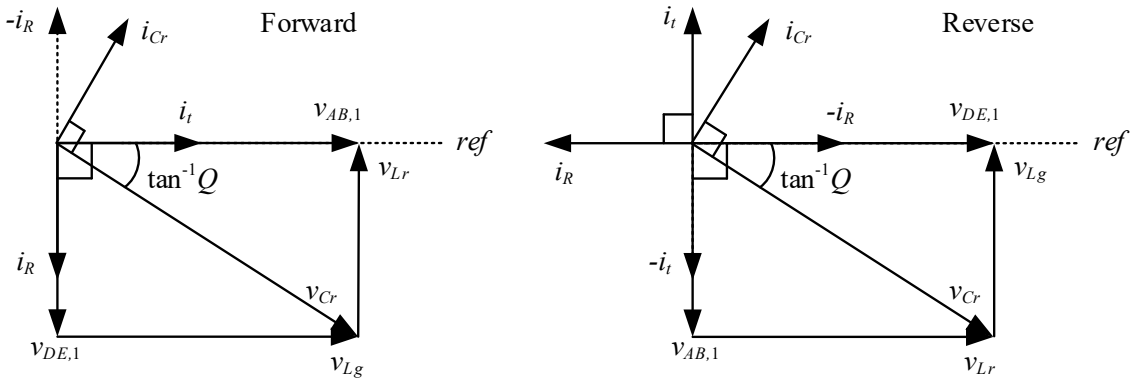


Fig. 7.13: Phasor diagram for the tank AC signals in forward and reverse power flow, at the operating condition.

7.2.2 Derivation of Converter Signals

With the selected operating set of modulating angles in (7.44) and (7.45), the resultant signals of the converter from Table 7.1 and Table 7.2 can be simplified to the signals tabulated in Table 7.3 where the terms Z_e and Q_z are modified to R_e and Q, respectively. From (7.16), Q is expressed as

$$Q = \frac{R_e}{Z_o}. \tag{7.46}$$

The AC signal expressions presented in Table 7.3 are referenced with their respective source voltage(s), *i.e.* $v_{AB,1}$ for forward power and $v_{DE,1}$ for reverse power. The phasor diagram of the tank AC signals at the operating condition is shown in Fig. 7.13. From the expressions of the tank AC signals in Table 7.3 and phasor diagram presented in Fig. 7.13, it can be observed that at the selected operating condition, both the H-bridges now operate at unity power factor (UPF), in terms of their fundamental AC voltage and current. Also, from these derivations, rms current(s) in the tank components can be calculated from their signal amplitude which are used to calculate the VA of the tank to design the resonant tank and transformer turn ratio for lowest VA rating.

Table 7.3: DAB LCL-T resonant converter – signals at the operating condition

Quantity	Forward Power	Reverse Power
V_1	$\frac{I_g}{R_{L2}}\left[\frac{\pi^2}{8n}\frac{Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right)}\right]^2$	$\lvert I_1\rvert R_{L1}$
I_1	I_g	$-\frac{8n}{\pi^2}\frac{V_g}{Z_o}\sin\left(\frac{\phi_{AB}}{2}\right)$
V_2	$\frac{\pi^2}{8n}\frac{I_g Z_o}{\sin\left(\frac{\phi_{AB}}{2}\right)}$	V_g
I_2	$\frac{V_2}{R_{L2}}$	$-R_{L1}V_g\left[\frac{8n}{\pi^2 Z_o}\sin\left(\frac{\phi_{AB}}{2}\right)\right]^2$
R_e	$\frac{8n^2}{\pi^2}R_{L2}$	$\frac{8}{\pi^2}R_{L1}\sin^2\left(\frac{\phi_{AB}}{2}\right)$
v_S	$v_{AB,1}=\frac{4}{\pi}V_1\sin\left(\frac{\phi_{AB}}{2}\right)\angle 0$	$v_{DE,1}=\frac{4n}{\pi}V_g\angle 0$
v_L	$v_{DE,1}=\frac{4n}{\pi}V_2\angle -\frac{\pi}{2}$	$v_{AB,1}=\frac{4}{\pi}V_1\sin\left(\frac{\phi_{AB}}{2}\right)\angle -\frac{\pi}{2}$
i_S	$i_t=\frac{\pi}{2}\frac{I_g}{\sin\left(\frac{\phi_{AB}}{2}\right)}\angle 0$	$i_R=\frac{\pi}{2}\frac{\lvert I_1\rvert}{\sin\left(\frac{\phi_{AB}}{2}\right)}Q\angle\pi$
i_L	$i_R=\frac{4n}{\pi}\frac{V_2}{QZ_o}\angle -\frac{\pi}{2}$	$i_t=\frac{4n}{\pi}\frac{V_g}{Z_o}\angle\frac{\pi}{2}$
v_{Cr}	$\frac{4n}{\pi}V_2\sqrt{1+\frac{1}{Q^2}}\angle\left(-\tan^{-1}Q\right)$	$\frac{\pi}{2}\frac{Z_o\lvert I_1\rvert}{\sin\left(\frac{\phi_{AB}}{2}\right)}\sqrt{1+Q^2}\angle\left(-\tan^{-1}Q\right)$
i_{Cr}	$\frac{4n}{\pi}\frac{V_2}{Z_o}\sqrt{1+\frac{1}{Q^2}}\angle\tan^{-1}\left(\frac{1}{Q}\right)$	$\frac{\pi}{2}\frac{\lvert I_1\rvert}{\sin\left(\frac{\phi_{AB}}{2}\right)}\sqrt{1+Q^2}\angle\tan^{-1}\left(\frac{1}{Q}\right)$

7.2.3 Design of Resonant Tank and Transformer

The VA of the resonant tank (S_{Tank}) can be expressed in terms of rms current through L_r, L_g and C_r as

$$S_{Tank} = \left(I_{t,rms}^2 + I_{R,rms}^2 + I_{Cr,rms}^2\right) Z_o. \tag{7.47}$$

Since the current through the resonant capacitor is phasor subtraction of i_t and i_R which are in quadrature to each other, the rms currents through the tank elements can be related as

$$I_{Cr,rms} = \sqrt{I_{t,rms}^2 + I_{R,rms}^2}. \tag{7.48}$$

Substituting (7.48) in (7.47) the tank VA is evaluated as

$$S_{Tank} = 2\left(I_{t,rms}^2 + I_{R,rms}^2\right) Z_o. \tag{7.49}$$

Using the expressions of i_t, i_R and V_2 from Table 7.3 and Q from (7.46), the tank VA expression from (7.49) can be further simplified to

$$S_{Tank} = 2\left(Q + \frac{1}{Q}\right) P_{load}, \tag{7.50}$$

where P_{load} represents the output load. The expression from (7.50) is normalized with respect to P_{load} and expressed as

$$S_{Tank\_norm} = 2\left(Q + \frac{1}{Q}\right). \tag{7.51}$$

Now, from the expression of V_2 from Table 7.3, Z_o can be expressed as

$$Z_o = \frac{8n}{\pi^2} \frac{V_2 \sin\left(\frac{\phi_{AB}}{2}\right)}{I_g}, \tag{7.52}$$

and substituting this value in (7.46), Q can be expressed as

$$Q = \frac{nI_g V_2}{P_{load} \sin\left(\frac{\phi_{AB}}{2}\right)}. \tag{7.53}$$

The tank VA rating is found under the maximum load condition ($P_{load} = P_{load\_max}$) and from (7.51) it can be seen that the normalized VA of the tank would be minimum when $Q = 1$, under maximum load. Plugging $Q = 1$ in (7.53), the optimum value of transformer turns ratio (n_{opt}) can be expressed as

$$n_{opt} = \frac{P_{load\_max} \sin\left(\frac{\phi_{AB}}{2}\right)}{V_2 I_g}. \tag{7.54}$$

Using (7.54) in (7.52), Z_o can be evaluated from which the values of resonant tank components can be calculated as

$$L_r = \frac{Z_o}{2\pi f_o} = \frac{Z_o}{2\pi f_s}, \tag{7.55}$$

$$C_r = \frac{1}{2\pi f_o Z_o} = \frac{1}{2\pi f_s Z_o}, \tag{7.56}$$

$$L_g = L_r = \frac{Z_o}{2\pi f_s}. \tag{7.57}$$

The normalized VA rating of the tank is plotted against transformer turn ratio (n) in Fig. 7.14 where it can be seen that the minimum value of tank VA occurs at $n = n_{opt}$.

7.2.4 ZVS Assistance

With the H-bridges of the converter designed to operate at UPF (FHA), all the MOSFETs will not have zero voltage switching (ZVS) and hence ZVS assisting circuits are needed. The secondary H-bridge operates at UPF with $\phi_{DE} = 180°$, resulting in zero current turn on and turn off, in either direction of power flow. So, a fixed inductor (L_{zvs_sec}) based passive ZVS assisting circuit, as presented in section 3.1, is used across leg D and leg E, since the bridge operates with fixed DC voltage V_2. On the primary side H-bridge, which operates with $\phi_{AB} = 180°$, tank current (i_t) does ZVS for MOSFETs in lagging

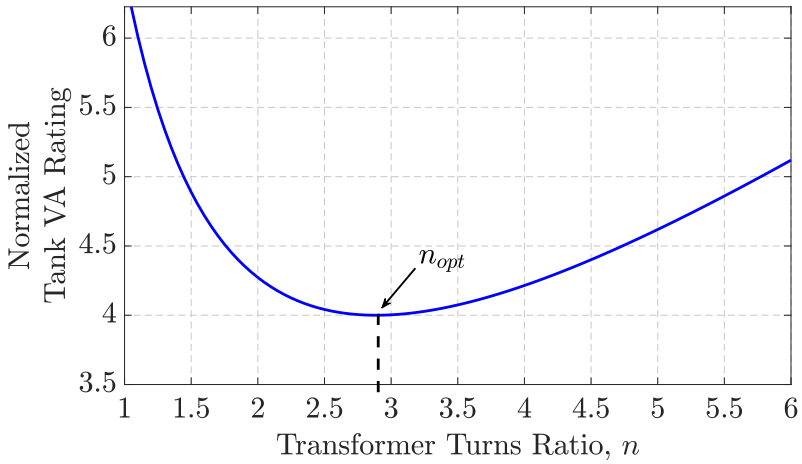


Fig. 7.14: Normalized VA rating of the tank for various transformer turn ratio (n).

leg, for forward power and leading leg, for reverse power. For the other leg in the primary bridge, an active ZVS assisting circuit with an inductor (L_{zvs_pri}) and a half-bridge, as presented in section 3.2.1, is used to achieve ZVS over the wide load range, since the DC voltage (V_1) for primary bridge varies with load.

7.3 Experimental Results

A prototype hardware has been built to verify the analysis presented in the previous sections whose details are presented in Table 7.4 and the test setup is shown in Fig. 7.15. DC blocking capacitors (C_{DC_pri} and C_{DC_sec}) are used in both primary and secondary side H-bridges to block any DC component of voltage arriving out of the H-bridges due to any component mismatch.

For forward power transfer, the converter is tested with 1 A constant DC current source with modulation angle set from (7.44) for a load range of 50 W to 500 W and the steady state waveforms of the H-bridge voltage and current are shown in Fig. 7.16(a) and Fig. 7.16(b) for a load of 50 W and 500 W, respectively. Similar set of waveforms are shown for reverse power flow from a 150 V constant DC voltage source, with modulation angle set from (7.45), in Fig. 7.17(a) and Fig. 7.17(b), for a load of 50 W and 500 W, respectively. In Fig. 7.16 and Fig. 7.17, CH1 (deep blue) shows the waveform of v_{AB}, CH2 (cyan) is for i_t, CH3 (purple) is for v'_{DE} and current i'_R is shown in CH4 (green). It can be seen from these

Table 7.4: Details of the bidirectional LCL-T resonant converter

Component / Parameter	Part Number / Value
I_g / $\|I_1\|$ [A]	1
V_2 / V_g [V]	150
f_s [kHz]	250
P_{load} [W]	50 – 500
L_r [µH]	194.4
C_r [pF]	2085
L_g [µH]	194.4
n	2.9
$Q_1 - Q_4$	C2M1000170D (2 in parallel)
C_{DC_pri} [µF]	0.23
L_{zvs_pri} [µH]	50
$Q_5 - Q_8$	IXFQ72N20X3
C_{DC_sec} [µF]	6.4
L_{zvs_sec} [µH]	60

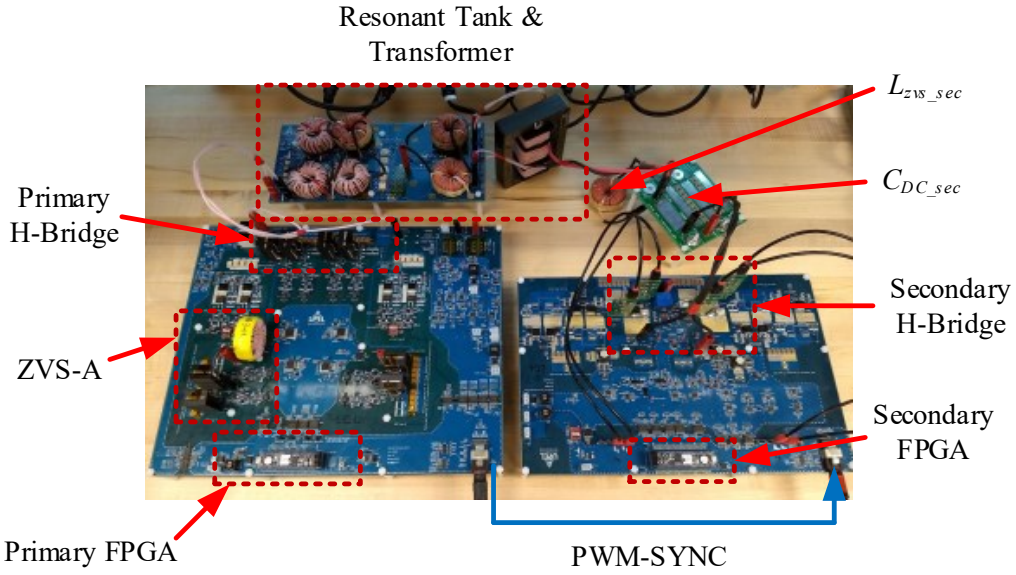
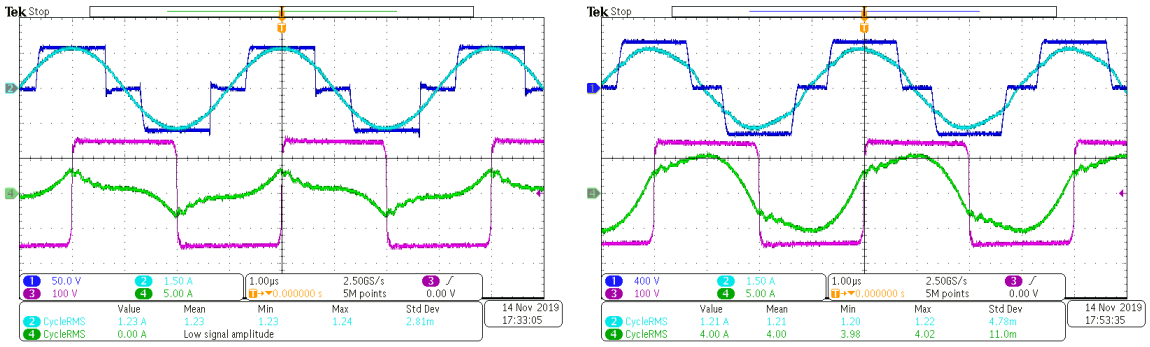
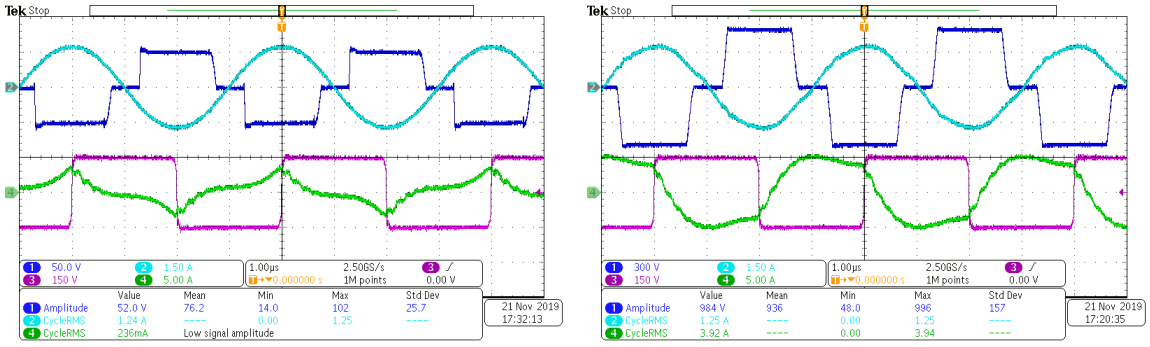


Fig. 7.15: Photograph of the hardware test setup.



(a) (b)

Fig. 7.16: Steady state operating waveforms (a) at 50 W and (b) at 500 W load for forward power transfer from 1 A current source (I_g) with $\phi_{AB} = 120°$, $\phi_{DE} = 180°$ and $\phi_{AD} = 60°$. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v'_{DE}, CH4 (green): i'_R.



(a) (b)

Fig. 7.17: Steady state operating waveforms (a) at 50 W and (b) at 500 W load for reverse power transfer from 150 V voltage source (V_g) with $\phi_{AB} = 120°$, $\phi_{DE} = 180°$ and $\phi_{AD} = -120°$. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v'_{DE}, CH4 (green): i'_R.

waveforms that for forward power transfer, fundamental components of v_{AB} and i_t are in phase and v'_{DE} and i'_R are in phase with v_{AB} leading v'_{DE} by 90°, as per the derivations and phasor diagram presented in Table 7.3 and Fig. 7.13, respectively. Whereas, in reverse power transfer, the corresponding pair of voltage and current are 180° out of phase with v'_{DE} leading v_{AB} by 90°, conforming to the derivations and phasor relationship presented in Table 7.3 and Fig. 7.13, respectively.

The steady state DC output voltage (V_2), with fixed control angle of $\phi_{AB} = 120°$, is plotted over the load range in Fig. 7.18(a), for forward power transfer. Whereas, the DC output current ($|I_1|$) with fixed control angle of $\phi_{AB} = 120°$ is plotted in Fig. 7.18(b),

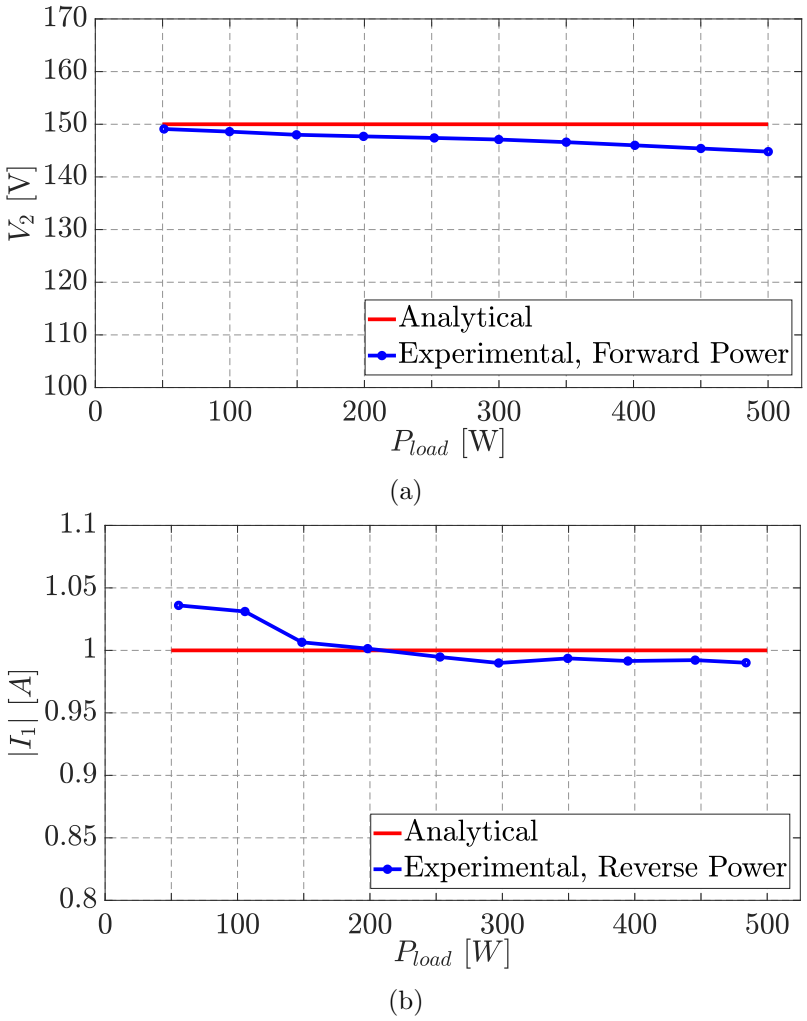
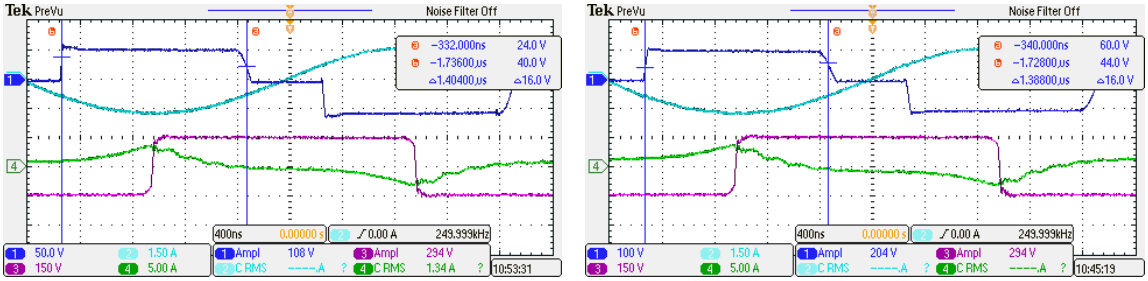


Fig. 7.18: Steady state DC output versus load power (P_{load}) – (a) voltage (V_2) in forward power and (b) current ($|I_1|$) in reverse power . Red: result from analysis, blue: experimental result.

for reverse power transfer operation. In Fig. 7.18, the red line(s) represent the analytical reference and the blue line(s) show the experimental data. It can be seen from these plot(s) that the DC output is almost constant over 10:1 load range, making them fairly independent of load. The small variation in the DC output is within around 3 % for forward power and within 4 % for reverse power transfer operation which, in part, is due to non-idealities such as ESR of components etc., which were ignored in the analysis.

The other reason for increased output at light load is due to change in effective operating ϕ_{AB}. In the primary H-bridge, the voltage transition in leading leg (positive rising edge



(a) (b)

Fig. 7.19: Zoomed in steady state operating waveforms (a) at 50 W and (b) at 100 W load for reverse power transfer from 150 V voltage source (V_g) showing higher effective ϕ_{AB}. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v'_{DE}, CH4 (green): i'_R.

of v_{AB}) in reverse power happens swiftly owing to low magnitude of V_1 under light load conditions which can be seen in the waveform of v_{AB} in Fig. 7.19(a) and Fig. 7.19(b), for 50 W and 100 W load, respectively. This makes the effective value of ϕ_{AB} to be higher than controller command, resulting in slightly higher output current. In Fig. 7.19(a), the effective $\phi_{AB} = 127°$ and in Fig. 7.19(b), the effective $\phi_{AB} = 125°$. Similar situation would take place for lagging leg in forward power transfer lowering the effective value of ϕ_{AB} and thus increasing the DC output voltage at light load.

Steady state DC output current ($|I_1|$) in reverse power, with the controller adjusted $\phi_{AB} = 120°$, over the load range, is plotted in black in Fig. 7.20 alongside the results shown in Fig. 7.18(b) with controller commanded $\phi_{AB} = 120°$ in blue. It can be seen from the black line in Fig. 7.20 that with adjusted $\phi_{AB} = 120°$, the output current stays fairly constant – within 2 % variation over the entire load range.

In practice, the converter needs to regulate its output over the load range and hence the variation of control angle (ϕ_{AB}) needed to keep the output regulated at the desired value is also checked for this converter operating in both directions of power flow. The experimental data is plotted in Fig. 7.21 where the blue plot is for forward power transfer, black plot is for reverse power transfer and red line shows the analytical reference. The experimental data range of ϕ_{AB} is within the control boundary of the converter and the variation is only within 8°, over the entire load range, for either direction of power flow.

The tank AC signals are captured for both direction of power flow and are shown in

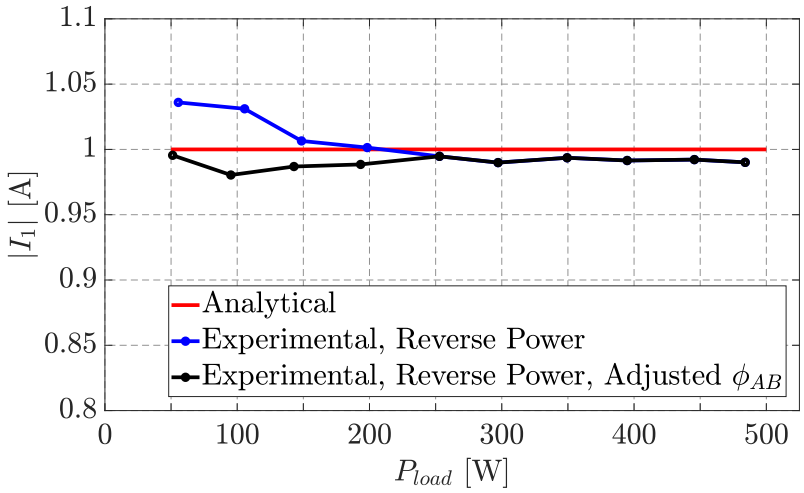


Fig. 7.20: Steady state DC output current ($|I_1|$) in reverse power, versus load power (P_{load}). Red: result from analysis, blue: experimental result with controller commanded $\phi_{AB} = 120°$, black: experimental result with controller adjusted $\phi_{AB} = 120°$.

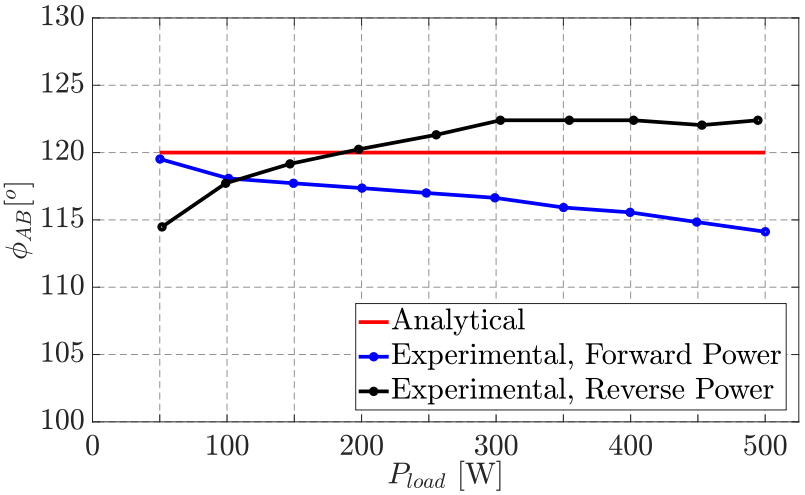
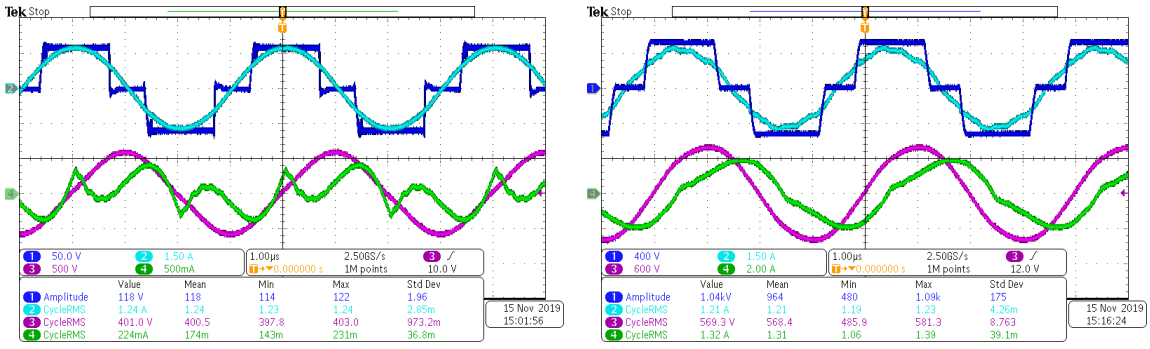


Fig. 7.21: Variation in control angle (ϕ_{AB}) over the range of load power (P_{load}). Red: analytical value, blue: regulating output voltage at 150 V for forward power flow, black: regulating output current at 1 A for reverse power transfer.



(a) (b)

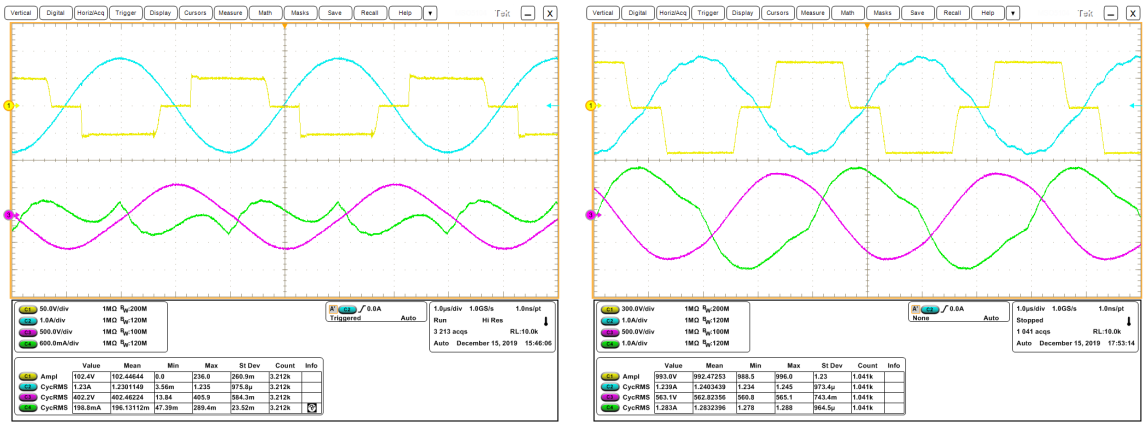
Fig. 7.22: Steady state operating waveforms of the resonant tank signals (a) at 50 W and (b) at 500 W load in forward power transfer with $\phi_{AB} = 120°$, $\phi_{DE} = 180°$, and $\phi_{AD} = 60°$. CH1 (deep blue): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v_{Cr}, CH4 (green): i_R.

Fig. 7.22 and Fig. 7.23 for forward and reverse power transfer, respectively, at 50 W and 500 W load. And it can be seen from these captures in Fig. 7.22 and Fig. 7.23 that the tank signals follow the phasor relationship shown in Fig. 7.13. The rms current in the tank inductors and rms voltage across the resonant capacitor are also measured in hardware, from the oscilloscope captures, for the entire load range in both direction of power flow and are compared to their analytical values. The comparison(s) are shown in Fig. 7.24(a) for forward power and in Fig. 7.24(b) for reverse power operation. In Fig. 7.24, the analytical results from Table 7.3 are plotted in solid line(s) whereas the measured data are shown in corresponding dots of same color. The top plot in Fig.7.24(a) and Fig.7.24(b) compares the rms current (i_t and i_R) in the tank inductors and the bottom plot compares the rms value of resonant capacitor voltage (v_{Cr}). The plots in Fig.7.24 depict a good match between analysis and results obtained from the hardware experiments.

The converter efficiency, regulating its DC output at its desired value – 150 V for forward power transfer and 1 A for reverse power transfer, are shown in Fig. 7.25 where the result for forward power is shown in blue and the black plot is for operating in reverse direction of power flow, with a peak efficiency around 96 %.

7.4 Tolerance Analysis

The variation of DC output voltage, for forward power flow and DC output current,



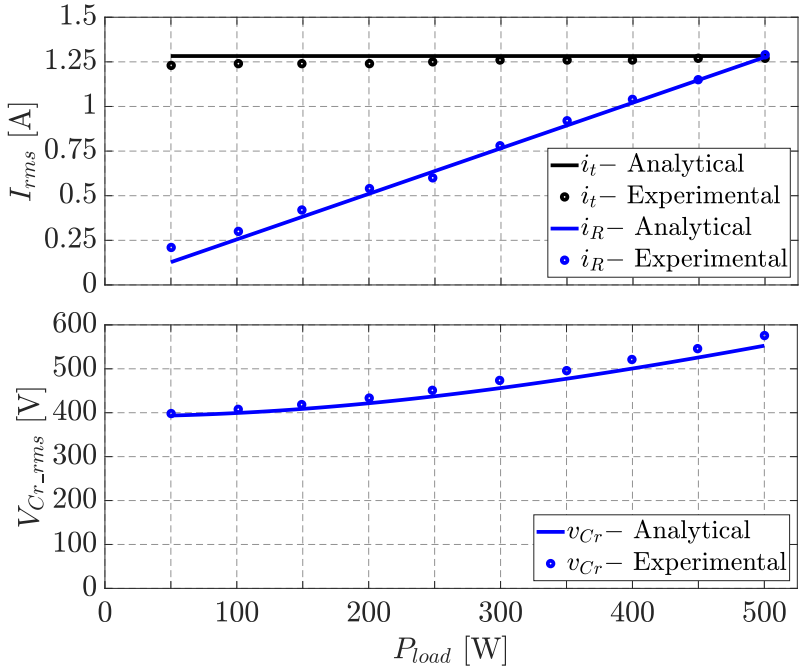
(a) (b)

Fig. 7.23: Steady state operating waveforms of the resonant tank signals (a) at 50 W and (b) at 500 W load in reverse power transfer with $\phi_{AB} = 120°$, $\phi_{DE} = 180°$, and $\phi_{AD} = -120°$. CH1 (yellow): v_{AB}, CH2 (cyan): i_t, CH3 (purple): v_{Cr}, CH4 (green): i_R.

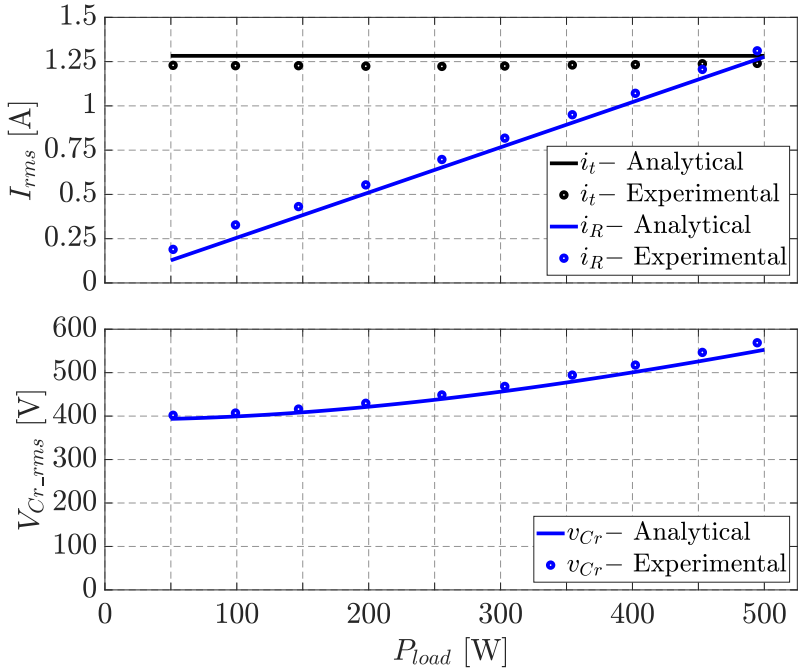
for reverse power flow are plotted in Fig. 7.26, for variation in each tank components, one at a time, keeping the other two elements at their nominal value. The results shown in Fig. 7.26 is from simulation carried out in MATLAB-PLECS at lowest output power of 50 W where the quality factor (Q) is highest and the output(s) would be most sensitive to component tolerances. In Fig. 7.26, the solid lines represent the percentage variation in the DC output for forward power flow and the dotted lines are for reverse power flow with respect to percentage variation in L_r (blue), C_r (red) and L_g (black). From this plot, it can be seen that the DC output is not sensitive to the variation in resonant inductor values but are strongly dependent on variation in resonant capacitor. However, since class I ceramic capacitors (C0G, NP0), stable over voltage bias and temperature, are used as the resonant capacitor, the tolerance in capacitance is within ±5 % resulting in a variation in output within ±6 %. This variation can be taken care of by the control range of ϕ_{AB} (120° to 180°). Further, since the tolerance is prominent at light loads, active shunt current control circuit [99] can also be utilized at the input source with slight drop in light load efficiency.

7.5 Bidirectional LCL-T Resonant Converter for Wide Voltage Range

The load independent output characteristics of bidirectional LCL-T resonant converter



(a)



(b)

Fig. 7.24: Comparison of analytical and experimentally measured rms values of tank signals plotted against load power for (a) forward power and (b) reverse power, operating with $\phi_{AB} = 120°$. Solid lines represent analytical expression and dots represent experimental result.

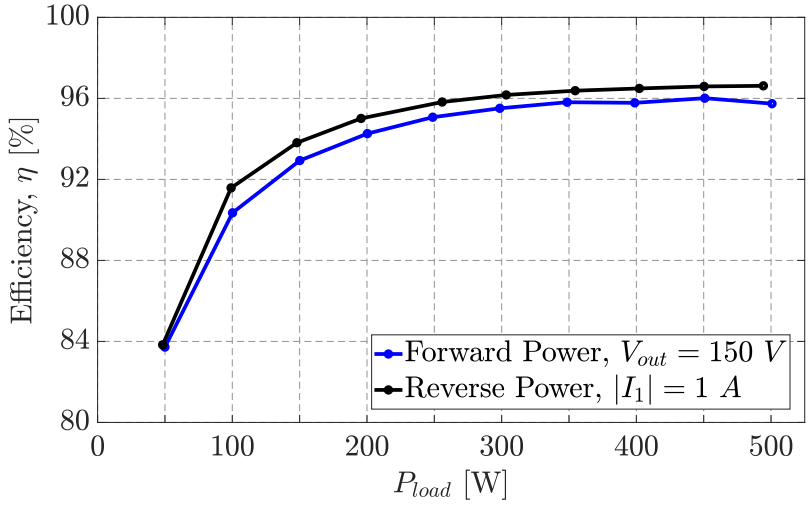


Fig. 7.25: Experimentally measured efficiency of the converter versus load power for forward (blue) and reverse power (black), regulating its output at 150 V and 1 A, respectively.

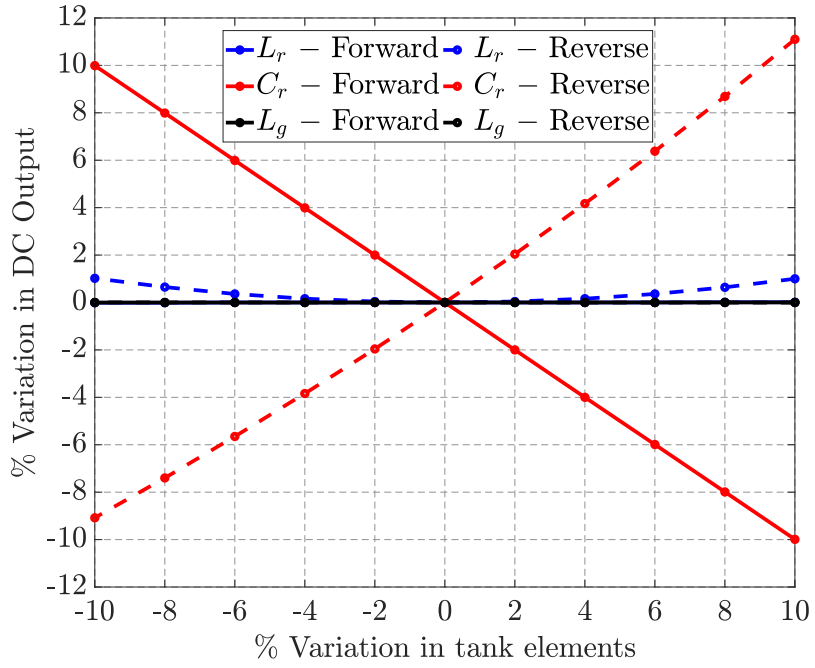


Fig. 7.26: Percentage variation in DC output with respect to variation in resonant tank elements. Solid lines are for forward power transfer and dotted lines are for reverse power flow operation. Blue lines are for L_r, red lines are for C_r and black lines are for L_g.

Table 7.5: Operation modes of the bidirectional converter over wide voltage range

Mode of operation	Active switches in switch network	Active transformer windings	Voltage range (V_2)
$n1$	Q_{21}, Q_{22}	P, S_1	$V_{2\_min} - rV_{2\_min}$
$n2$	Q_{19}, Q_{20}	P, S_2	$rV_{2\_min} - r^2V_{2\_min}$
$n3$	Q_{17}, Q_{18}	P, S_3	$r^2V_{2\_min} - r^3V_{2\_min}$
$n4$	Q_{15}, Q_{16}	P, S_4	$r^3V_{2\_min} - V_{2\_max}$

can be extended for use in critical applications requiring to interface constant current source to wide output voltage, similar to Section 5.4, in either direction of power flow. The converter hardware architecture is shown in Fig. 7.27 where in forward direction of power flow, power is drawn from current source (I_g) to load (R_{L2}), as shown in blue, and in reverse direction of power flow, power is drawn from voltage source (V_g) to load (R_{L1}), as shown in brown.

In forward direction of power flow, the output is regulated to a constant voltage over wide range and in reverse power flow, output current is regulated to a fixed value from input voltage source that can vary over wide range. The multi-winding transformer and the switch network on the secondary windings of the transformer are activated according to the need of V_2, as decided by the range presented in Table 7.5. A major difference between the LCL-T resonant tank based converter architecture shown in Fig. 7.27 compared to the architecture based on PRC, as shown in Fig. 5.21, is that in the LCL-T tank based converter, the transformer secondary windings work independently, one at a time, based on the range mentioned in Table 7.5 and thus do not need the transformer secondary windings to be closely coupled. This makes the transformer design relaxed in terms of close proximity of secondary windings. In addition, this converter architecture in Fig. 7.27 is capable of bidirectional power transfer whereas, the PRC based converter in Fig. 5.21 is unidirectional and to make it operate as bidirectional, the secondary side MOSFETs need to be replaced by 4-quadrant switches because of the presence of filter inductors (L_{f1} and L_{f2}) which make the secondary bridge(s) current fed in reverse direction of power flow.

In the converter shown in Fig. 7.27, the resonant inductor (L_r) and capacitor (C_r) are

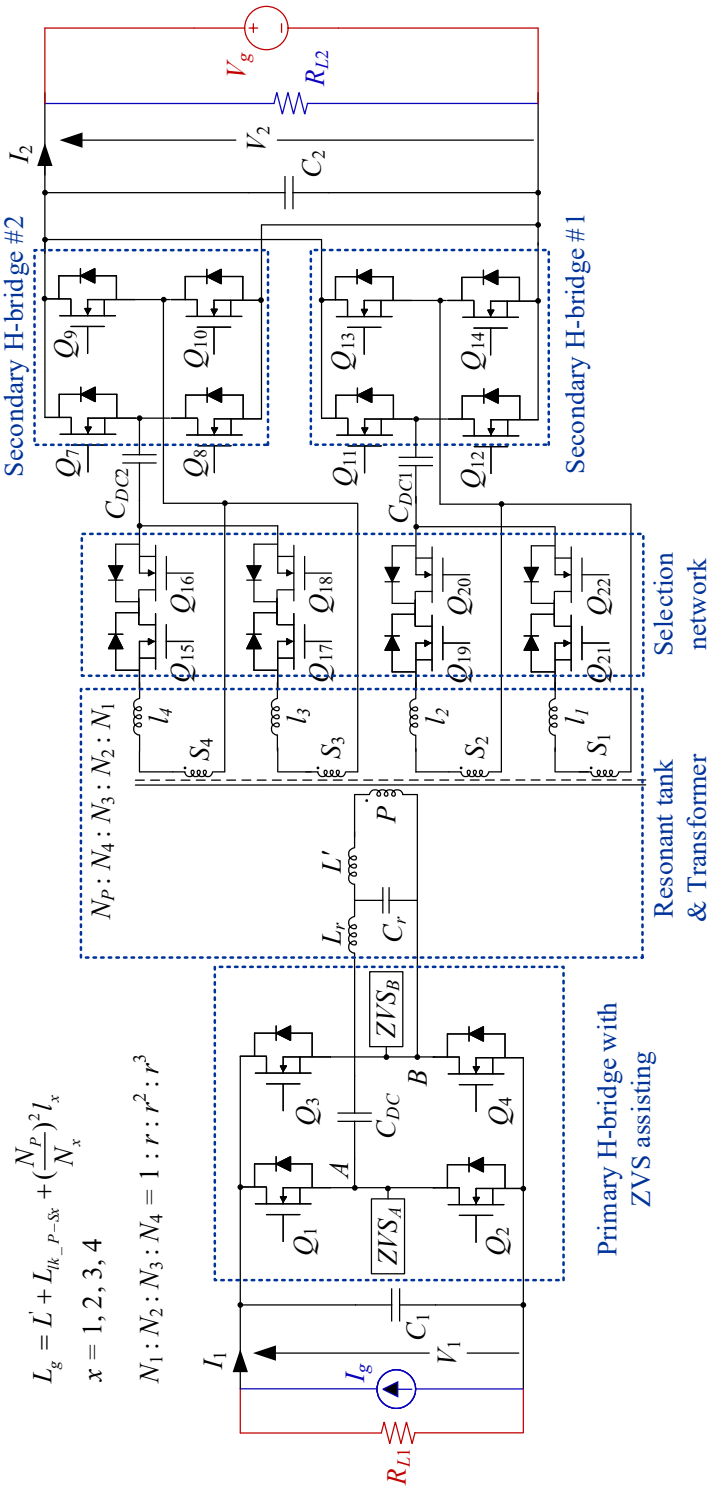


Fig. 7.27: Hardware architecture of the bidirectional converter for wide voltage range.

fixed, irrespective of the operating voltage. However, the second resonant inductor (L_g) consists of a fixed inductor (L') on the transformer primary side, another inductor ($l_1 - l_4$) placed in series with each of the secondary winding(s) and the leakage inductance between primary and the active secondary winding, represented by L_{lk_P-Sx}, where x ($= 1, 2, 3, 4$) denotes the index of the active secondary winding. Thus, the second resonant inductor (L_g) is given as

$$L_g = L' + L_{lk\_P-Sx} + \left(\frac{N_P}{N_x}\right)^2 l_x. \tag{7.58}$$

The leakage inductance between primary and any secondary winding (L_{lk_P-Sx}) will be different for different secondary winding(s) and hence having the flexibility of added inductor in the secondary ($l_1 - l_4$) makes it easy to tune the second resonant inductor (L_g) for all operating modes. Another option to overcome the challenge of mismatch of leakage inductance(s) across the secondary winding(s) is to use a series capacitor on the transformer secondary side, to compensate for mismatched part of the leakage inductance(s). And in such arrangements, the DC blocking capacitors on the secondary side of the transformer will not be needed.

The transformer turns ratio is related by

$$N_1 : N_2 : N_3 : N_4 = 1 : r^1 : r^2 : r^3, \tag{7.59}$$

where the term r is defined in 5.58. The converter shown in Fig. 7.27 can be extended for any number of secondary windings with switch network, based on the overall range of voltage ($V_{2\_min} - V_{2\_max}$). The converter in Fig. 7.27 is simulated in MATLAB-PLECS to check its bidirectional operation for one of the transformer winding (S_4) with 1 A source in forward power transfer and with voltage source of magnitudes of 140 V, 200 V and 250 V in reverse power, at different operating ϕ_{AB} while keeping ϕ_{DE} and ϕ_{AD} as per (7.44) and (7.45). The results are presented in Fig. 7.28 and Fig. 7.29 for forward and reverse power transfer, respectively. In Fig. 7.28 and Fig. 7.29, the dotted lines represent the analytically estimated

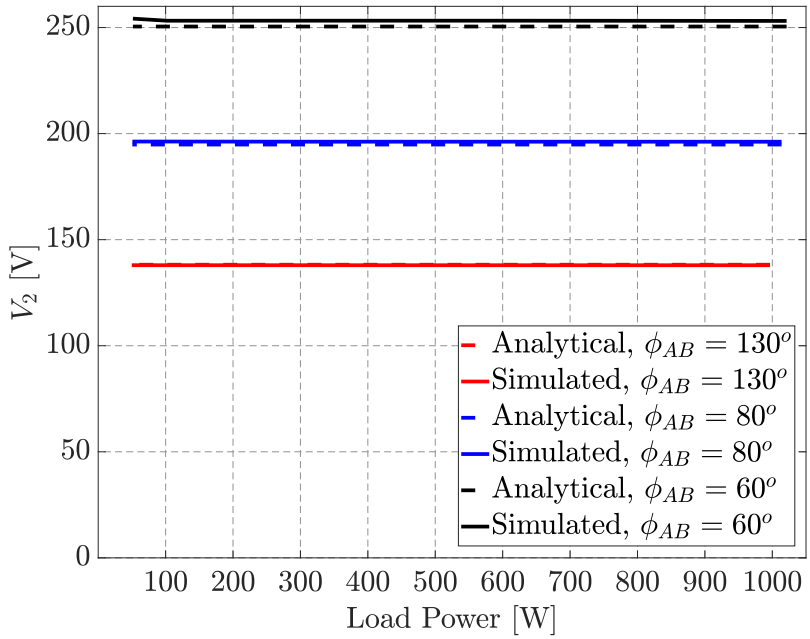


Fig. 7.28: Output voltage (V_2) over the load range in forward power transfer through winding S_4, for different control angle(s) (ϕ_{AB}).

DC output(s) from Table 7.3 and the solid lines are the result(s) obtained from simulation. It can be seen in Fig. 7.28 that in forward power transfer, the output voltage remains load independent over the load range of 50 W to 1 kW and the difference in simulation result(s) from analytical estimate(s) is within 2 %. Similarly, in reverse power flow, the output current is load independent and the deviation in simulation result(s) from analytical estimate(s) is within 2 %, as shown in Fig. 7.29. Since the transformer secondary windings for this converter operate independently, the converter characteristics will be similar in operation for other secondary windings, scaled by the turns ratio of the active secondary winding.

Summary

In this chapter needs of critical loads in underwater distribution network are introduced. A dual active bridge LCL-T resonant tank based DC-DC converter is analyzed to show how it can be designed to meet the requirements of such critical loads to provide constant voltage to the load from a constant current source, under regular operation and

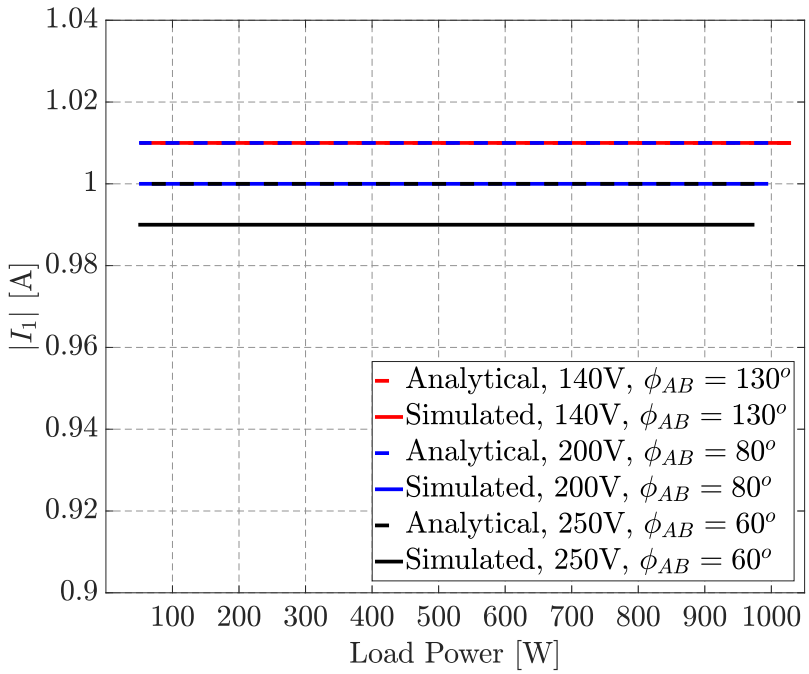


Fig. 7.29: Output current ($|I_1|$) over the load range in reverse power transfer through winding S_4, for different control angle(s) (ϕ_{AB}).

convert an auxiliary voltage source to a constant current drive in the event of loss of power from main feed. Steady state analysis and modeling have been shown for the general case with three angle modulation, for either direction of power flow, which is then optimized for use in constant current distribution system, meeting its constraints. The DC input/output relationships are established for this converter alongside its resonant tank signals with their phasor relationships. It is presented how the converter can be designed with proper modulation angle set in order to operate the converter with minimum VA rating for the H-bridges, resonant tank and transformer. The analysis is verified through experimental results from hardware prototype, showing good match between analytical and practical results.

The load independent output characteristics of tuned LCL-T resonant network is extended for applications requiring to interface constant current to wide range voltage, in either direction of power flow. A converter architecture with multi-winding transformer and switch network is introduced in this chapter to operate the converter with reduced component stress over the wide range of voltage. Simulation results from this converter

presented a good match with its analytical values, in both direction of power flow. The advantage of this architecture is that the transformer secondary winding(s) can operate independently, one at a time, and the different leakage inductance(s) across the secondary windings can be easily absorbed into the resonant tank which makes the converter operation less dependent on transformer parasitics.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

Underwater long distance distribution network uses constant current distribution due to its robustness against voltage drop over cable length and cable faults. Resonant power converters are popular choice for DC-DC power conversion at high switching frequency due to their soft-switching capability, high efficiency, high power density and low EMI owing to operation with sinusoidal waveforms. These features make resonant converters practical choice for use in underwater distribution system where efficient, reliable and quiet power conversion are of prime importance for long term operation. The design of resonant converters available in literature are for voltage source input whereas, the converters in underwater distribution network are fed from a DC current source. The characteristics of resonant converter with constant current input is quite different than converters with constant voltage input. If the resonant converters are not designed with care, there may be a restriction on minimum power transfer. In this dissertation, restriction of minimum power operation is investigated for resonant converters and its dependence on operating point is detailed which turned out to be dual of maximum power transfer theorem for voltage source based converters. This restriction is avoided by appropriate operating point selection for the converters. Soft switching requirements for the converters are also investigated and appropriate ZVS assisting circuits are employed in the design of series resonant, parallel resonant and LCL-T resonant converters operating in a system of 1 A DC current distribution network with switching frequency of 250 kHz.

8.1 Summary of Contributions

The contributions of the work presented in this thesis are summarized as follow.

8.1.1 Zero Voltage Switching

Resonant converters in underwater systems operate with the restriction of minimum power transfer which is eliminated by operating the converter at its resonant frequency. Fixed frequency symmetrical phase shift modulation in the converter makes the lagging leg soft switch and leading leg soft/hard switch, depending on the resonant tank. Hence, an assisting circuit is required for the leading leg to ensure ZVS turn on of the MOSFETs. Passive ZVS assisting circuits work well if the range of operating points is limited, but, can lead to inefficient power conversion if used in converter with wide range of operating conditions. This limitation is overcome through use of active ZVS assisting circuit. Design methodology for such assisting circuits are presented with practical consideration and the advantage and disadvantages of both type of ZVS assisting circuits are exemplified through operation of an SRC. Further, the ZVS assisting circuits are utilized in PRC and LCL-T resonant converters to ensure ZVS turn on of all the MOSFETs in the converter.

8.1.2 Series Resonant Converter

Series resonant converter is simplest of all types of resonant converter. With steady state modeling and detailed analysis, the DC input output relationships are established and from there it is shown that SRC can operate as load independent constant current drive if operated at the tank's resonant frequency. The converter is designed with resonant tank components' tolerance in mind so that the converter can regulate its output down to 10 % load even under worst case scenario. The stress on tank components are also established which can also be used for tank design. Results obtained from a 1 kW prototype SRC validates the analysis and shows that the converter behaves as constant current drive over 0 W to 1 kW load range with very little droop.

8.1.3 Parallel Resonant Converter

Parallel resonant converter, operating at its resonant frequency behaves as load independent constant voltage at the output with constant current input source. With detailed modeling and analysis, the steady state DC input and output relationship is established

along with resonant tank component stress. From this component stress, the converter is designed such that the VA rating of the tank inductor is minimized. Device ratings, output filter design, ZVS requirements are also presented. Results from experimental prototype shows the constant output voltage characteristics under steady state as well as under load transients.

Utilizing the load independent output voltage characteristics of PRC, a converter architecture with a multi-winding transformer and AC switch network is introduced for application involving wide range of output voltage. It is shown how this converter can operate with relatively low component stress under wide output voltage and load range. Simulation and experimental results are presented for the proof of concept hardware prototype of 500 W.

8.1.4 LCL-T Resonant Converter

Similar to PRC, LCL-T resonant converter can also provide load independent constant voltage at the output when supplied from constant current source, with proper design. The converter is analyzed with steady state modeling and shown that its output characteristics would be constant voltage if operated at its resonant frequency. The design for the converter is performed with the constrains of current source input in mind and minimizing the VA rating for the passive components. With simulation and experimental results it is shown that diode bridge based rectification on the secondary side imposes challenge on low Q design and use of active rectifier in place of diodes overcomes this limitation. Modulation scheme for such active rectifier based LCL-T resonant converter is presented to emulate the behavior of diode bridge rectifier. ZVS requirements for both primary and secondary bridges are analyzed and an active ZVS assisting circuit for primary H-bridge and a passive ZVS assisting circuit for secondary H-bridge are employed to achieve ZVS for the entire range of operating points. Results from experimental prototype shows very good match with the analytical results for a hardware prototype of 500 W.

8.1.5 Bidirectional DAB LCL-T Resonant Converter

Some of the power converters in underwater distribution system cater to critical loads

which demand redundant bidirectional power converters to be used. In such converters, DAB LCL-T resonant converter is a good fit which converts constant current source to voltage source in forward power flow and under loss of power from main feed, the module converts an auxiliary voltage source to a current drive, independent of load. Through detailed modeling and analysis, with generalized three angle modulation of DAB, the steady state DC input – output relationship and expressions for tank AC signals are derived. From there, the tank is designed to minimize the overall VA rating of the converter, keeping the constraints of constant current input in mind. Experimental prototype is developed and tested up to a power level of 500 W with 1 A current source to 150 V output, in forward power flow and 150 V DC voltage source to 1 A constant current drive, in reverse direction of power flow, with good match between analytical and experimental results.

8.2 Future Work

The work presented in this thesis covers a variety of resonant converters with their steady state analysis and design techniques. However, there are few areas where further improvements can be made and/or explored for future research.

- The converters presented in this dissertation are only tested for their open loop output characteristics. The converters have either constant current output or constant voltage output characteristics, independent of load which means the control effort required is minimal for the load range. However, in practical scenario the converter output needs regulation due to temperature change and other factors and hence suitable closed loop control strategy is needed. A small signal modeling of the converter(s) is needed to design such closed loop converter and phasor modeling can be employed for modeling the resonant converter(s) [109–111].

- In addition to converter closed loop control as a stand alone converter, stability analysis needs to be carried out for system of converters used in underwater system considering cable impedance. Due to long distance of the cable, the parasitic inductance and capacitance of the cable imposes restrictions on the bandwidth of the converter

controller [112]. This needs further investigation and the converter(s) may need a energy buffer at the input of the converter to maintain system stability under large load transients.

- The PRC converter architecture with multi-winding transformer and switch network for wide range of output voltage needs close coupling among the secondary windings of the transformer which becomes challenging for physical fabrication when number of secondary windings increase. This requires detailed modeling of multi-winding transformer [105] and the converter needs analysis for tolerance with the detailed transformer model.

- The LCL-T resonant converter presented in chapter 6 and chapter 7 can be extended for operation in systems with wide voltage range. This is achieved through employing a multi-winding transformer and switch network to reduce the component stress as presented in section 7.5. Unlike the configuration used in PRC for wide voltage range (section 5.4), this architecture uses only one transformer secondary winding at a time and thus relaxes the design of transformer. In addition, the resonant tank needs to be optimized for operation at full power, over the output voltage range.

- CLC-T resonant converter is the dual of LCL-T resonant converter and it has the same steady state output characteristics as the LCL-T resonant converter. Since the VA rating of inductors and capacitor are equal to each other in LCL-T network, CLC-T resonant converter will have same overall VA rating of the tank. However, the additional DC blocking capacitor(s) in LCL-T resonant converters will not be needed in CLC-T resonant converter and thus has slight edge in terms of component count. Moreover, the L in CLC-T resonant converter can be integrated in the isolation transformer which can reduce the overall size of the converter.

- Both LCL-T and CLC-T resonant converter topologies can provide load independent current drive from voltage source input which can be a good candidate topology for LED driving, battery charging applications etc. The modulation angle set or the

resonant tank can be modified to ensure ZVS operation of the active switches without the need of additional ZVS assisting circuits. This will result in higher power density of the converter in such applications.

APPENDICES

APPENDIX A

Controller Implementation

The controller implemented in FPGA for generating pulses for the converter are presented here. The control board used is a Xilinx Artix-7 based FPGA module (P/N: CMOD A7-35T) and it is coded using Verilog Hardware Description Language (Verilog HDL) through Vivado suite from Xilinx. The PWM signals are generated with 12 bit resolution in the FPGA with 250 MHz clock that provides a resolution of 0.36° in phase shift at 250 kHz. For SRC and PRC, the controller used is based on SPARTAN-6 FPGA, coded in Verilog HDL details of which, including synchronous rectification implementation for secondary side devices in PRC, can be found from Section 6.6 in [113]. The way of implementing the modules in Verilog HDL are similar in both the FPGAs and those are discussed here next.

A.1 Pulse Generation

The PWM signals are generated with phase A taken as reference and all other legs lagging with respect to phase A. For all the legs, the top and bottom PWM signals are complementary to each other with 150 ns dead time between them. The reference phase for phase A is set at zero as shown below.

```
always @(posedge clk)
 if(count == CounterMax - 1)
 Phi0A <= 12'd0;        // This will be the reference phase. Phase A
 else
 Phi0A <= Phi0A;
end
```

The phase lag for phase B is generated with respect to phase A by adding 'PhaseM' to 'Phi0A' which effectively creates control angle ϕ_{AB} and it is shown below.

```
always @(posedge clk)
 if(count == CounterMax - 1)
 Phi0B <= Phi0A + PhaseM;        //Phi0B = Phi0A + PhaseM. Phase B
 else
 Phi0B <= Phi0B;
end
```

The phase lag for phase ZA (ZVS assistance leg for leg A) is generated with respect to phase A by adding 'PhaseAZ' to 'Phi0A' which effectively creates control angle ϕ_{AZ} and it is shown below.

```
always @(posedge clk)
 if(count == CounterMax - 1)
 Phi0ZA <= Phi0A + PhaseAZ;        //Phi0ZA = Phi0A + PhaseAZ. Phase ZA
 else
 Phi0ZA <= Phi0ZA;
end
```

The phase lag for phase ZB (ZVS assistance leg for leg B, used in reverse power flow in DAB LCL-T resonant converter) is generated with respect to phase B by adding 'PhaseBZ' to 'Phi0B' which effectively creates control angle ϕ_{BZ} and it is shown below.

```
always @(posedge clk)
 if(count == CounterMax - 1)
 Phi0ZB <= Phi0B + PhaseBZ;        //Phi0ZB = Phi0B + PhaseBZ. Phase ZB
 else
 Phi0ZB <= Phi0ZB;
end
```

The PWM sync signal between primary and secondary H-bridges in DAB LCL-T resonant converter is generated with respect to phase A by adding 'PhaseM/2' ($\frac{\phi_{AB}}{2}$) and it

is shown below. The variable 'Phi_AD_Delay' is used in the sync signal to compensate any delay between the final gate-source signal(s) of leg A and leg D, in hardware.

```
always @(posedge clk)
 if(count == CounterMax - 1)
 PhiSync <= PhaseM[`NPHI-1:1] - Phi_AD_Delay;
 //PhiSync = PhaseM/2 - offset [PhaseM is phiAB]
 else
 PhiSync <= PhiSync;
end
```

The PWM module structure is shown below as an example for phase B where 'td' is the dead time and 'BHI' and 'BLO' are the PWM signal output from FPGA for top and bottom switches of leg B. This structure is used for PWM generation for all the legs in the converter.

```
   phaseSignalCreation PulseB //(Deals with BHI and BLO signals)
(
        .clk(clk),
        .count(count),
        .Half_CntMax(CounterMaxd2),
        .Phi0X(Phi0B[`NPHI-1:0]),
        .Td(td),
        .out_HI_buf(gateSignal[`BHI]),
        .out_LO_buf(gateSignal[`BLO])
);
```

The PWM generation module is shown below for any phase, where 'Phi0X' is the phase shift of that particular leg with respect to phase A.

```
module phaseSignalCreation(
        input wire              clk,    // PWM Clock, 250 MHz
```

```
        input wire [`NDPWM-1:0] count,  // PWM Counter (12-bit)
        input wire [`NDPWM-1:0] Half_CntMax,  // PWM Count for 180°
        input wire [`NDPWM-1:0] Phi0X,  // controlled leg phase-shift
        input wire [`NDPWM-1:0] Td,     // Dead time delay

        output wire        out_HI_buf,
        // Upper FET gate signal (after shoot-through protection)
        output wire        out_LO_buf
        // Lower FET gate signal (after shoot-through protection)
);

        reg  [`NDPWM-1:0]  HI_off; // Upper FET turn-off point
        reg  [`NDPWM-1:0]  LO_off; // Lower FET turn-off point
        reg  [`NDPWM-1:0]  HI_on;  // Upper FET turn-on point
        reg  [`NDPWM-1:0]  LO_on;  // Lower FET turn-on point
        reg  [`NDPWM-1:0] count_reg;
        output wire        out_HI,
        // Upper FET gate signal (before shoot-through protection)
        output wire        out_LO,
        // Lower FET gate signal (before shoot-through protection)

        always @(posedge clk)
         count_reg <= count;        //counter

        always @(posedge clk)
         HI_on <= Phi0X;
        always @(posedge clk)begin
         HI_off <= Phi0X + Half_CntMax - Td;
```

```
        //generation of top switch PWM with dead time
        end

        always @(posedge clk)begin
         LO_on <= Phi0X+Half_CntMax;
        end

        always @(posedge clk)begin
         if(Phi0X > (Td-1))
                LO_off <= Phi0X - Td;
         else
                LO_off <= Phi0X+Half_CntMax + Half_CntMax - Td;
                //generation of bottom switch PWM with dead time
        end

endmodule
```

The PWM sync signal from primary FPGA controller is passed to the secondary side FPGA controller to generate the PWM signals for leg D and leg E with $\phi_{DE} = 180°$ and a dead time of 150 ns, synchronized with respect to leg A of primary, which is presented below.

```
module pwm_gen_2 (clk,
        rst,
        sync,
        gate_sgnl);

        input clk;
        input rst;
        input sync;         //PWM synchronization signal from primary
```

```
        output [3:0] gate_sgnl;

        wire hi;
        wire lo;
        wire [11:0] count;
        wire rise;
        wire fall;

        assign gate_sgnl[0] = hi;        //D_top
        assign gate_sgnl[1] = lo;        //D_btm
        assign gate_sgnl[2] = lo;        //E_top
        assign gate_sgnl[3] = hi;        //E_btm

pwmCtl_2 pwm1_inst(.clk(clk),
        .rst(rst),
        .fall(fall),
        .rise(rise),
        .Hi_O(hi),
        .Lo_O(lo));

edge_detector dtct_1(.clk(clk),
        .rst(rst),
        .puls_in(sync),
        .rise(rise),
        .fall(fall));

endmodule
```

```
module pwmCtl_2(clk,
        rst,
        rise,
        fall,
        Hi_O,
        Lo_O
        );
        parameter max = 9'd462;         //180deg - Td
        input clk;
        input rst;
        input rise;
        input fall;
        output Hi_O;
        output Lo_O;

        reg PO;
        reg Hi_O;
        reg Lo_O;
        reg [8:0] negCount;
        reg [8:0] posCount;
        reg negLock;
        reg posLock;

        always @ (posedge clk or posedge rst)begin
                if(rst)begin
                        negCount <= 9'd0;
                        negLock <= 1'b0;
```

```
        end
        else begin
                if(fall && negCount < max && !negLock)begin
                        negCount <= negCount + 1;
                        Lo_0 <= 1'b1;
                end
                else begin
                        negCount <= 9'd0;
                        negLock <= 1'b1;
                        Lo_0 <= 1'b0;
                end
                if(rise)
                        negLock <= 1'b0;
        end
end

always @ (posedge clk or posedge rst)begin
        if(rst)begin
                posCount <= 9'd0;
                posLock <= 1'b0;
                Hi_0 <= 1'b0;
        end
        else begin
                if(rise && posCount < max && !posLock)begin
                        posCount <= posCount + 1;
                        Hi_0 <= 1'b1;
                end
                else begin
```

```
                posCount <= 9'd0;
                posLock <= 1'b1;
                Hi_O <= 1'b0;
            end

            if(fall)
                posLock <= 1'b0;
        end
    end

endmodule
```

A.2 FPGA Interface through MATLAB

The FPGA code is initiated through serial interface (USB) using MATLAB function as presented below where different control registers are used for controlling the various phase shift angle(s) between the legs of H-bridge(s) and enabling the PWM signals.

```
function [ pg ] = BDPC_LCL_Startup(  )
clc;
BDPC_Serial_Open('COM42');          % Primary COM port opening
pause(1);
BDPC_Serial_Write_Register(9,499)   % phi_AB: default 180 deg
pause(1);
BDPC_Serial_Write_Register(1,1000)  % fs: 250 kHz default with 250 MHz clk
pause(1);
BDPC_Serial_Write_Register(12,1)        % ZVS A Phase Angle
pause(1);
BDPC_Serial_Write_Register(13,2)        % ZVS B Phase Angle
pause(1);
```

```
BDPC_Serial_Write_Register(21,0)        % Active clamp reference
pause(1);
BDPC_Serial_Write_Register(22,21)        % Phi_AD adj; 1count=4ns reduction
pause(1);
BDPC_Serial_Write_Register(0,2055)        % Enable the PWM
clc;
end
```

CURRICULUM VITAE

Tarak Saha

Journal Articles

J1 A. C. Bagchi, T. Saha and R. Zane, Design of a Constant Voltage Output Wireless Power Supply for Autonomous Underwater Vehicles Fed from a Constant Low-Current DC Source, in *IEEE Transactions on Power Electronics*, *submitted for review.*

J2 T. Saha, A. C. Bagchi and R. Zane, Analysis and Design of an LCL-T Resonant DC-DC Converter for Underwater Power Supply, in *IEEE Transactions on Power Electronics*, *in review.*

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Patents

P1 T. Saha, A. C. Bagchi, R. Zane and H. Wang, *Dual active bridge bi-directional resonant DC-DC converter for load independent constant current to constant voltage conversion and vice versa over wide range*, disclosure filed, June, 2020.

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P3 T. Saha, H. Wang and R. Zane, *A Low RMS current Zero Voltage Switching Assisting Circuit with low power loss and EMI*, patent filed, March, 2019.

P4 H. Wang, R. Zane and T. Saha, *DC Power Supply From a Constant Current Source*, Pub. No.: US 2019/0296650 A1, Pub. Date: Sep. 26, 2019.

Conference Papers

C1 T. Saha, A. C. Bagchi and R. Zane, Time-Domain Analysis and ZVS Assistance Design for a DAB LCL-T Resonant Converter in Underwater Current Distribution Network, in *2020 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, *accepted for publication.*

C2 T. Saha, S. Mukherjee, V. P. Galigekere and O. C. Onar, Design of Auxiliary Circuit Elements for Achieving Zero Voltage Switching in a Wireless Power Transfer System, in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, 2020, *accepted for publication.*

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