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Active Stability Monitoring and Stability Control of DC Microgrids Using Incremental Continuous Injection

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ACTIVE STABILITY MONITORING AND STABILITY CONTROL OF DC

MICROGRIDS USING INCREMENTAL CONTINUOUS INJECTION

by

Rohail Hassan

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of

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in

Electrical Engineering

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ABSTRACT

Active Stability Monitoring and Stability Control of DC Microgrids Using Incremental

Continuous Injection

by

Rohail Hassan, Doctor of Philosophy

Utah State University, 2021

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Existing dc microgrids such as those integrating renewable energy to the grid, and emerging dc microgrids such as all-electric ships, more-electric aircraft, automobiles and automobile charging stations all involve several kinds of power electronic converters connected to a common dc bus. Stable operation of these interfacing converters for all operating conditions has been a topic of renewed interest in the last couple of decades. Traditionally, dc microgrids have been designed conservatively to be over-damped and able to handle worst case conditions. However, increasing power capacity of emerging dc microgrids causes this conservative design to become cost and size prohibitive, and overdamping causes the system to become slow and unable to handle high bandwidth loads such as pulsed power loads, radars etc. To reduce the dependency on passives and to increase system response speed, active techniques have been proposed so that the system may be designed with smaller filters and active damping has been used to assist in guaranteeing system stability. Traditional design of dc microgrids uses impedance-based stability analysis method originally developed to analyze stability of cascaded converters and later extended to include multiple interfaced converters. This proved to be useful in the design stages for systems with duplicated sources/loads like in solar systems. However, the existing stability analysis

methods are not applicable for online evaluation of stability and for active stabilization in a dynamic system with reconfiguration and addition/removal of various kinds of sources and loads.

This dissertation first re-visits impedance-based stability analysis and develops a general stability criterion which is easily applicable to complex dc microgrids, and highly suitable for online evaluation of stability. Next, an online stability monitoring system is developed based on the new criterion which uses incremental continuous injection by an existing converter interfacing energy storage in the system and continuously evaluates system stability margin. Furthermore, this dissertation develops an active stability control for dc microgrids which utilizes the evaluation of the continuous monitor and shapes the dc bus interface impedance of the converter interfacing energy storage to maintain a prescribed system stability margin. The theory and techniques developed in this dissertation are demonstrated on a lab scale 2 kW dc microgrid.

(80 pages)

PUBLIC ABSTRACT

Active Stability Monitoring and Stability Control of DC Microgrids Using Incremental

Continuous Injection

Rohail Hassan

Electrified transportation and integration of renewable energy in the electric power grid requires the use of power electronic converters for integrating different forms of power; from ac to dc, dc to ac, dc to dc, etc. Recent trend towards electrifying automobiles, aircraft and ships, and increasing penetration of renewable energy has increased the required power levels and number of the power electronics converters connected together in a dc microgrid system. Stable operation of these interfacing converters for all operating conditions has been a topic of renewed interest in the last couple of decades. Traditionally, dc microgrids have been designed conservatively to handle the worst case conditions. However, increasing power capacity of emerging dc microgrids causes this conservative design to become cost and size prohibitive, and over-designing causes the system to become slow and unable to handle fast loads such as pulsed power loads, radars etc. To reduce the dependency on passives components and to increase system response speed, recent literature proposed techniques using control so that the system may be designed with smaller filters and guaranteed with system stability. Traditional design of dc microgrids extend the existing stability analysis techniques originally developed to analyze stability of cascaded power converters. This proved to be useful in the design stages for systems with duplicated power sources/loads like in solar systems. However, the existing stability analysis methods are not applicable for online evaluation of stability and for control-based stabilization in a dynamic system with reconfiguration and addition/removal of various kinds of sources and loads.

This dissertation first develops a general stability criterion which is easily applicable to complex dc microgrids, and highly suitable for online evaluation of stability. Next, an online

stability monitoring system is developed based on the new criterion which uses incremental continuous injection by an existing converter interfacing energy storage in the system and continuously evaluates system stability margin. Furthermore, this dissertation develops an active stability control for dc microgrids which utilizes the evaluation of the continuous monitor and provides additional damping without adding any passive filters. The theory and techniques developed in this dissertation are demonstrated on a lab scale 2 kW dc microgrid.

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Rohail Hassan

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ACRONYMS

CPL	constant power load
DVI	dynamic virtual immittance
FPGA	field-programmable gate array
RHP	right-halp plane
GMPM	gain-margin phase-margin
ESAC	Energy Source Analysis Consortium
ESC	energy storage converter
EMI	electro-magnetic interference
PI	proportional-integral
ESR	effective series resistance
HF	high-frequency
LC	inductor(L) capacitor(C)
ZVS	zero-voltage switched/switching
BMS	battery management system
IMLG	impedance minor loop gain
VSC	voltage-source converter
TI	Texas Instruments
GaN	Galium Nitride
RC	resistor-capacitor
UART	universal asynchronous receiver transmitter
PRBS	psuedo-random binary sequence
FFT	fast-fourier transform
RLC	resistor(R)-inductor(L)-capacitor(C)
AWG	american wire gauge
ADC	analog to digital converter/conversion
PWM	pulse-width modulation

CHAPTER 1

INTRODUCTION

Over the past couple of decades, there has been a great push towards electrification of transportation. The increased power level and interfacing of different kinds of power sources and loads including energy storage integration have led to new challenges in terms of design and stability analysis of such systems. Figure 1.1 shows how the future dc microgrid may be configured. Examples of such systems are found in electric vehicles [1], electric aircraft [2] and all-electric ships [3, 4].

There are two main causes of stability degradation within a dc microgrid, 1) the constant power load effects that exhibit negative incremental impedance and provide constraints on the design of the dc characteristics of the interfacing converters, and 2) interactions of the feedback loop created by the input/output impedances of the interconnected converters which dictate the system small-signal stability and provide constraints on the control and
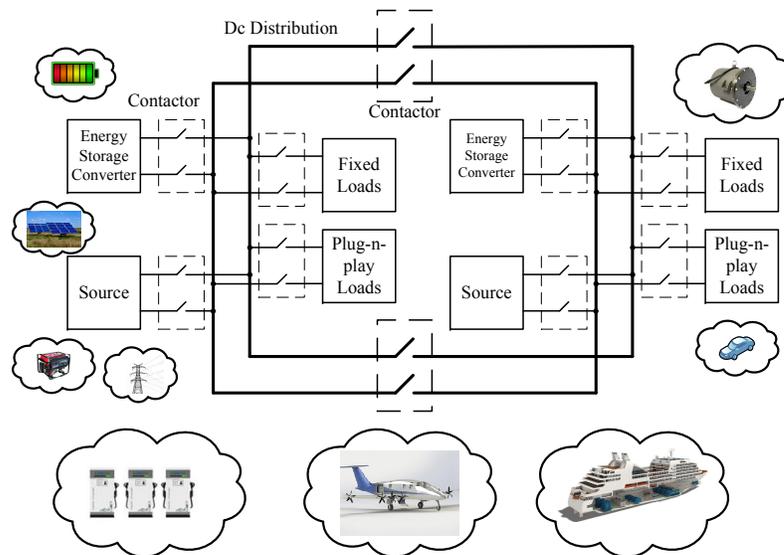
Fig. 1.1: Representative future dc microgrid system.
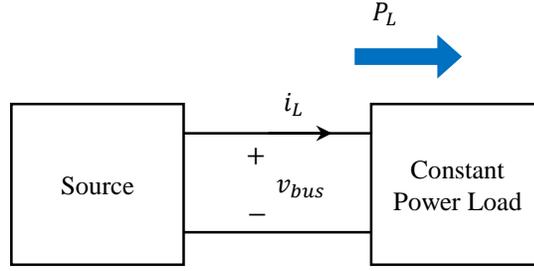
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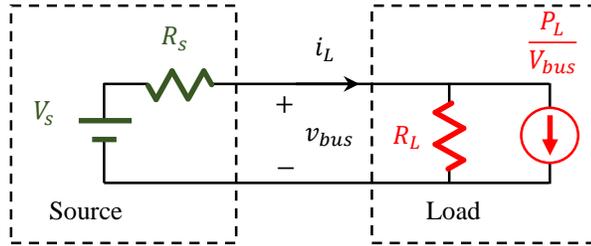
(b)

Fig. 1.2: Cascade connection of a source and a constant power load; (a) diagram, and (b) dc equivalent model.

design of passives components.

1.1 Negative Incremental Resistance of Constant Power Loads

Consider a simple case where a source, with a Thevenin equivalent voltage V_s and an output resistance R_s, is connected to a constant power load (CPL), as shown in Fig. 1.2a. The current of the CPL is given by

$$i_L = \frac{P_L}{v_{bus}}, \tag{1.1}$$
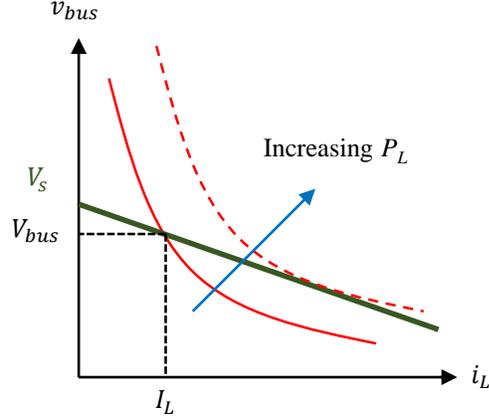
Fig. 1.3: I-V characteristics of source and load with increasing load power.

where P_L is the load power and v_{bus} is the dc bus voltage. Differentiating (1.1), we can find the load incremental resistance as

$$R_L = \frac{\partial v_{bus}}{\partial i_L} = -\frac{v_{bus}^2}{P_L}.$$ (1.2)

The resulting dc-equivalent circuit for the cascade connection is shown in Fig. 1.2b. The I-V characteristics of the source and load in Fig. 1.2 are shown in Fig. 1.3, where the source characteristics are shown by a thick green line and the load characteristics are shown by the red curves.

From Fig. 1.3, it can be seen that, for any power level, the dc operating point is given by the intersection of the source and load characteristics, (V_{bus}, I_L). As the load power increases, the load characteristics move upward and R_L decreases in magnitude. The dotted line in Fig. 1.3 shows the maximum power that has an intersection with source characteristics. At this power the negative resistance magnitude is equal to the source resistance. If the power increases further, there is no intersection and the dc bus voltage collapses with load current increasing. This gives us the first condition of stability given by

$$||R_s|| < ||R_L|| \ \forall \ P_L.$$ (1.3)
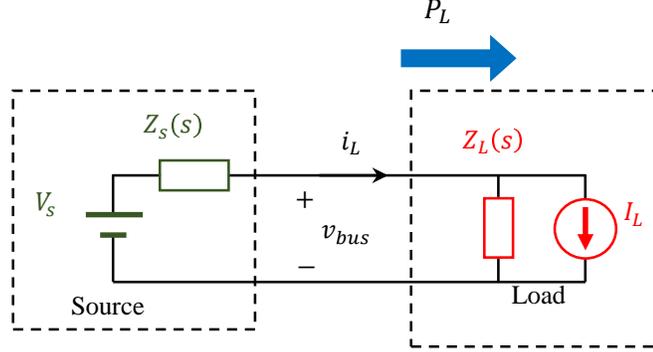
Fig. 1.4: Small-signal model of cascade connection with source and load impedances.

1.2 Impedance Interactions

The second cause of stability degradation in a dc microgrid is the interaction of the interconnected converters and their controllers. This is analyzed by using the small-signal models of the source and load, evaluated around an operating point. Among the several stability analysis methods proposed in the literature, impedance-based methods have become popular. In impedance-based stability analysis, the source and the load are represented by their Thevenin or Norton equivalent, with a complex impedance that is a function of the Laplace variable 's', as shown in Fig. 1.4. The source impedance, Z_s, and the load impedance, Z_L, shown in Fig. 1.4, capture the dynamics of the source and load converters respectively, including the behavior of the passive components and the closed loop control algorithms. Furthermore, the dc values of these impedances correspond to the resistances are shown in Fig. 1.2b, i.e.

$$Z_s(0) = R_s, \quad Z_L(0) = R_L. \tag{1.4}$$

Extending the stability condition found for the dc case in (1.3) to each frequency component, a simplistic but sufficient condition for stability is derived as

$$||Z_s(s)|| < ||Z_L(s)|| \ \forall \ \{s, P_L\}. \tag{1.5}$$

The stability criterion shown in (1.5) was developed by R. D. Middlebrook, and is referred

to as the Middlebrook Criterion [5]. The Middlebrook Criterion states that a cascade connection of power electronics converters will be stable if, for all frequencies and power levels, the magnitude of the source output impedance, Z_s, is lower than the magnitude of the load input impedance, Z_L. While the Middlebrook Criterion leads to a stable system with one source and one load, it leads to a highly conservative design with large filters and slow controllers, which becomes prohibitive as the power level of the dc microgrid increases. Furthermore, the Middlebrook Criterion cannot be easily extended to dc microgrid systems with multiple sources, loads and bidirectional converters. The current literature proposes several extensions of the Middlebrook's impedance-based stability criterion, however, very few are applicable to the dynamic and re-configurable dc microgrid such as that shown in Fig. 1.1, and fewer still allow for low cost implementation.

1.3   Impedance Compensation for Stability

Recent research has focused on reducing the conservatism posed by the Middlebrook Criterion. This has led to system designs that violate the Middlebrook Criterion but are still stable according to more relaxed stability criteria. For systems that do not satisfy the stability criteria due to changing system conditions or addition of new converters in the system, impedance-based stabilization techniques have been proposed in literature. For the one-source-one-load system shown in Fig. 1.4, if Z_s and Z_L do not satisfy the desired stability criteria, a compensation impedance may be added in series as Z_{cs} or in parallel as Z_{cp}, as shown in Fig. 1.5a. If it is desired to satisfy the Middlebrook Criterion, the compensation impedance may be designed such that

$$||Z_{s,eff}(s)|| < ||Z_L(s)|| \; \forall \; \{s, P_L\}, \tag{1.6}$$

where $Z_{s,eff} = Z_{cp}//Z_s$ if parallel compensation is used, or $Z_{s,eff} = Z_{cs} + Z_s$ if series compensation is used. The effective small-signal model of the cascade connection is shown in Fig. 1.5b.
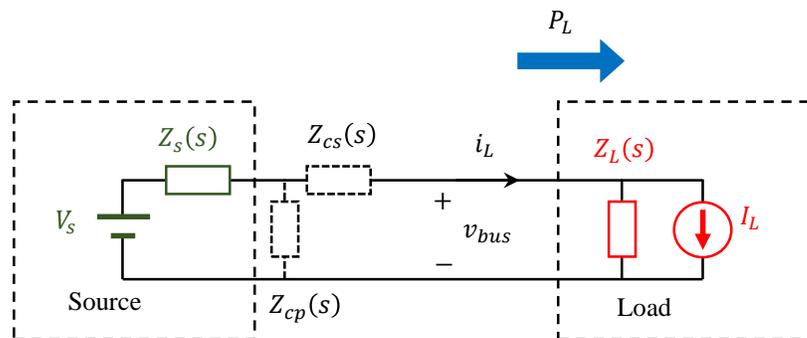
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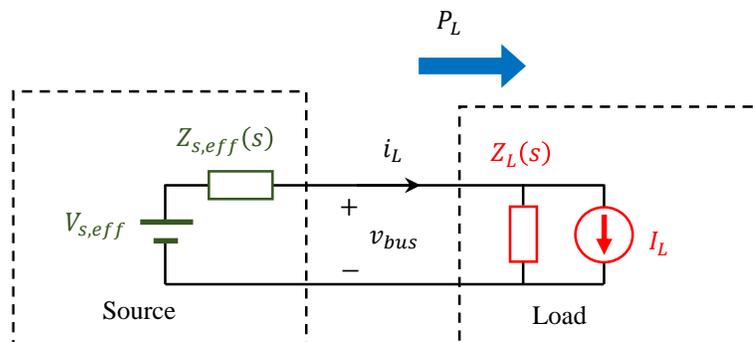
(b)

Fig. 1.5: Impedance-based compensation for stability; (a) series- and parallel-compensation, and (b) effective small-signal model.

The compensation impedance may be implemented using passive components comprising resistors, capacitors and inductors, but it adds to the cost and volume of the system, which is undesirable. An attractive alternative is active compensation in which the control of a converter in the system is used to emulate the behavior of resistors, capacitors, and inductors. This approach helps to reduce the system size and cost, but it requires online monitoring of system stability. This is the approach that is taken in this work.

1.4 Contributions of this Thesis

Traditional dc microgrid system design methods lead to system overdesign including oversizing of filters and slow controllers. Future dc microgrids require higher bandwidth controllers to handle loads such as radars and pulsed power loads, and size and weight constraints restrict the size of the filters that can be used. This poses a challenge in terms of managing loads and maintaining stability. To avoid system overdesign, active stabilization techniques have been developed which reduce dependence on passives and allow for higher load bandwidths. Application of these techniques require online system identification for which several methods have been developed. There are three main accomplishments in this thesis:

1. Re-visited the impedance-based stability analysis of dc microgrids and developed a method that can handle a dynamically re-configurable system such as that shown in Fig. 1.1 and is well suited for online monitoring of system health in such systems,

2. Designed a method to measure system stability online and continuously as the system operating point changes in order to provide a proactive approach for maintaining system stability, and

3. Developed a control method to regulate system stability with a prescribed stability margin by shaping the impedance of the dc bus using power converter interfacing energy storage.

The work done in this thesis to demonstrate these achievements has been published in high quality conferences and journals. Each published paper reviews the literature, details the design and implementation, and shows hardware results for one of the contributions mentioned above. The published papers, which are attached thereafter, are introduced below:

1. *Nodal Impedance-Based Stability Analysis of Dc Nanogrids* [6]: This paper proposes a novel stability analysis method based on nodal analysis targeted for future dc nanogrid systems. The proposed method does not require source and load identification or grouping and hence can be applied easily in a dynamically changing system. Furthermore, it is shown that the analysis using the proposed method can be performed at the terminal of any converter in the dc nanogrid, making this an ideal candidate for online stability analysis. The proposed method provides necessary and sufficient conditions for stability, and leads to new solutions for active stabilization.

2. *Continuous Stability Monitoring of DC Microgrids Using Controlled Injection* [7]: This paper presents a novel system stability monitor that can be added onto any existing converter in the system as an auxiliary function and continuously monitors the stability margin of the interconnected system. The stability margin evaluation is enabled by Nodal Stability Analysis. The proposed continuous monitor injects a controlled single-frequency perturbation using one of the converters already in the system, with a small amplitude that does not affect the normal operation of the system. The proposed method can be used in any interconnected system for proactive monitoring and maintaining the system stability, and its continuous nature would enable development of new techniques in adaptive stability enhancement of dc microgrids.

3. *High Frequency Link Isolated Multi-Port Converter for Active Cell Balancing Applications* [8]: This paper proposes an isolated multi-port converter based on high-frequency ac link to combine the multiple modular cell-level active balancing converters into a single multi-port converter. The paper focuses on introducing this novel converter topology which has applications where a battery energy storage is interfaced

with a dc microgrid system. The proposed topology can be utilized in achieving cell level balancing as well as serve as a platform for implementing the stability monitoring tasks for the dc microgrid system.

4. *A Continuous Stability Margin Monitor for DC Microgrids* (in submission): This article extends the stability monitor presented in [7] by developing a rigorous small-signal model and design guidelines for the stability monitor. The article proposes a novel control strategy to improve the dynamics of the stability monitor controllers and demonstrates the effectiveness of the designed monitor on a lab scale 2 kW dc microgrid system.

5. *Active Stability Control of DC Microgrids using Dynamic Virtual Immittance* (in submission): This paper presents an active stabilization method for dc microgrids based on a dynamic virtual immittance (DVI), where immittance is used to combine impedance and admittance. The proposed DVI may be emulated at the terminal of one of the converters already in the dc microgrid, or emulated using an additional converter with a fraction of the power rating, added to the system and interfacing capacitive or battery energy storage. A feedback loop regulates the stability margin of the dc microgrid system. The output of the stability regulator continuously adjusts the parameters of the DVI to add just enough damping at the critical frequency as required to maintain the reference stability margin, thereby optimizing the reactive power required to support the system stability. In this paper, the stability margin and critical frequency are continuously evaluated using a continuous stability margin monitor [7] that is implemented in the converter emulating the DVI. In general, however, application of the DVI can use any system stability monitor that provides information about the system stability and critical frequency. The stability regulator, monitor, and DVI are implemented in a single CMOD A7 field-programmable gate array (FPGA) [9] using fixed-point computations, along with the primary control functions of the converter, demonstrating low computational cost. Its performance is demonstrated on a lab scale 2 kW dc microgrid.

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CHAPTER 2

Nodal Impedance-Based Stability Analysis of Dc Nanogrids

Nodal Impedance-Based Stability Analysis of Dc Nanogrids

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Abstract— **With the growing interest in electrification and interfacing of clean energy and energy storage, new challenges are emerging in stability analysis and control of such systems. Existing stability analysis methods work well for systems with pre-defined power flow and fixed architecture, and most lead to design criteria for source and load impedances. However, the methods presented in the literature are not suitable for analyzing dynamically changing systems, especially for online stability evaluation and monitoring. The nodal impedance-based stability analysis method presented in this paper extends the boundaries of the existing criteria and leads to a practical and effective solution for online stability evaluation and monitoring. Hardware results are provided to validate the proposed analysis method on a scaled-down nanogrid system.**

Keywords—impedance, stability, dc nanogrid, microgrid, Nyquist

I. INTRODUCTION

Growing penetration of renewable energy and a growing interest in electrification of transportation has led to new challenges in terms of stability analysis and control of such systems. Future dc nanogrids are expected to involve dynamically changing systems with bi-directional converters incorporating energy storage, plug and play loads and system reconfiguration. Fig. 1 shows how the future dc nanogrid systems are expected to be configured. Examples of such systems are found in electric aircraft and electric ships [1-4]. The complexity of the emerging dc nanogrids has led to a renewed interest in stability analysis of such systems [5-8].

There are two main causes of stability degradation within a dc nanogrid, 1) interactions of the feedback loop created by the input/output impedances of the interconnected converters and 2) the constant power load effects that exhibit negative incremental impedance. These two causes can compromise the stability of both the converters and the complete interconnected nanogrid system. Several approaches have been proposed for modeling the dynamics of such systems, including eigenvalue based full system modeling [9], nonlinear modeling [10], and impedance-based modeling techniques. Among these, impedance-based modeling techniques have been shown to facilitate design

specifications for sources and loads [11-15]. The existing criteria are restrictive in that they require connected converters identifies as sources and loads, and require grouping of sources and loads in order to apply the criteria. This becomes increasingly difficult in systems with reconfigurations, bidirectional converters and power flow changes. Furthermore, the existing criteria are not easily to apply online in a dynamically changing system such as that in Fig. 1.

This paper proposes a novel stability analysis method based on nodal analysis targeted for future dc nanogrid systems. The proposed method does not require source and load identification or grouping and hence can be applied easily in a dynamically changing system. Furthermore, it is shown that the analysis using the proposed method can be performed at the terminal of any converter in the dc nanogrid, making this an ideal candidate for online stability analysis. The proposed method provides necessary and sufficient conditions for stability, and leads to new solutions for active stabilization.

The rest of the paper is organized as follows; Section II reviews impedance-based stability analysis methods to highlight the need for a new method, Section III presents the nodal impedance-based stability analysis method, Section IV presents
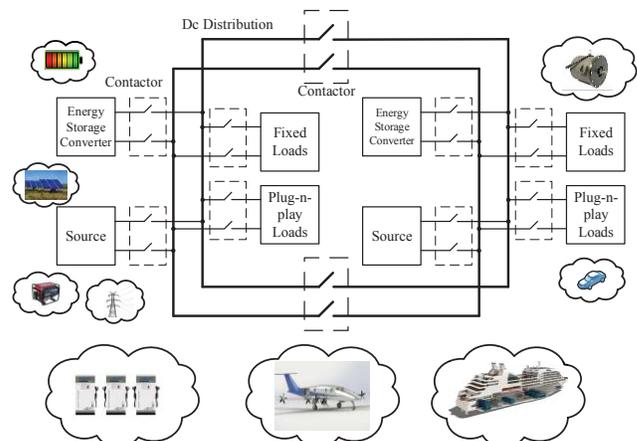

Fig. 1 Future dc nanogrid systems [20-27].

hardware test setup and results in order to validate the results and Section V concludes the paper by summarizing the findings and identifying the applications of the proposed method.

II. IMPEDANCE-BASED STABILITY ANALYSIS

Impedance-based stability analysis is done by representing sources and loads by their output impedances, as shown in Fig. 2. For a multi-source multi-load system, traditional methods typically group sources and loads into a single-source single-load system using various methods [12-13, 16]. The analysis is then performed in an identical manner on the simpler system. For the voltage source system shown in Fig. 2, the dc bus voltage is found as

$$V_{bus} = V_s\left(\frac{Z_L}{Z_s+Z_L}\right) = \frac{V_s}{Z_L}\left(\frac{1}{1+\frac{Z_s}{Z_L}}\right), \quad (1)$$

where V_s and Z_s represent the Thevenin equivalent voltage and output impedance of the source respectively, and Z_L represents the input impedance of the load. The right-hand-side of (1) forms a closed loop system whose stability is determined by the following conditions.

1) Z_L must not have a right half plane (RHP) zero, and

2) Minor loop gain Z_s/Z_L must satisfy the Nyquist criterion.

If these conditions are satisfied, the system is guaranteed to be stable. If the source has a current source behavior, it is represented by its Norton equivalent, as shown in Fig. 2, and the load current is found as

$$I_L = I_s\left(\frac{Z_s}{Z_s+Z_L}\right) = \frac{I_s}{Z_s}\left(\frac{Z_s}{1+\frac{Z_L}{Z_s}}\right), \quad (2)$$

where I_s is the Norton equivalent current source and I_L is the load input current. The conditions for stability are then derived as follows.

1) Z_s must not have a RHP zero, and

2) Minor loop gain Z_L/Z_s must satisfy the Nyquist criterion.

It is interesting to note that by using Thevenin equivalent or Norton equivalent circuit for the source, we get completely opposite conditions for stability. One would expect the conditions of stability to be the same as any Thevenin equivalent circuit can be mathematically represented as a Norton equivalent as well. It will be shown in Section III that the conditions leading from (1) and (2) are in fact a subset of the conditions required for stability and that both the minor loop gain and its inverse can equivalently represent the system. The conditions derived from (1) and (2) lead to simpler application of the Nyquist criterion than the general method proposed in this paper, and would still be preferred at system design-time.

Using the impedance-based stability analysis, several design criteria have been proposed in the literature. Fig. 3 shows commonly used criteria, including the Middlebrook criterion [16], gain margin phase margin (GMPM) criterion [12], opposing argument criterion [13], the energy source analysis consortium (ESAC) criterion [17] and the passivity-based stability criterion [18]. In general, the system is guaranteed to be stable if the Nyquist plot of the impedance loop gain does not
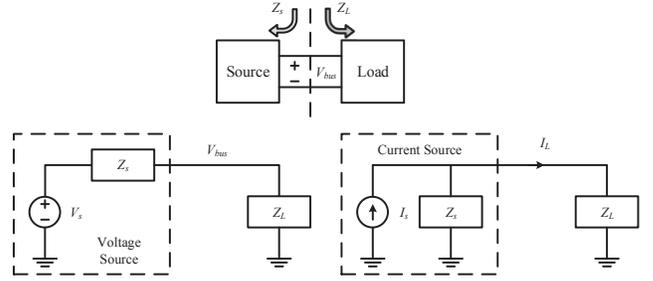

Fig. 2   Traditional impedance-based stability analysis.

enter the forbidden region defined by each criterion, provided that the converters/loads are stable individually [11].

The existing stability analysis methods and criteria become increasingly hard to apply on emerging dc nanogrid systems such as that shown in Fig. 1. The bidirectional energy storage converters (ESCs) can be a source or a load depending on the operating point. Using the existing methods the ESC would need to be grouped differently based on the operating point, making the minor loop gain dependent on the operating point. Furthermore, evaluation of stability using the existing methods which require source/load grouping would have a different interface evaluated every time a converter (source or load) is added or removed from the system. The evaluation would require complete system information (for analytical methods) or changing the point of injection (for measurement based methods) in order to reduce the system to the simpler form of Fig. 2. The existing methods also do not lend themselves to online monitoring of stability and active stabilization in a dynamically changing system of Fig. 1.

III. PROPOSED NODAL IMPEDANCE-BASED STABILITY ANALYSIS

The impedance-based analysis approach presented in this paper is based on nodal impedance analysis. The most important aspect of the proposed method is that unlike the existing criteria that typically group sources and loads into separate subsystems, the proposed method does not require converters to be defined as sources or loads, hence becoming impervious to changes in power flow, addition/removal of converters from the system or system reconfigurations. By allowing the use of the generalized
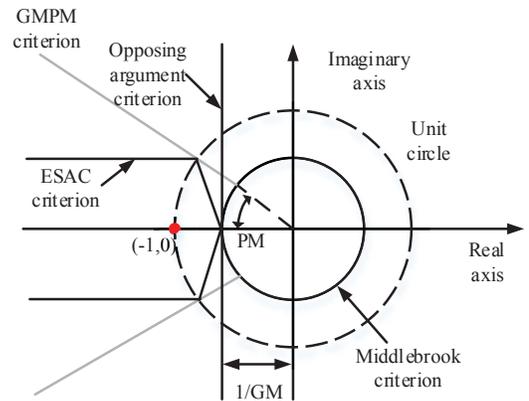

Fig. 3   Impedance-based stability criteria from literature.

Nyquist stability criterion, the proposed method provides necessary and sufficient conditions for stability. Furthermore, the proposed method performs the stability analysis at the terminal of one (any) of the converters connected at a system node, making this an ideal candidate for online implementation based on online measurement.

A. Derivation of the Nodal Stability Criteria

Consider a system with n converters (any of which could be sources or loads) connected to the dc bus of a nanogrid, as shown in Fig. 4. The sources and loads are represented by their Thevenin equivalent models. The small-signal current injected by i-th converter into the dc bus is given by

$$i_i = \frac{V_i - V_{bus}}{Z_{oi}}, \qquad (3)$$

where V_i and Z_{oi} are the Thevenin equivalent voltage and output impedance of the converter as shown in Fig. 4, and all of the variables of (3) are functions of the Laplace variable 's'. Adding the currents from all converters and equating to zero, we get

$$\sum_{i=1}^{n} \frac{V_i}{Z_{oi}} = V_{bus}\left(\frac{1}{Z_{o1}} + \frac{1}{Z_{o2}} + \cdots + \frac{1}{Z_{on}}\right). \qquad (4)$$

Each term of the summation on the left-hand side of (4) represents the current injected into an ideal dc bus by i-th converter. If the converters in Fig. 4 were represented by Norton equivalent rather than Thevenin equivalent, the V_i/Z_{oi} terms in the summation would be replaced by the Norton current sources I_i, but the right-hand side of (4) will remain the same. Thus, there is no loss of generality by representing converters with their Thevenin equivalent. From (4), the small-signal voltage at the dc bus is found as

$$V_{bus} = \left(\sum_{i=1}^{n} \frac{V_i}{Z_{oi}}\right)(Z_{o1}//Z_{o2} \ldots //Z_{on}), \qquad (5)$$

where V_i are the ideal voltage sources or loads, and Z_{oi} are the output impedances. For the general form shown in (5), the small-signal stability of the dc bus voltage depends on two things:
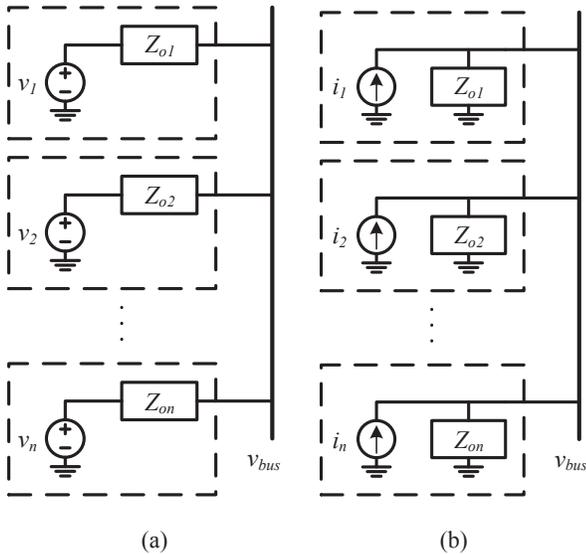
1) Individual sources and loads, V_i/Z_{oi} (or I_i), are stable when connected to an ideal dc bus, i.e. Z_{oi} does not have any right-half plane (RHP) zeros, and
2) The bus impedance, which is a parallel combination of all of the converter impedances, looking into the node, is stable.

Generally, each source and load in the system is designed to be stable individually, so the first condition is automatically satisfied. Hence, the dc bus voltage stability can be evaluated by the bus impedance at the node which represents the impedance interactions. This forms the nodal stability criteria which provides necessary and sufficient conditions for stability.

B. Evaluation of Stability from Bus Impedance

The overall bus impedance is comprised of n impedances which are connected in parallel. By partitioning the system in different ways, this parallel combination can be expanded in $\sum_{i=1}^{n-1}\binom{n}{i}$ ways. As illustrated in Fig. 5, one example of the expansion at the terminal of arbitrary converter 1 can be given as

$$Z_{bus} = Z_{o1}//Z_{o2}\ldots//Z_{on} = \frac{Z_{o1}(Z_{o2}\ldots//Z_{on})}{Z_{o1}+(Z_{o2}\ldots//Z_{on})} = \frac{Z_{o1}Z_{away,1}}{Z_{o1}+Z_{away,1}}, \quad (6)$$

where $Z_{away,1} = Z_{o2}\ldots//Z_{on}$, as shown in Fig. 5. In a similar way, the generalized form of the bus impedance seen from the terminal of i-th converter can be expressed as

$$\frac{Z_{oi}Z_{away,i}}{Z_{oi}+Z_{away,i}} = \frac{Z_{oi}}{1+\frac{Z_{oi}}{Z_{away,i}}} = \frac{Z_{away,i}}{1+\frac{Z_{away,i}}{Z_{oi}}}, \qquad (7)$$

where Z_{oi} is the output impedance of converter i and $Z_{away,i}$ is the rest of the bus impedance excluding Z_{oi}. Conceptually, $Z_{away,i}$ can be seen as the impedance of the system looking from the terminal of i-th converter. Equation (7) shows that the bus impedance forms a closed loop system whose minor loop gain, which is used to evaluate system stability, can be defined as either $Z_{oi}/Z_{away,i}$ or $Z_{away,i}/Z_{oi}$. In the preceding derivation, none

Fig. 4 A nanogrid system with n converters; (a) Thevenin equivalent and (b) Norton equivalent.
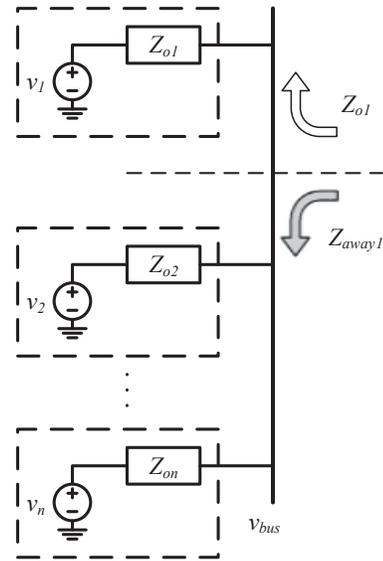

Fig. 5 System partitioning corresponding to one possible expansion of bus impedance.

of the converters connected to the dc bus were classified as sources or loads, which emphasizes that regardless of the power flow direction, the system stability can be evaluated by evaluating the minor loop gain formed by the expansion given in (7).

Assuming that the first stability condition defined in the previous subsection is satisfied and all converters are stable individually, the overall system is stable if and only if the closed loop system formed by the bus impedance is stable. With the minor loop gain given in (7), the system is stable if the Nyquist plot of the ratio $Z_{oi}/Z_{away,i}$ or $Z_{away,i}/Z_{oi}$ satisfies the Nyquist stability criterion. It is important to note here that in a nanogrid system, $Z_{away,i}$ consists of a complex combination of impedances which may include cable impedances, contact impedances, parameter variations and power flow variations. One or more of these may cause $Z_{away,i}$ to have RHP zero, which in turn causes a RHP pole in the minor loop gain. Hence, to analyze the stability in such cases, use of the generalized Nyquist criterion is required [19]. By allowing this, necessary and sufficient conditions for stability are obtained in all cases since no assumptions are made about $Z_{away,i}$.

IV. HARDWARE SETUP AND RESULTS

A small system emulating essential parts of a dc nanogrid, including a source converter, a load converter and a bidirectional energy storage converter (ESC), has been built to validate the proposed stability analysis and evaluation approach, as shown in Fig. 6. In the system illustrated in Fig. 6, where all converters are synchronous buck converters, the source and load converters are rated for 100 W, the ESC is rated at 20 W, and the bus voltage is 5 V. The load converter has a 4.7 uH input filter to limit EMI injection into the bus. The source converter follows a droop characteristic to regulate the output voltage based on the load. The load converter regulates its output load voltage, hence appearing as a constant power load to the dc bus. The bidirectional converter regulates its output current to/from the dc bus based on a voltage droop.

A. System Control and Impedance Modeling

The source converter and the ESC each have a fast current control loop regulating their output currents. Each of them have an outer loop regulating the output voltage with a voltage reference following the droop characteristics shown in Fig. 7. For the source converter, the PI controllers for the current and voltage loops were designed assuming a 100 W resistive load. For the ESC, the PI controllers were designed assuming the droop resistance of the source converter as the load. The load converter regulates its output voltage and feeds a 0.1 Ω resistive load, appears as a constant power load on the dc bus with the dc characteristics shown in Fig. 7. The detailed control diagram for the source converter, with its small-signal model, is shown in Fig. 8. The ESC has the same control structure as the source converter with the difference in the current reference range and hence has identical impedance model. The controller parameters for the three converters are presented in Table 1.

Based on the small-signal model shown in Fig. 8, the output impedance of the source and ESC is derived as
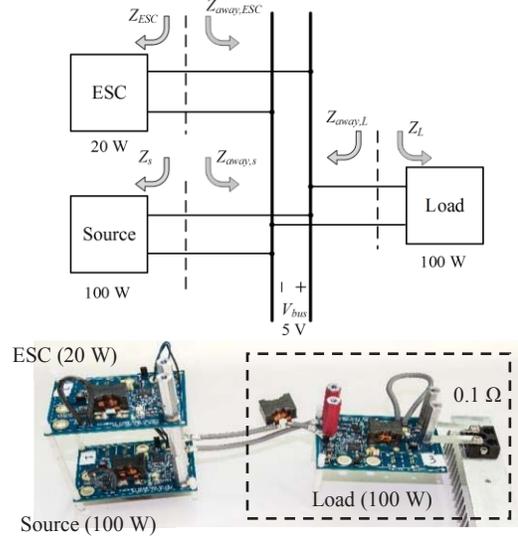
Fig. 6 Hardware Setup; System diagram (Top), picture of actual hardware (Bottom).

$$Z_{source} = Z_{ESC} = \frac{Z_L + V_{in}G_{ci}(1+G_{cv}R_{drp})}{1+\frac{Z_L}{Z_c}+V_{in}G_{ci}G_{cv}},\qquad(8)$$

where the variables in (8) are defined in Fig. 8. The impedance model for the ESC is identical to that of the source converter with the difference in the control parameters as listed in Table 1. For the load converter, the input impedance is derived in a similar manner as

$$Z_{Load} = Z_{Lin} + Z_{cin}//Z_{conv},\qquad(9)$$

where Z_{Lin} and Z_{cin} are series and shunt branches of the LC input filter of the load converter, and Z_{conv} is the input impedance of the load converter with output voltage control, given by

$$Z_{conv} = \frac{1+\frac{Z_L}{R_{load}}+\frac{Z_L}{Z_c}+V_{in}G_{cv}}{D^2\left(\frac{1}{Z_c}+\frac{1}{R_{load}}\right)-G_{cv}I_{in}},\qquad(10)$$
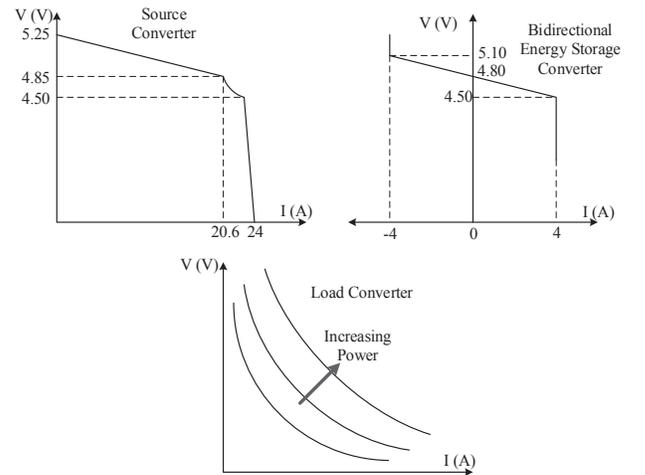
Fig. 7 Dc characteristics of the source (Top left), ESC (Top right) and load converter (Bottom).

Fig. 8   Detailed control diagram and small-signal model of the source converter.

Fig. 9   Impedance models; Source converter (solid), bidirectional converter (dash) and load converter (dot-dash).

where the operating point is defined by the duty ratio, D, and the input current, I_{in}. The bode plots of the impedance models are shown in Fig. 9. For the load converter, the low frequency impedance changes with the operating point, and the case shown in Fig. 9 is at 45 W of power.

B. Stability Analysis Case Studies

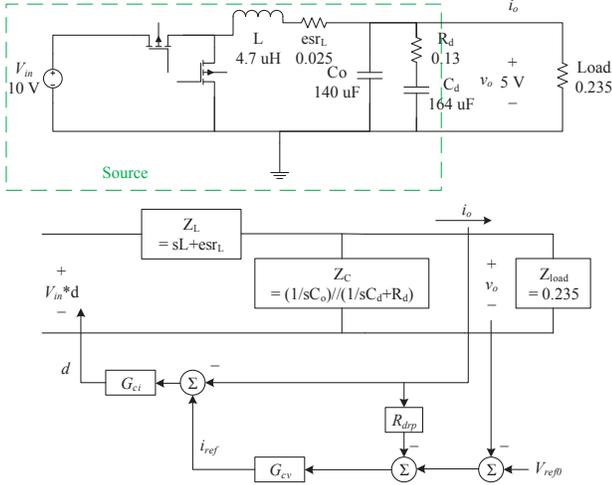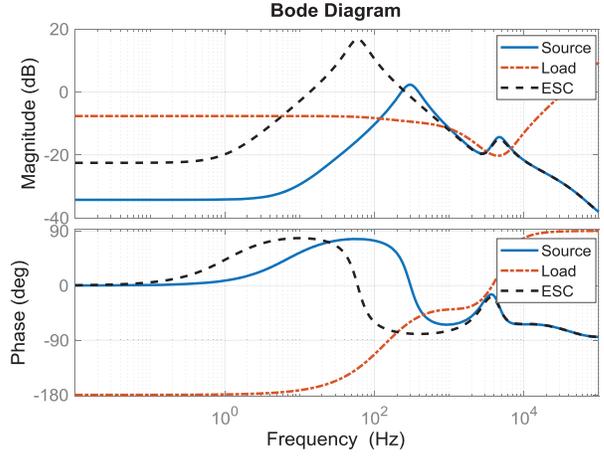In order to validate that the proposed method predicts accurate system stability, the test setup of Fig. 6 was operated under two scenarios; one in which the system is stable and another in which the system is unstable. It is shown that, in both scenarios, the proposed method predicts correct stability regardless of the system partitioning or power flow configurations. The system is started up by enabling the droop controls of ESC and source converters and zero load converter power. The load power is then ramped up to 40 W. At this point, the dc bus voltage is at 5 V and the ESC is drawing about 15 W of power from the dc bus. For the first scenario, the load power is stepped from 40 W to 45 W to capture the response of the system in the stable region. The response is shown in Fig. 10(a). It can be seen in Fig. 10(a) that the system remains stable after the step although with a small phase margin causing underdamped oscillations. For the second scenario, the load power is stepped from 45 W to 50 W to capture the response of the system in the unstable region. The response is shown in Fig. 10(b). As shown in Fig. 10(b) , the oscillation grow slowly after the step, indicating the system at the boundary of instability. The oscillations grow until the overvoltage protection in the source converter triggers a system shutdown.

The behavior of the system is hereby analyzed using the proposed method. With the Z_{source}, Z_{Load} and Z_{ESC} as given by (8)-(10), the generalized Nyquist stability criterion is applied at the interface of each converter by combining the other two impedances in parallel. The Nyquist plots of the two scenarios are shown in Fig. 11. In each of the Nyquist plots shown in Fig. 11, the solid lines show the plots with 45 W load power while the dashed lines show the plots with 50 W load power. Fig. 11(a) and (d) show the Nyquist plots of the impedance ratio at the source converter terminal, i.e. $Z_{source}/Z_{away,source}$ where

(a)

(b)
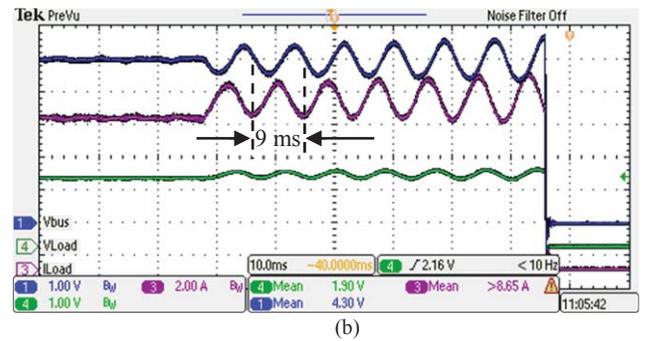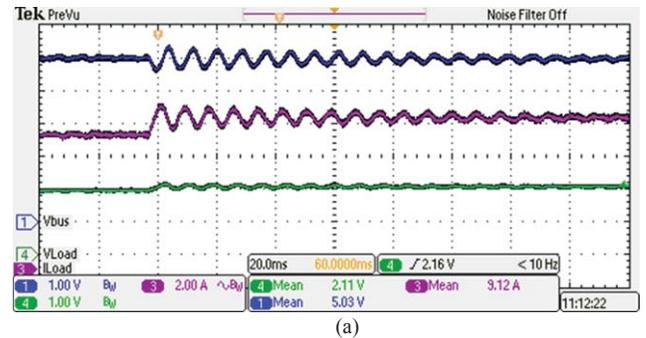
Fig. 10 The response of the system under (a) stable case (45 W) and (b) unstable case (50 W), showing Dc bus voltage (top), load converter input current (middle) and load resistor voltage (bottom).

TABLE I.   CONTROL PARAMETERS OF CONVERTERS IN TEST SETUP

	Current control bandwidth (Hz)	Voltage control bandwidth (Hz)	Droop resistance
Source converter	1000	500	0.0194
Bidirectional ESC	3000	100	0.0750
Load converter	N/A	150	N/A

Fig. 11 Nyquist plots of the minor loop gain at the interface of, (a) source converter, (b) ESC, (c) load converter, (d) source converter zoomed around (-1,0), (e) ESC zoomed and (f) load converter zoomed.

$Z_{away,source}$ is defined as the parallel combination of the other two impedances as shown on Fig. 11. It is evident that the plot with 45 W load power does not encircle the critical point but is close to it, indicating a stable system but with low margin. The plot with 50 W load power crosses right though the critical point, indicating an unstable system. Furthermore, the period of oscillations of 9 ms shown in Fig. 10 agrees with the frequency where the Nyquist plot crosses the critical point (105 Hz in this case). The analysis at the terminal of the ESC is shown in Fig. 11(c) and (e). Similar to the source terminal, the Nyquist plot does not encircle the critical point with 45 W of load power but crosses through it with 50 W load power.

The analysis at the load converter terminal is shown in Fig. 11(e)-(f). This is a case where the simplified Nyquist criterion of non-encirclement of critical point fails. However, looking closely at Fig. 11(c) and (f), we can see that for the 45 W case, the Nyquist plot crosses the real axis twice beyond the critical point; once clockwise and once counter-clockwise. Applying the generalized Nyquist criterion [19], this results in zero net encirclements of the critical point and hence a stable system. For the 50 W case, the counter-clockwise crossing goes though the critical point, resulting in net clockwise encirclement of the critical point. This shows that, even at the load converter terminal, the minor loop gain given by $Z_{Load}/Z_{away,Load}$ gives a correct prediction of stability or instability.

It is important to note that all three interfaces predict the same frequency of unstable oscillations, i.e. 105 Hz, which emphasizes their equivalence in the stability prediction. The stability margin for the stable case, h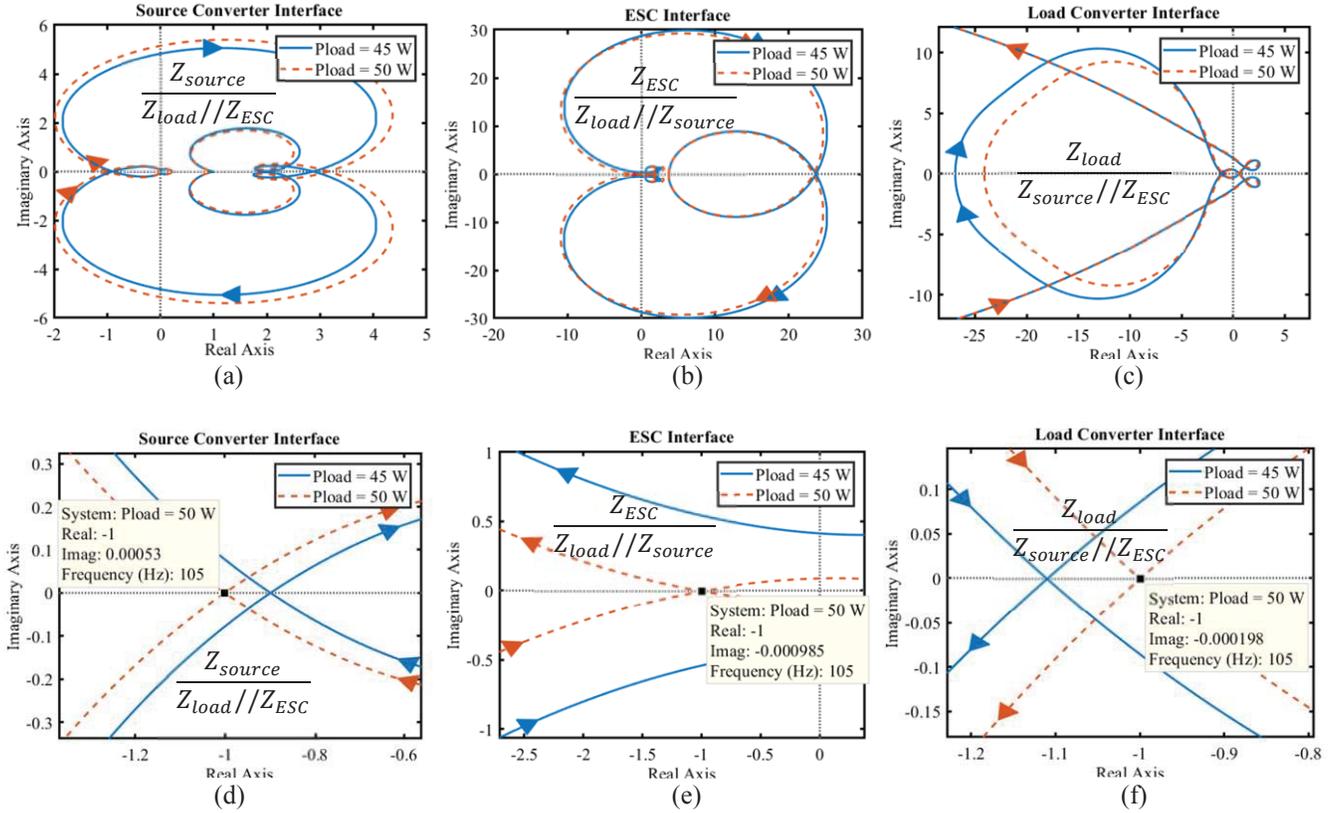owever, is different in each case, as evident from Fig. 11(d)-(f). This is because the phase margin of the impedance minor loop gain depends on the relative sizes of the converter impedance to the rest of the system. A larger phase margin indicates more damping available across the interface. A larger gain margin indicates more room for variation in the impedance magnitude of the ESC or the rest of the system. For the load converter, the stability margins can be evaluated based on the generalized Nyquist method [19].

V. CONCLUSIONS

A novel method for analyzing stability of dc nanogrids was presented in this paper. It was shown through analysis and hardware results that stability of a dc nanogrid can be evaluated at the terminal of any of the parallel-connected converters, regardless of the power flow configurations. Furthermore, it was shown that the proposed method provides necessary and sufficient conditions for system stability. Nodal impedance-based stability analysis can be used to a great advantage by selecting a source converter or an energy storage converter as the terminal of choice for analysis and using it to measure the combined impedance of the rest of the system. The measured impedance would account for parameter variations, capture the effects of cable impedances, contact impedances and adapt to the dynamically changing system. The measured impedance, Z_{away}, would then be used along with the output impedance of the measuring converter to perform the online stability analysis.

A requirement for the converter performing the online impedance measurement of Z_{away} would be high control bandwidth, which can be a design consideration for an ESC.

Another application of the proposed method would be to analyze if an existing system would remain stable after the addition of a new converter in the system. The impedance of the system looking into the dc bus where the new converter is to be inserted would be measured or evaluated. This would be used as Z_{away} in the denominator, while the output impedance of the new converter used in the numerator of the loop gain to be analyzed for stability. The proposed nodal impedance-based stability analysis method can be further utilized in providing active damping where needed. The analysis performed at the terminal of an ESC, for example, could be used to determine the stability margin which indicates the amount of damping in the system. The high-bandwidth controller of the ESC could then be used to provide active damping in the system by targeting the critical frequencies identified in the minor loop gain. The applications discussed here are all topics of ongoing research which are enabled by the proposed nodal impedance-based stability analysis.

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CHAPTER 3

Continuous Stability Monitoring of DC Microgrids Using Controlled Injection

Continuous Stability Monitoring of DC Microgrids Using Controlled Injection

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Abstract—**Emerging dc microgrids incorporating energy storage are presenting new challenges in system design and stability analysis. Several methods have been proposed in literature for online stability evaluation of such dc microgrids using impedance-based stability analysis. This paper presents a method for continuous monitoring of system stability that is not computationally intensive and can be added as a supplemental function to existing converters in the system so that no additional power hardware is required. The proposed method evaluates stability continuously and can be used as a proactive approach for monitoring and maintaining system stability. Hardware results are presented to validate the proposed continuous stability monitor, which shows its effectiveness in predicting the system stability margins.**

Keywords—impedance, stability, dc microgrids, monitoring

I. INTRODUCTION

Owing to the continued push towards electrified transportation and integration of renewables, the dc microgrids of the future are expected to be much more dynamic than they have been in the past. Future dc microgrids are expected to incorporate different kinds of sources such as renewable energy and fuel-based generators. They are expected to be re-configurable, have bidirectional converters interfacing energy storage, and may have constant power, intermittent or plug and play loads. Examples of such systems can be found in all-electric aircraft, electric ships and dc fast charging stations [1-3] and are expected to be configured as shown in Fig. 1. Stable operation of these microgrids is challenged by the negative incremental resistance behavior of the constant power loads as well as interactions among the controllers of the interconnected converters [4-5].

Traditional methods of designing the system to handle all possible scenarios lead to an overdesigned system including oversized filters and slow controllers. To avoid system overdesign, active stabilizing techniques and adaptive tuning techniques have been proposed. In [6-8], the authors used online measurements of system health [6] or frequency response [7-8] to auto-tune the digital controllers of the converters to improve transient performance and stability. In [9], the authors proposed an active stabilizer to add virtual damping in the system based on a measured oscillation frequency at the onset of instability. Application of these auto-tuning and active damping techniques requires online measurement of system impedances or system health, for which several methods have been proposed.

These methods typically use wide-band perturbation followed by a Fourier transform to measure impedances and derive the system stability or tuning parameters from them. In [10], the authors proposed using wideband perturbation to measure ac grid impedance for adaptive control. In [11], the authors used cross-correlation methods to find the input and output impedances of cascaded converters. Ref. [12] used an additional converter in a multi-source system to measure the source and load subsystem impedances and apply the Nyquist criterion to find the system stability. In [13], the authors proposed a medium voltage impedance measurement unit to measure the impedance of the source and load subsystem to evaluate stability in a multi-source multi-load system. A common drawback of the existing methods is that they are computationally intensive and, for microgrids with multiple sources and loads, require an additional converter to perform the analysis [12-13].

This paper presents a novel system stability monitor which can be added onto any existing converter in the system as an auxiliary function and that continuously monitors the stability margin of the interconnected system. The stability margin evaluation is enabled by Nodal Stability Analysis which has been recently proposed as a generalized impedance-based stability analysis method especially suited for dynamic dc microgrids with various interconnected sources, loads and bidirectional converters [14]. The monitor itself is derived from a continuous monitoring method developed to monitor the phase margin of a converter loop gain [15-16]. The proposed
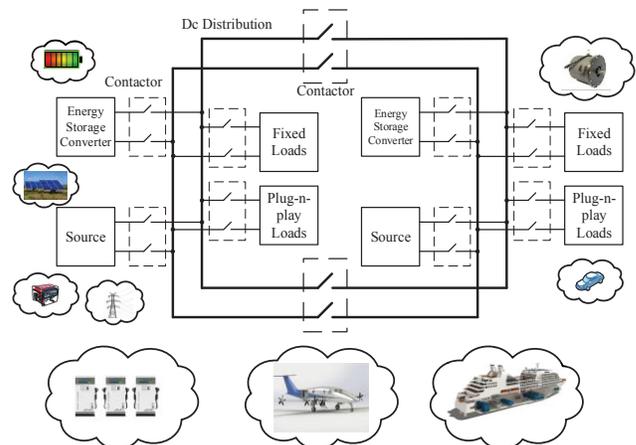

Fig. 1.   Representative future dc microgrid system [21-28].

continuous monitor injects a controlled single-frequency perturbation using one of the converters already in the system, with a small amplitude that does not affect the normal operation. The proposed method can be used in any interconnected system for proactively monitoring and maintaining the system stability, and its continuous nature would enable development of new techniques in adaptive stability enhancement of dc microgrids.

The paper is organized as follows: Section II summarizes the nodal stability analysis method that enables the continuous monitor, Section III describes the continuous monitor and its various controllers, Section IV derives the small-signal model for the monitor and designs the controllers, Section V presents the experimental results to validate the proposed monitor and Section VI summarizes the findings.

II. NODAL STABILITY ANALYSIS

The proposed continuous system stability monitoring technique evaluates stability using measurements at the terminal of the converter that incorporates it. The approach relies on measurements directly available to the converter, namely the dc link voltage at its output and its own output current. This data provides information about the system impedance as seen from the output terminals of the monitoring converter. The proposed approach uses impedance-based stability analysis to evaluate the stability margin. However, the monitoring converter cannot divide the system into source and load subsystems as required by traditional impedance-based stability analysis methods [17-19]. This is because the impedance that the monitoring converter sees is the parallel combination of all sources, loads and bidirectional converters connected in the system and there is no way for it to distinguish sources from loads in the impedance measurement at its output terminals. Hence, traditional methods cannot be used with the proposed monitor. The Nodal Stability Analysis proposed in [14] and summarized here presents an impedance-based analysis method that does not require identification or grouping of sources and loads, making it the ideal candidate for such applications.

Consider a dc microgrid comprising n converters connected to a common dc bus, as shown in Fig. 2, where all converters are
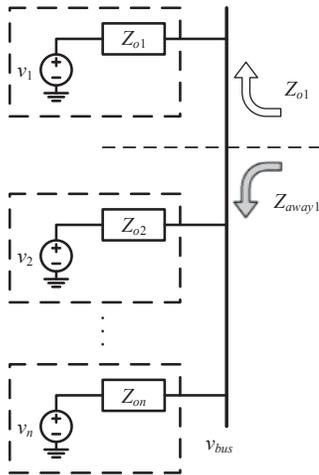

Fig. 2. A generic dc microgrid showing an arbitrary system partitioning.

represented by their Thevenin equivalent. The small-signal dc bus voltage is given by

$$V_{bus} = \left(\sum_{i=1}^{n} \frac{V_i}{Z_{oi}} \right) Z_{bus}, \qquad (1)$$

where

$$Z_{bus} = (Z_{o1}//Z_{o2}// ...//Z_{on}). \qquad (2)$$

All variables in (1) and (2) are functions of the Laplace variable s, V_i and Z_{oi} are the Thevenin equivalent voltage and output impedance of the i-th converter, respectively, and Z_{bus} is the overall bus impedance from the parallel combination of all the converter output impedances. Assuming the converters are individually stable when connected to an ideal dc bus, the system stability is given by the stability of Z_{bus} [14].

The stability of the dc bus impedance Z_{bus} is determined in [14] by expanding (2). One such expansion of Z_{bus} is given by

$$Z_{bus} = \frac{Z_{o1} Z_{away,1}}{Z_{o1} + Z_{away,1}} = \frac{Z_{o1}}{1 + \frac{Z_{o1}}{Z_{away,1}}} = \frac{Z_{away,1}}{1 + \frac{Z_{away,1}}{Z_{o1}}}, \qquad (3)$$

where $Z_{away,1}$ is the parallel combination of all converter impedances except Z_{o1}. The expansion shown in (3) corresponds to partitioning the system at the terminal of the arbitrary converter 1, as shown in Fig. 2. Equation (3) shows Z_{bus} expressed in the form of a closed loop system representing interactions of all the interconnected converters and with a minor loop gain represented by the ratio of the output impedance Z_{o1} and the impedance of the rest of the system, $Z_{away,1}$. From (3), the dc bus impedance is stable if the minor loop gain $Z_{o1}/Z_{away,1}$ satisfies the Nyquist stability criterion [14].

It is shown through hardware results in [14] that the minor loop gain Z_o/Z_{away} can be evaluated at the terminal of any converter in the system, and it is not necessary to group or identify source and load converters in Z_{away} to perform the analysis. This property is utilized in this paper to develop the continuous monitoring technique which evaluates the system stability by continuously measuring the crossover frequency and phase margin of the minor loop gain given by the ratio of Z_o to Z_{away}.

III. CONTINUOUS STABILITY MARGIN MONITOR

From (3), the minor loop gain of the microgrid system is given by $Z_o/Z_{away,}$. If both impedances are perturbed using the same current perturbation i_o, then the minor loop gain can be written as

$$\text{Minor loop gain} = \frac{Z_o}{Z_{away}} = \frac{V_s I_o}{V_o I_o} = \frac{V_s}{V_o}, \qquad (4)$$

where v_s is the response of Z_o and v_o is the response of $Z_{away,}$ to i_o. Utilizing the freedom of system partitioning [14], any converter in the system can be assigned the monitoring task. The assigned converter would inject a current perturbation in the
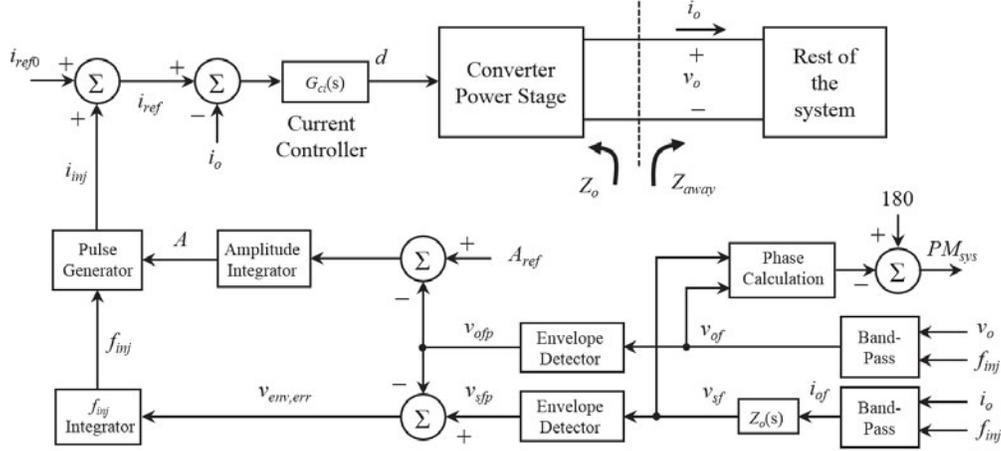
Fig. 3. Schematic of continuous stability margin monitor .

system and directly measure v_o (the response of Z_{away}) and i_o, as indicated in the overall schematic of the continuous monitor in Fig. 3. The measured i_o is then used with the analytical model of the converter output impedance to calculate v_s. With v_s and v_o, the system stability margin can be determined since the frequency at which the amplitudes of v_s and v_o match is the minor loop gain crossover frequency, and the phase margin of the minor loop gain is the phase difference of v_s and v_o at that frequency [15].

A. Injection and Response Filtering

As shown in Fig. 3, a pulse generator outputs a square wave current reference i_{inj} with frequency f_{inj} and amplitude $\pm A$, which is added on top of the base current reference i_{ref0} and fed into the converter output current controller. The overall current reference, i_{ref}, looks like that shown in Fig. 4. The resulting i_o and the response voltage v_o are measured and fed into a band-pass filter tuned at the injection frequency f_{inj}. The band-pass filter is made online tunable and is of the form

$$G_{bp}(s) = \frac{\left(\frac{2\pi f_{inj}}{Q}\right)s}{s^2 + \frac{2\pi f_{inj}}{Q}s + (2\pi f_{inj})^2}, \quad (5)$$

where Q is the quality factor of the filter (usually set high), and f_{inj} is the same frequency at which i_{inj} is generated. The dynamic parameter f_{inj} in (5) requires that the parameters of the band pass filter be evaluated continuously as f_{inj} changes, making it essential that the rate of change of f_{inj} be much smaller than the value of f_{inj}. The outputs of the band-pass filter, i_{of} and v_{of}, contain only the frequency component of i_o at f_{inj} and its response
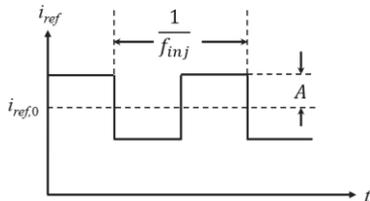

Fig. 4. Waveform of the current reference with square-wave perturbation.

to Z_{away} respectively. Filtered current, i_{of} is then fed into the analytical model of Z_o to calculate v_{sf}. A peak-detection algorithm is used to find the peak-to-peak amplitudes of v_{of} and v_{sf} at the injection frequency f_{inj}, given by v_{ofp} and v_{sfp}. The error between v_{ofp} and v_{sfp} is integrated to find the frequency where the error is zero, i.e. where $v_{sfp} = v_{ofp}$.

B. Injection Control and Phase Margin Evaluation

It is desirable to limit the amplitude of the voltage perturbation resulting from the injected current, and also to make sure that the response is detectable. To achieve that, the amplitude of voltage perturbation, v_{ofp}, is compared to a reference amplitude A_{ref} and fed into a slow integrator which outputs the amplitude of the current injection A. From (4), the goal is to inject a perturbation at the impedance crossover frequency where $v_{sfp} = v_{ofp}$. This allows us to define a feedback error

$$v_{env,err} = v_{sfp} - v_{ofp}, \quad (6)$$

which is integrated to output the injection frequency f_{inj}. The frequency integrator changes the injection frequency until it reaches the impedance crossover frequency. Correct operation of this integrator requires the correct sign of the error to be used as well as a good estimate for the integrator initial condition, which can be estimated from analytical models or a one-time measurement using a frequency sweep or other wide-band methods [10-13]. According to (4), as the error of (6) goes to zero, the injection frequency, f_{inj}, will converge to the crossover frequency of the minor loop gain (4), and given by

$$f_{c,sys} = f_{inj}\big|_{v_{env,err}=0}, \quad (7)$$

where $f_{c,sys}$ is the minor loop gain crossover frequency. Also, when (6) goes to zero, the system phase margin, hereby called PM_{sys}, is proportional to the phase difference between v_{of} and v_{sf}, and is given by

$$PM_{sys} = 180\big(1 - 2\Delta t_{zc}f_{inj}\big)\big|_{v_{env,err}=0}, \quad (8)$$

where Δt_{zc} is the time difference between the zero crossings of v_{sf} and v_{of}.

IV. ANALYSIS AND DESIGN OF THE CONTINUOUS MONITOR

This section aims to discuss the modeling of the dynamics of the continuous monitor and the design of its two controllers, namely the f_{inj} integrator and amplitude integrator. The experimental setup from which the models are derived is discussed before the modeling of the monitor dynamics themselves.

A. Hardware Test Setup

To validate the proposed stability margin monitor, a test setup emulating essential parts of a dc microgrid, namely a source converter, a load converter and a bidirectional converter (emulating an energy storage interface) has been built as shown in Fig. 5. All converters in Fig. 5 are synchronous buck converters which are chosen for their well understood behavior and impedance models. The source converter and the load converter are each rated for 100 W and have the same control structure as in [14]. The source converter has an inner current control loop regulating its output current and an outer voltage controller with droop. The load converter regulates the voltage at its own output, thereby appearing as a constant power load to the dc bus. The impedance models of the source and the load converters are same as in [14].

The energy storage converter (ESC) is chosen as the continuous monitor of the system. Hence, its control structure is as shown in Fig. 3. The ESC regulates its output current with a constant reference while the injection is added on top of the constant current reference. The impedance model of the ESC, following similar derivation to [14], is given by

$$Z_{ESC} = \frac{Z_L + V_{in} G_{ci}}{1 + \frac{Z_L}{Z_c}}, \tag{9}$$

where V_{in} is the input voltage of the ESC, G_{ci} is the current controller, Z_L is the impedance of the inductor of the synchronous buck including its ESR, and Z_c is the impedance of the output shunt filter branch. To evaluate the system stability, the following minor loop gain is evaluated,

$$\text{Minor Loop Gain} = \frac{Z_{ESC}}{Z_{away,ESC}} = \frac{Z_{ESC}}{Z_{SC}//Z_{Load}} = \frac{v_{sf}}{v_{of}}, \tag{10}$$

where Z_{sc} is the impedance of the source converter while Z_{load} is the impedance of the load converter. The parallel combination of the source and load converter impedances is seen by the ESC. The controller bandwidths of the three converters are listed in Table 1 below. To help in validating the proposed monitor over a wide operation range, the parameters are intentionally chosen such that the system crossover frequency and phase margin changes significantly as the load converter increases its power.

B. Modeling of the Continuous Monitor Dynamics

Following an approach similar to [15], we can find the transfer function from f_{inj} to envelope error, i.e.

$$G_{f_{inj},v_{err}}(j\omega_m) = \frac{\hat{V}_{env,err}(j\omega_m)}{\hat{f}_{inj}(j\omega_m)}, \tag{11}$$

where $v_{env,err}$ is given by (6). Similar to [15], the overall transfer function of (11) can be evaluated by evaluating the difference of two transfer functions

$$G_{f_{inj},v_{s,env}}(j\omega_m) = \frac{\hat{V}_{s,env}(j\omega_m)}{\hat{f}_{inj}(j\omega_m)}, \tag{12}$$

and

$$G_{f_{inj},v_{o,env}}(j\omega_m) = \frac{\hat{V}_{o,env}(j\omega_m)}{\hat{f}_{inj}(j\omega_m)}, \tag{13}$$

where $v_{s,env}$ represents the small-signal variations in v_{sfp} and $v_{o,env}$ represents the small-signal variations in v_{ofp}. The overall transfer function is then found as

$$G_{f_{inj},v_{err}}(j\omega) = G_{f_{inj},v_{s,env}}(j\omega) - G_{f_{inj},v_{o,env}}(j\omega). \tag{14}$$
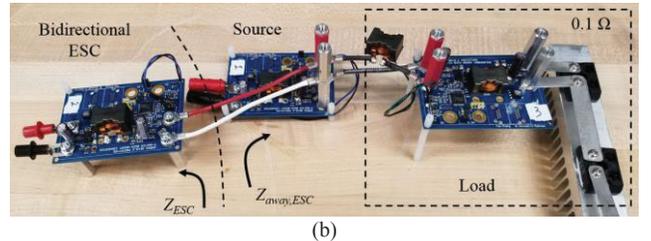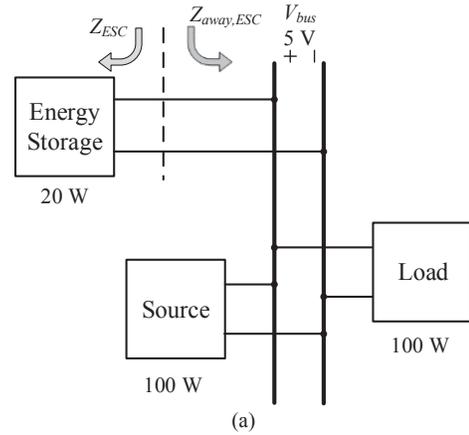

(a)

(b)

Fig. 5. Hardware Setup; (a) system diagram and, (b) picture of actual hardware.

TABLE I. CONTROL PARAMETERS OF CONVERTERS IN TEST SETUP

	Current control bandwidth (Hz)	Voltage control bandwidth (Hz)	Droop resistance
Source converter	1000	500	0.0194
Bidirectional ESC	2000	N/A	N/A
Load converter	N/A	160	N/A

The derivation of the envelope dynamics follows [20], which treats the small-signal variations in frequency as frequency modulation of the square wave generation, filtered by the band pass filter of (5). Following [20], it can be shown that (12) and (13) can be evaluated as

$$G_{f_{inj},v_{env}}(j\omega_m) = \frac{4V_{in}}{\pi} \frac{(A_0 A_l^* + A_0^* A_u)}{\|A_0\|}, \quad (15)$$

where A_0, A_l and A_u are defined as

$$A_0 = G_{plant}(j\omega_m),$$
$$A_l = -\frac{1}{2w_m} G_{plant}[j(\omega_{inj} - \omega_m)],$$
$$A_u = \frac{1}{2w_m} G_{plant}[j(\omega_{inj} + \omega_m)]. \quad (16)$$

For evaluating (12), $G_{plant}(j\omega_m)$ in (16) is given by

$$G_{plant,v_s}(j\omega_m) = G_{i,ESC}(j\omega_m)Z_{ESC}(j\omega_m)G_{bp}(j\omega_m), \quad (17)$$

where $G_{i,ESC}(j\omega_m)$ is the closed loop current transfer function of ESC. For evaluating (13), $G_{plant}(j\omega_m)$ in (16) is given by

$$G_{plant,v_o}(j\omega_m) = G_{i,ESC}(j\omega_m)Z_{away,ESC}(j\omega_m)G_{bp}(j\omega_m). \quad (18)$$

The dynamics of the perturbation amplitude control loop are also derived by following [20], which treats the small-signal variations in A as amplitude modulation. It can be shown that for the square wave perturbation of Fig. 3 the amplitude loop has the transfer function

$$G_{A,v}(j\omega_m) = \frac{4V_{in}}{\pi} \frac{(A_0 A_l^* + A_0^* A_u)}{\|A_0\|}, \quad (19)$$

where

$$A_0 = G_{plant}(j\omega_m),$$
$$A_l = -\frac{1}{2\omega_m} G_{plant}[j(\omega_{inj} - \omega_m)],$$
$$A_u = \frac{1}{2\omega_m} G_{plant}[j(\omega_{inj} + \omega_m)], \quad (20)$$

and

$$G_{plant}(j\omega_m) = G_{i,ESC}(j\omega_m)Z_{away,ESC}(j\omega_m)G_{bp}(j\omega_m). \quad (21)$$

For the hardware setup described in Section III.A, the frequency response of the f_{inj} loop and amplitude loop models were evaluated with an estimated system crossover frequency, $f_{c,sys}$, of 168 Hz and a perturbation amplitude, A, of 63 mA. The responses are shown in Fig. 6. It is evident from Fig. 6 that the transfer functions exhibit low pass filter characteristics with a dominant pole pair which is highly damped.

C. Design of the Monitor Controllers

Unlike designing the controller for monitoring a converter loop gain [15], our goal is to design the controllers for monitoring the minor loop gain of a dynamic system that has multiple converters and whose impedance changes with operating point. We cannot, therefore, rely on complete models for our design as we are not assuming that Z_{away} is known. Hence, we would like to simplify the small-signal models developed above and derive a measurement-based strategy to design the monitor controllers. From above analysis, both the amplitude loop and the frequency loop exhibit low-pass filter characteristics and a dominant pole with a pole frequency of

$$\omega_1 = \sqrt{\omega_{inj}^2 - 2\omega_{inj}\omega_0\sqrt{1 - \frac{1}{4Q^2}} + \omega_0^2}, \quad (22)$$

where ω_0 is the resonant frequency of the band-pass filter, Q is the quality factor of the band-pass filter and ω_1 is the pole frequency of the dominant pole pair. In the continuous monitor presented here, the band-pass filter resonant frequency is the same as the injection frequency such that $\omega_{inj} = \omega_0$, so the frequency of the dominant pole-pair for the continuous monitor becomes
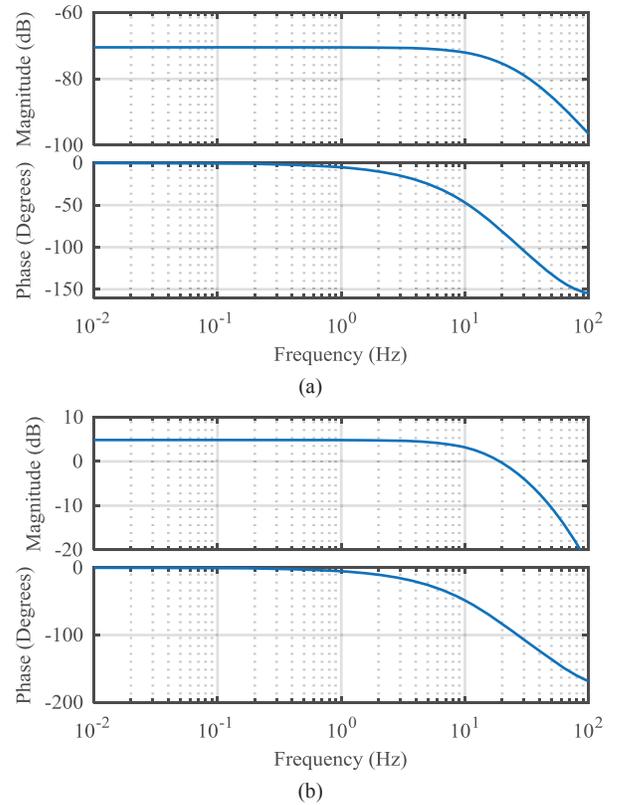

Fig. 6. Frequency response of the envelope models; (a) f_{inj} loop and, (b) amplitude loop.

$$\omega_1 = \sqrt{2}\omega_{inj}\sqrt{1 - \sqrt{1 - \frac{1}{4Q^2}}}. \quad (23)$$

Equation (23) shows that the dominant pole frequency is linearly dependent on f_{inj} and that it reduces with increasing Q. While a high Q is desired to extract the single frequency component at f_{inj}, a very high Q cannot be used as it would place ω_1 at a low frequency, reducing the achievable bandwidth for the monitor controllers. In this work, a Q of 5 was used. According to [20], the dc gain of the f_{inj} loop is proportional to the slope of G_{plant} in (16) and is given by

$$G_{f_{inj},0} = \frac{4A}{\pi}\left.\frac{\left(\delta\|G_{plant}(j\omega)\|\right)}{\delta\omega}\right|_{\omega=\omega_{inj}}, \quad (24)$$

where

$$G_{plant}(j\omega) = G_{plant,v_s}(j\omega) - G_{plant,v_o}(j\omega). \quad (25)$$

The dc gain of the f_{inj} loop can thus be estimated by measuring $v_{env,err}$ in (6) at two frequencies around an estimated $f_{c,sys}$ and finding the slope. Furthermore, the initial value of A, the amplitude of square perturbation, can be set as

Fig. 7. (a) Bode plot of ZESC and Zaway,ESC and, (b) Nyquist plots of system minor loop gain for load converter powers from 0 W to 30 W.

$$A = \frac{\pi}{4}\frac{A_{ref}}{\|Z_{away}(j\omega_{c,sys})\|}, \quad (26)$$

where A_{ref} is the desired amplitude of voltage perturbation and $\|Z_{away}(j\omega_{c,sys})\|$ can be estimated from measurement. Similarly, the dc gain of the amplitude loop is given by [20] as

$$G_{A,0} = \frac{4}{\pi}\|G_{plant,vo}(j\omega_{c,sys})\|, \quad (27)$$

where $\|G_{plant,vo}(j\omega_{c,sys})\|$ can be estimated by measuring $\|v_o\|/\|i_{ref}\|$ at the estimated $f_{c,sys}$. With these simplifications, and observing from Fig. 6 the dominant pole characteristics, the f_{inj} integrator can be designed as

$$k_{i,f_{inj}} = \frac{2\pi f_{c,f}}{G_{f_{inj},0}}, \quad (28)$$

where $f_{c,f}$ is the desired crossover frequency of the f_{inj} loop and $k_{i,finj}$ is the integrator gain. Similarly, the amplitude controller can be designed as

$$k_{i,A} = \frac{2\pi f_{c,A}}{G_{A,0}}, \quad (29)$$

where $f_{c,A}$ is the desired crossover frequency of the amplitude loop and $k_{i,A}$ is the integrator gain. For both controllers, the crossover frequency is placed much lower than the pole frequency given by (23). Once these controllers are designed in continuous time, a suitable method can be used to convert it to discrete time before implementing in a microcontroller or FPGA.

V. Experimental Results

The hardware tests presented in this section aim to establish the practicality and applicability of the proposed stability margin monitor in a wide variety of systems by initializing the continuous monitor using only online measurements and the simplified models presented in Section III. Furthermore, tests are performed to evaluate the performance of the continuous monitor with system operating points changing. This is done by varying the load converter power from 0 W to 30 W and monitoring the change in system minor loop gain crossover frequency and phase margin.

A. Analysis of Test Cases

As mentioned in Section IV, the current and voltage controllers of the converters in the test setup are designed such that the system crossover frequency, $f_{c,sys}$, given by (7) and the system phase margin, PM_{sys}, given by (8) changes significantly as the load power increases. To have a baseline for comparison, the analytical models of Z_{ESC} and $Z_{away,ESC}$ are computed, where the impedance models of Z_{sc} and Z_{Load} are given in [14]. The frequency response of Z_{ESC} and $Z_{away,ESC}$, and the Nyquist plot of the minor loop gain (4) are shown in Fig. 7. It is evident from the bode plots in Fig. 7(a) that, as the load converter increases its power it changes the impedance seen by the ESC, resulting in a change of $f_{c,sys}$. Similarly, it can be seen from both the bode
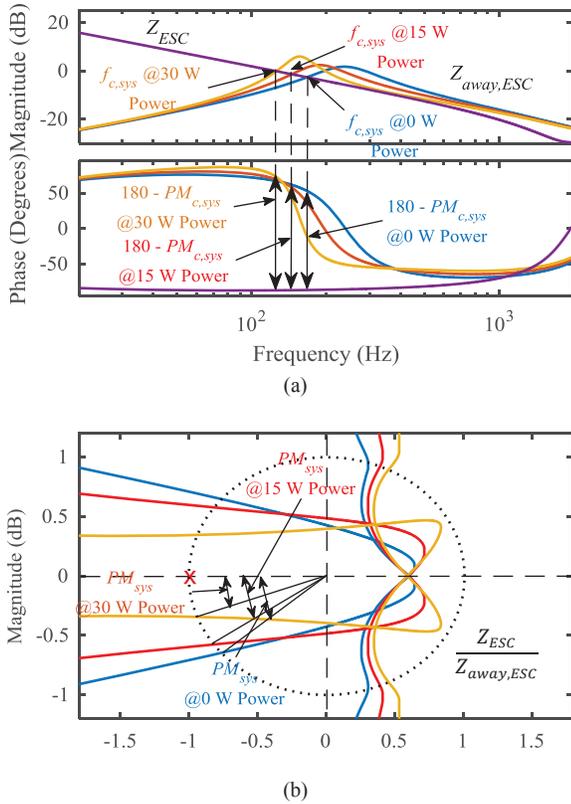
and Nyquist plots in Fig. 7(b) that the phase margin PM_{sys} reduces as the load power increases.

B. Initialization of the Continuous Monitor

A dc microgrid such as that shown in Fig. 1 is expected to be dynamic with sources and loads coming on and going off during normal operation of the system. This implies that, for the continuous monitor, Z_{away} cannot be known a priori. However, the operation and controller design of the stability margin monitor depend on Z_{away}. Hence a measurement-based initialization of the continuous monitor is proposed in this paper based on the model simplification presented in Section IV.

To better explain the initialization steps, the experimental results of the continuous monitor initialization for the hardware setup of Fig. 5 is shown in Fig. 8 where, from the top, the first trace (cyan) shows the dc bus voltage, the second trace (pink) shows the current that the ESC draws from the bus, the third trace (green) shows the identified system crossover frequency $f_{c,sys}$ and the last trace (blue) shows the identified system phase margin PM_{sys}. The initialization steps shown in Fig. 8 are as follows.

1) Time t_1: At time t_1, the source converter starts up, ramps up the dc link voltage and starts regulating it in closed loop.

2) Time t_2: At time t_2, the ESC starts up, enables closed loop regulation of the output current control and ramps up the current drawn from the dc link to 4 A.

3) Time t_3: At time t_3, the continuous monitor enables the injection of square wave perturbation. The frequency of injection, f_{inj}, is set to be the initial estimate of $f_{c,sys}$ (180 Hz) which can be estimated from a one-time frequency sweep or a wide-band injection. The amplitude of perturbation is ramped up from zero to an initial value computed from (26).

4) Time t_4: At time t_4, the dc gain of the amplitude loop is estimated from (27) by setting

$$\left\| G_{plant,vo}(j\omega_{inj}) \right\| = \frac{v_{ofp}}{A}, \tag{30}$$

where A is the value of the initial amplitude of injection. Then the integrator gain for the perturbation amplitude controller is computed using (29) and the integrator is enabled. From t_4 onwards, the perturbation amplitude is regulated to be 150 mV which is 3% of the rated dc bus voltage of 5 V.
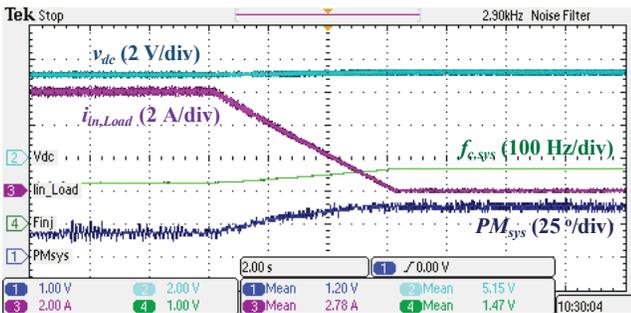

Fig. 9. Dc bus voltage (cyan), load converter input current (pink), system crossover frequency (green) and system phase margin (blue) during load transient.
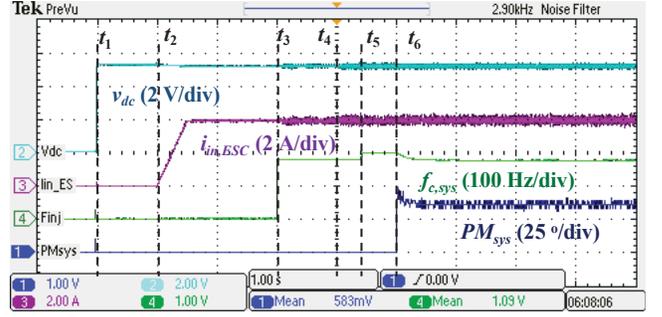
Fig. 8. Dc bus voltage (cyan), ESC current input from dc bus (pink), system crossover frequency (green) and system phase margin (blue) during initialization of the continuous monitor.

5) Time t_5: At time t_5, the envelope error, $v_{env,err}$, is recorded for an f_{inj} of 180 Hz and then f_{inj} is ramped up to 200 Hz.

6) Time t_6: At time t_6, the envelope error, $v_{env,err}$, is recorded for f_{inj} of 200 Hz. This value and the value at t_5 are used in (24) to compute the dc gain of the f_{inj} loop and then the f_{inj} integrator gain is computed using (28). Finally, the f_{inj} integrator and PM_{sys} computation are enabled, after which, the ESC monitors $f_{c,sys}$ and PM_{sys} continuously.

C. Performance of the Continuous Monitor

Once the continuous monitor has been initialized, the load converter power is ramped up to 30 W, at which point PM_{sys} is low (~20°). Then, the load power is ramped down to 0 W at a rate of 5 W/s. The response of the system and the monitor outputs ($f_{c,sys}$ and PM_{sys}) for this transient are shown in Fig. 9 where, from the top, the first trace (cyan) shows the dc bus voltage, the second trace (pink) shows the load converter input current, the third trace (green) shows the identified system crossover frequency $f_{c,sys}$ and the last trace (blue) shows the identified system phase margin PM_{sys}.

From the v_{dc} trace in Fig. 9, it is evident that the amplitude of perturbation is regulated before, during and after the load transient. As the load power reduced from 30 W to 0 W, the identified $f_{c,sys}$ changed from 124 Hz to 168 Hz and the identified PM_{sys} changed from 18° to 37°. To compare the performance of

Fig. 10. Comparison of the experimental performance of the continuous monitor with theoretical analysis results.

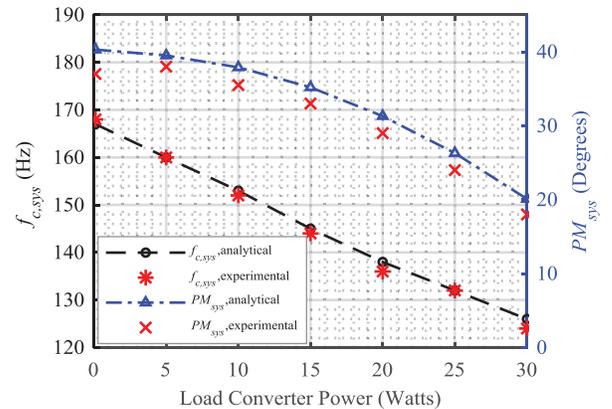the monitor with the analytical models, the identified $f_{c,sys}$ and PM_{sys} were recorded for load powers from 0 W to 30 W and plotted against theoretical values found using the Nyquist plots of Fig. 7(b). The comparison is shown in Fig. 10, where the left y-axis shows frequency in Hz and the right y-axis shows the phase margin in degrees. Fig. 10 shows that the continuous monitor was able to identify $f_{c,sys}$ and PM_{sys} with reasonable accuracy.

VI. CONCLUSIONS

A novel method to monitor the system stability margin of a dc microgrid online in a continuous fashion has been proposed in this paper. The continuous monitoring technique can be embedded into any one of the converters already present in the system to evaluate the system stability margin without much additional computational cost. The proposed small-signal analysis of the continuous monitor and simplification method allow the online measurement-based design and tuning of the monitor controllers, with an estimated system crossover frequency to start. To validate the proposed analysis and design, hardware results are provided for the auto-initialization and operation of the proposed continuous monitor and compared with the theoretical prediction over a range of operating conditions. The continuous monitor proposed in this paper is applicable to other systems with multiple sources, loads and bidirectional converters connected. The monitored system crossover frequency and phase margin can be used in active stabilization, active damping and system central controller for system stabilization.

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CHAPTER 4

High Frequency Link Isolated Multi-Port Converter for Active Cell Balancing Applications

High Frequency Link Isolated Multi-Port Converter for Active Cell Balancing Applications

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Abstract—This paper proposes an isolated multi-port converter based on high-frequency AC link to combine the multiple modular cell-level active balancing converters into a multi-port converter. The topology uses integrated magnetics and just one central secondary bridge, which reduces significantly the number of switching devices and passive components required for the implementation of the battery management system. Additional advantages include use of the same ground reference for all the cells, eliminating the need for isolated communications between active balancing converters. Steady-state analysis for the topology is given. A simple control scheme is proposed for the differential currents required for active cell balancing. Closed-loop simulation results are provided for a three-cell system that validates the proposed control scheme for the topology. A 100 W 4-port prototype converter is developed and experimental results are given to prove the feasibility of the proposed high-frequency link coupled multi-port converter.

Index Terms—Active balancing, resonant converter, high-frequency link, isolated DC/DC, high power density, integrated magnetics

I. Introduction

Modular active balancing systems offer simplicity, high efficiency, and faster balancing speeds by integrating cell balancing and power processing functions onto a cell-level dc/dc converter [1]–[5]. Unlike the simple passive balancing system, the modular active balancing system requires a DC/DC converter for each battery cell which results in a large number of power converters and high component count for a large battery pack. To reduce cost, various topologies and methods specific to cell balancing applications have been proposed in literature [6]–[10]. Three-port converters for cell-balancing are reported in [6], [7] to reduce the cost by balancing two cells per converter. Time-sharing of the balancing converter [9], or some components of the converter [10], are reported in the literature. This time-sharing method is cost-effective but does not provide continuous cell balancing.

In many battery applications, a high-frequency (HF) transformer based isolated DC/DC converter is used to process the power before connecting to the load. The HF transformer serves the purpose of providing galvanic isolation [11], [12] or voltage matching [13], [14]. Existing magnetically coupled isolated topologies [15], [16] are usually limited to three ports,

extending these approaches to larger number of ports creates control complexities and hardware challenges with transformer fabrication. In [17], [18], a single multi-winding transformer is used to magnetically couple multiple ports. This approach would require long cables to connect all the cell ports to the common magnetics when used for large battery packs.

In a battery pack, all the cells are similar with small tolerance in ($\approx 10\%$) in their parameters. The active balancing converter needs to be designed to manage only a small ($\approx 10\%$ of rated current) fraction of current mismatch between cells. Taking advantage of this small current mismatch requirement, an isolated multi-port topology is proposed that has multiple symmetrical input ports and one common secondary winding and secondary bridge that is shared among all the inputs. The common secondary winding spans over all the cell ports picking up power and acts as an AC busbar. This greatly reduces the size and cost of the converter due to the reduced component count. All the input ports are connected to a common output through a high-frequency (HF) link. The topology has no limitation on the number of ports it can have. The number of ports might only be limited by the computational and peripheral capabilities of the implemented control platform.

This paper focuses on introducing and validating the topology. Also, a closed-loop control scheme is proposed to simultaneously achieve output regulation and continuous cell balancing. The proposed control scheme is simple and scalable in order to handle active balancing for a large number of cells.

II. High Frequency Link Multiport converter

In battery management applications, different cell currents are to be drawn to achieve active cell balancing. Based on the mismatch in the cell capacity, the worse-case difference required can be up to 10 % to 20 % of the average cell currents. Identifying that the differential power is only a small fraction of the total battery power a new topology is proposed. A multi-port topology based on the series connection of high-frequency (HF) link is shown in Fig. 1. This approach is particularly beneficial for cell-balancing applications since multiple ports are in physical close proximity allowing for the HF link connection. And also, the particular way of connecting the transformer creates a unique advantage that all the primary
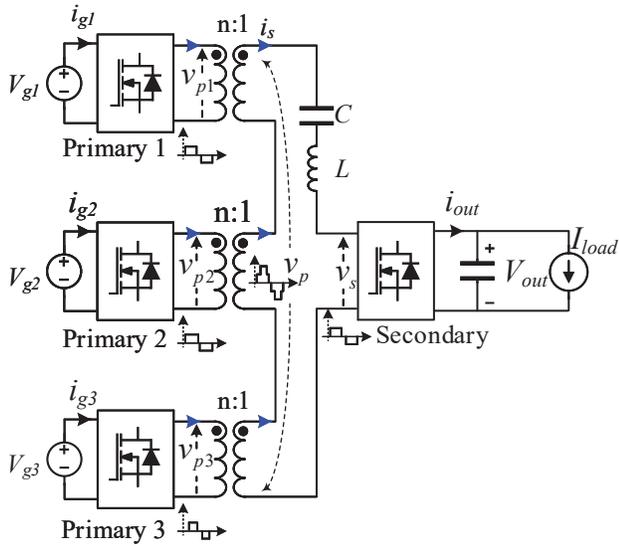
Fig. 1: Schematic of the proposed multiport converter shown with 3 cell ports

(a) Top cross-section view (b) Front cross-section view

Fig. 2: Transformers realization with commercial planar E core structures

windings are decoupled. This allows the control to be relatively simpler while having a large number of ports.

A. Topology description

Each port has a bridge that generates high-frequency quasi-square voltage and each bridge has a transformer with secondary windings such that all the primary bridge voltages effectively add up to drive the resonant tank. This can be done by either having all the secondaries connected in series or equivalently by having a magnetic structure that sums up the magnetic field generated by each primary bridge. One such way is to use a single secondary winding that goes through all the magnetic cores. In the schematic shown in Fig.1, three cell ports and one output port are shown. The HF link uses a resonant LC tank as the energy transferring element. Other isolated bi-directional topologies based on the convention 2-port topologies can be used as well. For example, the non-resonant dual active bridge. Advantages of the proposed topology and magnetics approach are **1) Reduced component count:** Since only one secondary bridge is used, the number of bridges are reduced to $m + 1$. Here, m is the number of primary ports. A traditional two-port converter per cell would have $2m$ bridges. **2) Efficient Magnetics:** Since all these converters are physically close, the secondary winding can be wound continuously through all the cores reducing the winding length compared to using an individual DC-DC converter per cell. The secondary winding doubles as a busbar connecting all the input ports power to the central output port. **3) Elimination of contact resistance:** Output termination requirement and contact resistance for each individual DC/DC output are eliminated. If a single DC/DC converter were to be used per cell then each of those outputs needs to be connected to the common bus bar and each secondary winding of the transformer would have termination losses at the secondary bridges. But here, the secondary-side of the transformer acts
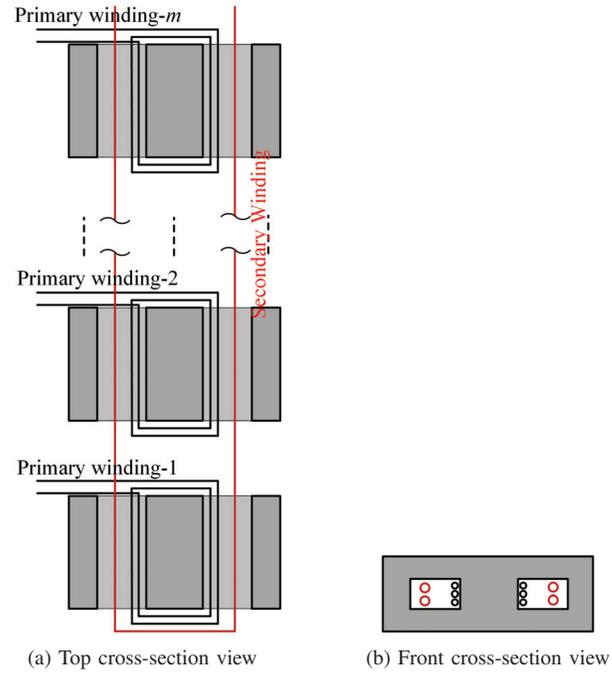
as the bus bar collecting the current. Hence, serves the dual purpose of isolation and bus. **4) Common ground reference:** All the cells can be referred to the same ground potential, eliminating the need for isolation for communications and control signals between different modules.

B. High Frequency Magnetics

There are many ways to realize the isolated high-frequency link. Individual transformers can be built, each with it's own primary and secondary, or all the primaries can have one common secondary winding as shown in Fig. 2. If individual secondaries are used, then they have to be connected in series. Since the cells in a battery are usually packed together is close physical proximity, it is beneficial to have a common secondary winding that is wound through all the transformer cores. This will avoid the need to make connections between adjacent terminals. The effective mean length per turn of the secondary winding using this approach will be lower if the distance between adjacent cores is kept lower than the width of the cores. Hence, this leads to lower resistance than the cumulative individual transformers winding resistance.

C. Sinusoidal Analysis

The operation of the proposed high-frequency (HF) link based series resonant topology is explained in this section. Analysis is first given for the 3-input port topology shown in Fig. 1 and then is extended for a more generalized m-port topology.

V_{g1}, V_{g2}, V_{g3} are the dc-link voltages at the primary bridges, and V_{out} is the dc-link voltage at the output bridge. The primary bridges and secondary bridge generate quasi-square wave voltages v_{p1}, v_{p2}, v_{p3}, v_s respectively. The definitions
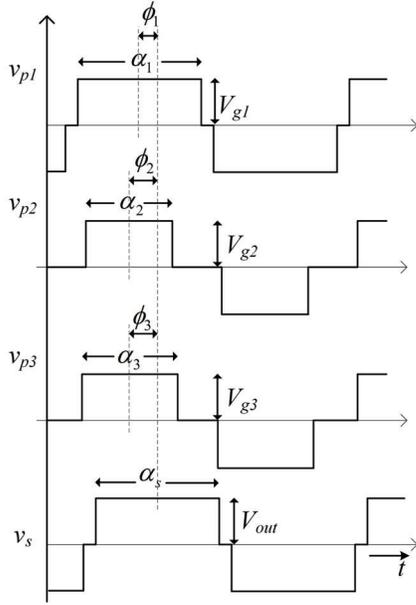
Fig. 3: Phase-shift and duty-cycle definitions for bridge voltages

for phase-shift (ϕ_k) and duty cycle (α_k) of these voltages are given in Fig. 3. The equivalent circuit based on fundamental approximation is shown in Fig. 4a. The fundamental phasor diagram of this equivalent circuit is given in Fig. 4b. The transformer secondaries are connected such that the sum of the instantaneous voltages drive the resonant tank. The equivalent circuit and phasor diagram also clearly conveys this idea. For the analysis, only the fundamental component of the bridge voltages are used. This simplifies the analysis and gives reasonable accuracy. The secondary bridge voltage is used as reference for the phasor analysis. For the following analysis, the turns ratio is assumed to be unity so as to simplify the equations. I is the amplitude and θ_k is the angle of tank current i_s from k^{th} bridge voltage. The fundamental phasor voltages in polar and rectangular co-ordinates are given as

$$
\begin{aligned}
\vec{v}_{p1} &= \frac{4}{\pi} V_{g1} \sin(\frac{\alpha_1}{2}) \angle \phi_1 \\
&= \frac{4}{\pi} V_{g1} \sin(\frac{\alpha_1}{2})(\cos(\phi_1) + j\sin(\phi_1)), \\
\vec{v}_{p2} &= \frac{4}{\pi} V_{g2} \sin(\frac{\alpha_2}{2}) \angle \phi_2 \\
&= \frac{4}{\pi} V_{g2} \sin(\frac{\alpha_2}{2})(\cos(\phi_2) + j\sin(\phi_2)), \\
\vec{v}_{p3} &= \frac{4}{\pi} V_{g3} \sin(\frac{\alpha_3}{2}) \angle \phi_3 \\
&= \frac{4}{\pi} V_{g3} \sin(\frac{\alpha_3}{2})(\cos(\phi_3) + j\sin(\phi_3)), \\
\vec{v}_{s} &= \frac{4}{\pi} V_{\text{out}} \sin(\frac{\alpha_s}{2}) \angle 0 \\
&= \frac{4}{\pi} V_{\text{out}} \sin(\frac{\alpha_s}{2}).
\end{aligned}
\tag{1}
$$

Effective primary voltage,

$$
\vec{v}_p = \vec{v}_{p1} + \vec{v}_{p2} + \vec{v}_{p3}.
\tag{2}
$$

Effective tank current,

$$
\vec{i}_s = \frac{\vec{v}_p - \vec{v}_s}{jX_s},
\tag{3}
$$

where, $X_s = \omega_s L - \frac{1}{\omega_s C}$ is the impedance of the resonant tank. Port powers P_1, P_2, P_3, P_{out} and port average currents $\langle i_{g1} \rangle$, $\langle i_{g2} \rangle$, $\langle i_{g2} \rangle$, $\langle i_{\text{out}} \rangle$ are given by

$$
\begin{aligned}
P_1 = \frac{8V_{g1}\sin(\frac{\alpha_1}{2})}{\pi^2 X_s} [&V_{\text{out}} \sin \frac{\alpha_s}{2} \sin \phi_1 \\
&+ V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2 - \phi_1) + V_{g3} \sin \frac{\alpha_3}{2} \sin(\phi_3 - \phi_1)],
\end{aligned}
$$

$$
\begin{aligned}
P_2 = \frac{8V_{g2}\sin(\frac{\alpha_2}{2})}{\pi^2 X_s} [&V_{\text{out}} \sin \frac{\alpha_s}{2} \sin \phi_2 \\
&+ V_{g1} \sin \frac{\alpha_1}{2} \sin(\phi_1 - \phi_2) + V_{g3} \sin \frac{\alpha_3}{2} \sin(\phi_3 - \phi_2)],
\end{aligned}
$$

$$
\begin{aligned}
P_3 = \frac{8V_{g3}\sin(\frac{\alpha_3}{2})}{\pi^2 X_s} [&V_{\text{out}} \sin \frac{\alpha_s}{2} \sin \phi_3 \\
&+ V_{g1} \sin \frac{\alpha_1}{2} \sin(\phi_1 - \phi_3) + V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2 - \phi_3)],
\end{aligned}
$$

$$
\begin{aligned}
P_{\text{out}} = \frac{8V_{\text{out}}\sin(\frac{\alpha_3}{2})}{\pi^2 X_s} [&V_{g1} \sin \frac{\alpha_1}{2} \sin \phi_1 \\
&+ V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2) + V_{g3} \sin \frac{\alpha_3}{2} \sin(\phi_3)].
\end{aligned}
\tag{4}
$$

$$
\begin{aligned}
\langle i_{g1} \rangle = \frac{8\sin(\frac{\alpha_1}{2})}{\pi^2 X_s} [&V_{\text{out}} \sin \frac{\alpha_s}{2} \sin \phi_1 \\
&+ V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2 - \phi_1) + V_{g3} \sin \frac{\alpha_3}{2} \sin(\phi_3 - \phi_1)],
\end{aligned}
$$

$$
\begin{aligned}
\langle i_{g2} \rangle = \frac{8\sin(\frac{\alpha_2}{2})}{\pi^2 X_s} [&V_{\text{out}} \sin \frac{\alpha_s}{2} \sin \phi_2 \\
&+ V_{g1} \sin \frac{\alpha_1}{2} \sin(\phi_1 - \phi_2) + V_{g3} \sin \frac{\alpha_3}{2} \sin(\phi_3 - \phi_2)],
\end{aligned}
$$

$$
\begin{aligned}
\langle i_{g3} \rangle = \frac{8\sin(\frac{\alpha_3}{2})}{\pi^2 X_s} [&V_{\text{out}} \sin \frac{\alpha_s}{2} \sin \phi_3 \\
&+ V_{g1} \sin \frac{\alpha_1}{2} \sin(\phi_1 - \phi_3) + V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2 - \phi_3)],
\end{aligned}
$$

$$
\begin{aligned}
\langle i_{\text{out}} \rangle = \frac{8\sin(\frac{\alpha_3}{2})}{\pi^2 X_s} [&V_{g1} \sin \frac{\alpha_1}{2} \sin \phi_1 \\
&+ V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2) + V_{g3} \sin \frac{\alpha_3}{2} \sin(\phi_3)].
\end{aligned}
\tag{5}
$$

The analyses can be extended to m input ports. $\vec{v}_{p,k}$ is the phasor for the fundamental component of the primary bridge-$'k'$. The secondary bridge voltage $\vec{v}_s$ is used as reference for the phasor analysis. The duty cycle α_k and phase shift ϕ_k of
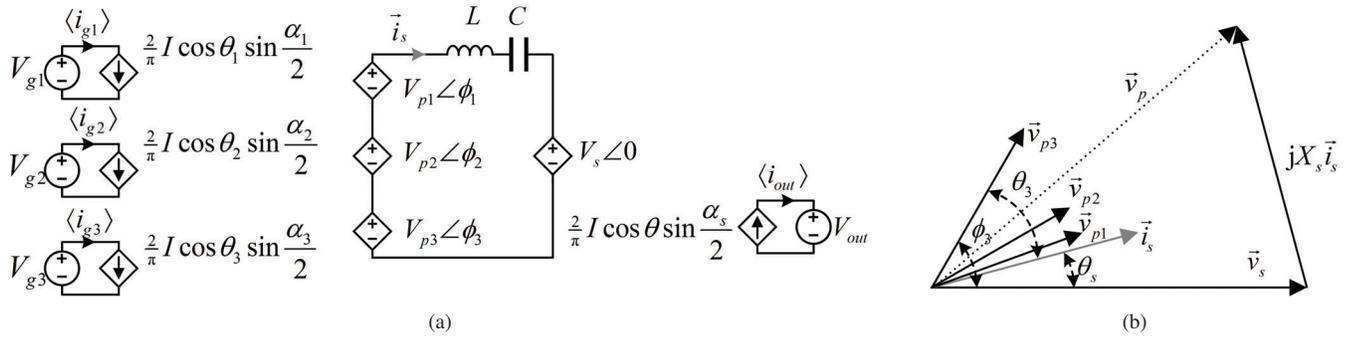
Fig. 4: (a) Equivalent circuit based on fundamental approximation, and (b) Fundamental phasor diagram of the proposed multi-port converter
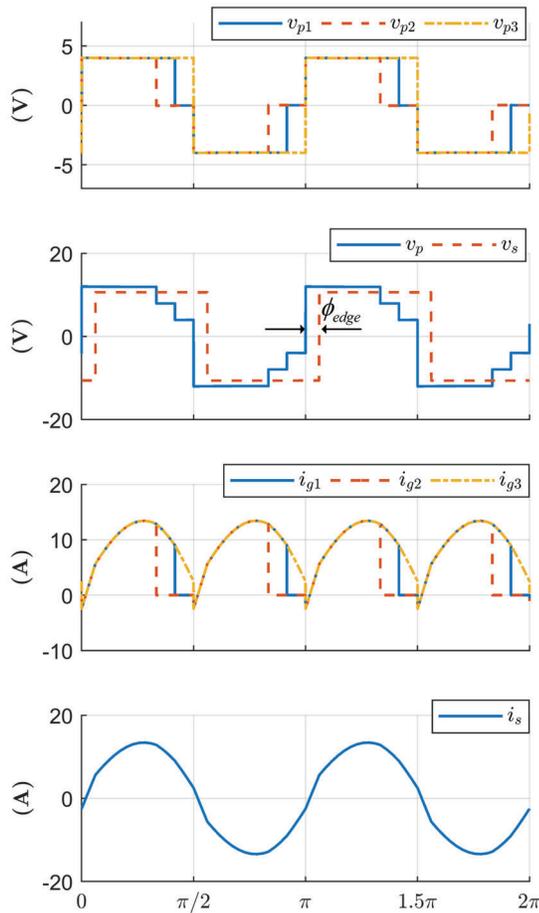

Fig. 5: Simulation waveforms for 3-cell converter for an operating point $V_{g1} = V_{g1} = V_{g1} = 4$ V, $V_{out} = 11V$ ($\alpha_1 = 0.83\pi$, $\alpha_2 = 0.67\pi$, $\alpha_3 = \alpha_s = \pi$, and $\phi_{edge} = 0.12\pi$). It is clear from waveforms that $\langle i_{g3}\rangle$= 9.12 A > $\langle i_{g1}\rangle$= 8.15 A> $\langle i_{g2}\rangle$= 6.31 A for $\alpha_3 > \alpha_1 > \alpha_2$.

these voltages with respect to secondary are used as control variables. The primary bridge voltage phasors are given as

$$\vec{v}_{p,k} = V_{p,k}(cos\phi_k + jsin\phi_k), \qquad (6)$$

where, $V_{p,k} = \frac{4}{\pi}sin(\frac{\alpha_k}{2})$, is the amplitude of the fundamental phasor of kth bridge voltage.

Effective primary voltage is $\vec{v}_p = \sum_{k=1}^m \vec{v}_{p,k}$, where, m is the total number of input ports.

Input average current for k^{th} port, output power and output bus current for unity turns ratio are given by

$$I_{g,k} = \frac{1}{2X_s}[V_s sin\phi_k + V_{p1}sin(\phi_1 - \phi_k) + V_{p2}sin(\phi_2 - \phi_k)$$
$$+ ... + V_{gm}sin(\phi_m - \phi_k)],$$

$$P_{out} = \frac{V_{out}}{2X_s}[V_{p1}sin\phi_1 + V_{p2}sin\phi_2 + ... + V_{pm}sin\phi_m],$$

$$I_{out} = \frac{1}{2X_s}[V_{p1}sin\phi_1 + V_{p2}sin\phi_2 + ... + V_{pm}sin\phi_m]. \qquad (7)$$

III. CONTROL APPROACH AND SIMULATION RESULTS

Bridge-k has two control parameters duty cycle α_k and phase-shift ϕ_k. The power delivered to the secondary depends on the values of duty cycle and phase-shift of all the bridges. This is clearly seen in the steady-state equations (7). The topology offers many degrees of control freedom. In the proposed control scheme, the duty cycle (α_s) of the secondary bridge is always kept at π and is not used as a control parameter. All the primary bridge voltages are active transition aligned. A new control variable ϕ_{edge}, defined as the angle between the rising edge of the primary voltages and rising edge of secondary voltage, is used as control variable to regulate the output. The duty cycles (α_1, α_2, .. α_m) are used achieve cell balancing task.

Figure 5 provides insight and intuition for the control approach taken to introduce a difference in the input port currents. Each primary bridge voltage has a different duty cycle but all the bridge voltages' rising edge are aligned. By aligning the switching of the lagging legs, devices in all the primary bridges can zero voltage swtiched (ZVS). From the port current waveforms i_{g1}, i_{g2}, i_{g3}, it can be seen that the average port current will be relatively low for the bridge with lower duty cycle. Hence, by controlling the relative duty cycles, the relative loading between the cells can be regulated. For the operating condition $\alpha_3 > \alpha_1 > \alpha_2$ given in Fig. 5 the average currents will also be in the order $\langle i_{g3}\rangle > \langle i_{g1}\rangle > \langle i_{g2}\rangle$. This monotonic relation between duty cycle to the relative current sharing allows design of closed loop control using simple linear controls.

The block diagram of the control scheme for 3-cell system is given in Fig. 6. To implement the relative sharing, a weight is given to each port current. The port that must have the highest input current sharing is used as the base (i_{base}) for determining the weights based on the relative sharing required. The base port and weights (w_k^{ref}) for each port current are commanded by the battery management algorithm. These values are dynamically changed over time by the BMS to acheive the balancing task. The primary base port with the highest current is weighted as '1' and its primary voltage will have a full duty of π. And all the other port references are weighted relative to this highest port and will have weights less than or equal to '1'. For example, if cell-3 must have the highest current, $\langle i_{g3} \rangle$ is used as the base and α_3 is set as π.

TABLE I: TABSRC prototype parameters

Parameter	Description
Rated Power	100 W
Nominal Input	4 V at each of the three input port
Nominal Output	12 V
Switching Frequency	278 kHz
Resonant tank	L =1.17 µH (includes transformer leakages), C =400 nF
Switching Devices	BSC016N06NS, 60 V, 1.6 mΩ
Transformer	1:1 turns ratio
	Core: ELT25 planar, PC95 material
	Winding: 0.2 mm thick copper foil
Tank Inductor	1 µH
	Core: ELT25 planar, PC95 material
	Winding: 0.2 mm thick copper foil
Tank Capacitor	100 nF, 50 V, ceramic capacitor. 4 in parallel,

The simulations for a three-cell system with parameters listed in Table I were performed in PLECS software. The bandwidth of the output loop is designed to be approximately 1 kHz and the cell balancing loops to be 100 Hz. The simulation results of the closed-loop control implementation are given in Fig. 7. The output current is regulated to 8 A during the entire simulation. Till 2.5 ms, all the port currents are maintained equal by setting the reference weights $w_1^{ref} = w_2^{ref} = 1$ and from 2.5 ms the i_{g1} is commanded to be regulated to 80% of i_{g3} and i_{g2} 90% of i_{g3}. To achieve this, at t = 2.5 ms, the reference weights w_1^{ref} and w_2^{ref} are step changed from 1 to 0.8 and 0.9 respectively. Here, i_{g3} is regulated to have the highest current sharing. Hence, α_3 stays at π while the other two duty cycles (α_1, α_2) reduce to create the difference in currents. The simulation results validate the control approach proposed to regulate output and perform cell balancing, simultaneously.

IV. HARDWARE PROTOTYPE

A 100 W prototype (see Fig. 8) is designed to operate with three cells. The component parameters are given in Table I. All the three primary H-bridges are symmetrical and each primary

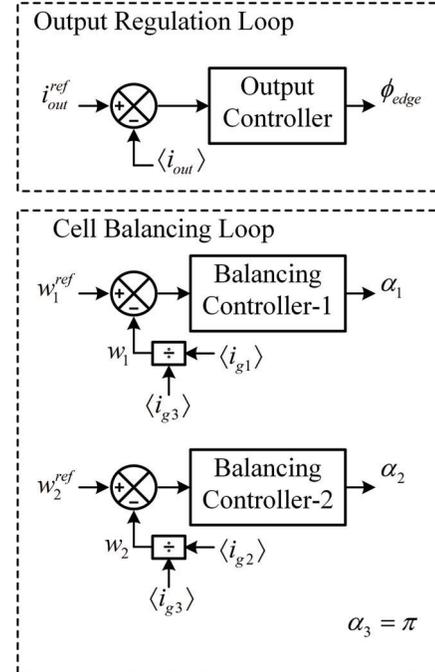Fig. 6: Control scheme block diagram of a three cell system with cell-3 required to have the highest current and hence port-3 input current ($\langle i_{g3} \rangle$) is used as the base to calculate the weights w_1 and w_2 in the feedback loops.
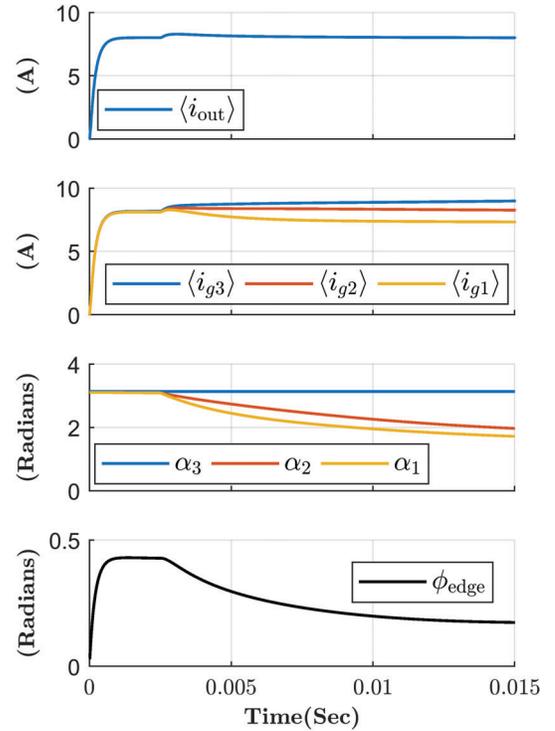

Fig. 7: Closed-loop simulation waveforms for i_{out}^{ref} = 8 A and step change in w_1^{ref}, w_2^{ref} from 1 to 0.8 and 1 to 0.9 respectively at t=2.5 ms.
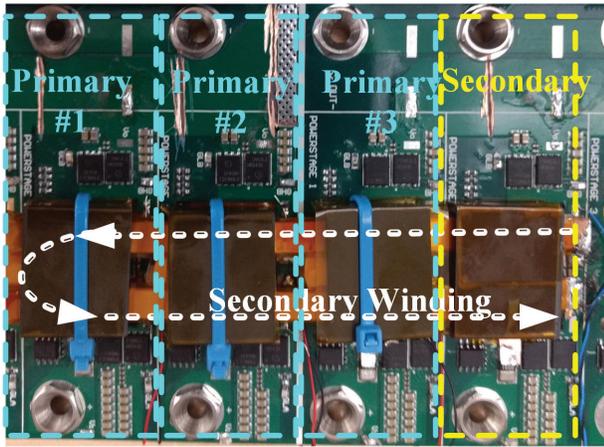
Fig. 8: Four-port prototype with parameters of Table I built for evaluation of the topology.
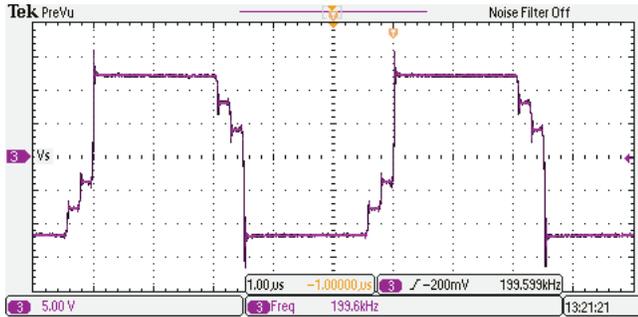

Fig. 9: Effective primary voltage measured on open-circuited secondary winding with the proposed HF link. The rising edge of the voltages are aligned.

board has a transformer. The series resonant capacitance (400 nF) and inductance (1 µH) are on the secondary bridge.

Figure 8 shows the prototype highlighting the common secondary winding. Magnetic coupling as shown in Fig. 2 forms the HF link between the primaries and the secondary winding with unity turns ratio. Figure 9 shows the open circuit secondary winding voltage. For this result, the secondary winding is not soldered on to secondary bridge. The measured secondary voltage is equivalent to resultant primary voltage since the turns ratio is 1:1. The input voltage across each primary bridge was 4 V, resulting in a peak primary voltage of 12 V. The secondary winding voltage appears as a staircase because the bridges are operated at different duty cycles with their rising edges aligned.

The open loop test results are given in Fig. 10 to Fig. 13 For the results in Fig. 10 and Fig. 11, all the primary duty cycles are kept equal to π , and the $\phi_{edge} = 0.12\pi$. From the waveforms, it can seen that all there primary input average currents are equal. The output power is 71 W. In Fig. 12 and Fig. 13, results with different duty cycles for each primary are given. The operating condition is similar to the simulation result given in Fig. 5, that is, $\alpha_1 = 0.83\pi$, $\alpha_2 = 0.67\pi$, $\alpha_3 = \alpha_s = \pi$, and $\phi_{edge} = 0.12\pi$. As expected the input currents are different and have magnitudes close to simulation. This validates the approach of using duty cycle to introduce difference in cell currents.
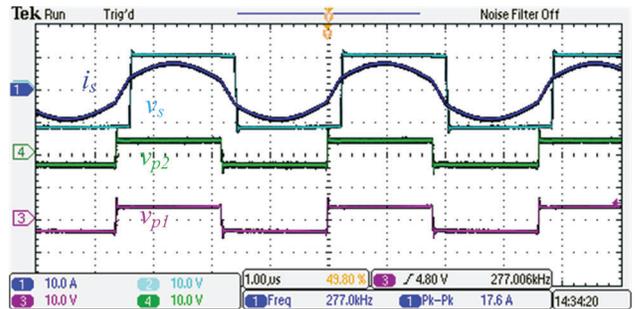
Fig. 10: High-frequency link waveforms for operating point $V_{g1} = V_{g1} = V_{g1} = 4\ V$, $V_{out} = 11\ V$ ($\alpha_1 = \alpha_2 = \alpha_3 = \alpha_s = \pi$, and $\phi_{edge} = 0.12\pi$). Ch1: Secondary winding current (i_s), Ch-2: Secondary bridge voltage (v_s), Ch-3: Primary bridge-1 voltage (v_{p1}), Ch-4: Primary bridge-2 voltage (v_{p2}).

Fig. 11: Input and output DC port currents operating point $V_{g1} = V_{g2} = V_{g3} = 4\ V$, $V_{out} = 11\ V$ ($\alpha_1 = \alpha_2 = \alpha_3 = \alpha_s = \pi$, and $\phi_{edge} = 0.12\pi$). Ch1: Port-1 current ($\langle i_{g1} \rangle$), Ch-2: Port-2 current ($\langle i_{g2} \rangle$), Ch-3: Port-3 current ($\langle i_{g3} \rangle$), Ch-4: Output port current ($\langle i_{out} \rangle$).
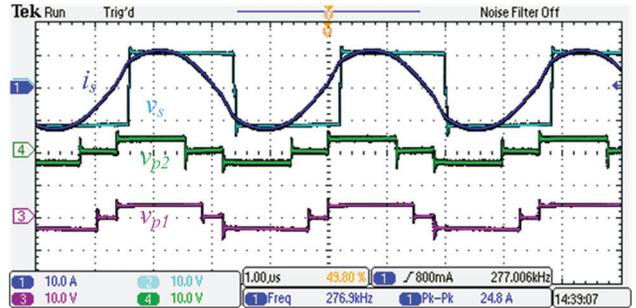
Fig. 12: High-frequency link waveforms for operating point $V_{g1} = V_{g1} = V_{g1} = 4\ V, V_{out} = 11V$ ($\alpha_1 = 0.83\pi$, $\alpha_2 = 0.67\pi$, $\alpha_3 = \alpha_s = \pi$, and $\phi_{edge} = 0.12\pi$). Ch1: Secondary winding current (i_s), Ch-2: Secondary bridge voltage (v_s), Ch-3: Primary bridge-1 voltage (v_{p1}), Ch-4: Primary bridge-2 voltage (v_{p2}).

Fig. 13: Input and output DC port currents for operating point $V_{g1} = V_{g1} = V_{g1} = 4\ V, V_{out} = 11V$ ($\alpha_1 = 0.83\pi$, $\alpha_2 = 0.67\pi$, $\alpha_3 = \alpha_s = \pi$, and $\phi_{edge} = 0.12\pi$).Ch1: Port-1 current ($\langle i_{g1} \rangle$), Ch-2: Port-2 current ($\langle i_{g2} \rangle$), Ch-3: Port-3 current ($\langle i_{g3} \rangle$), Ch-4: Output port current ($\langle i_{out} \rangle$).
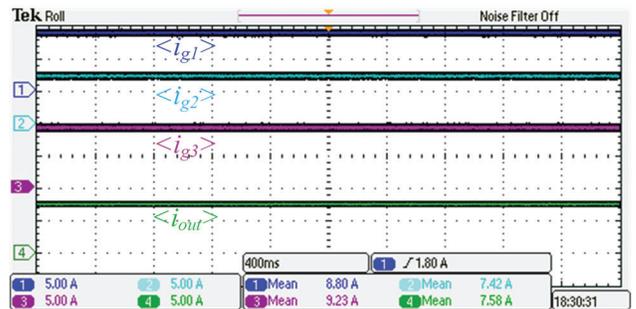
V. Conclusion

A new isolated multi-port topology to implement the active cell balancing with reduced cost is proposed. The proposed high-frequency link based multi-port topology eliminates the need for isolated communication, reduces component count and system cost. Steady-state analysis, simulation results, and hardware results are presented to show the efficacy of the proposed converter. A closed-loop control scheme is proposed that regulates the output and also performs cell balancing. The control scheme proposed for this topology is simple and can be extended to a large number of cells. A 100 W, 4-port prototype is developed and hardware results are presented for validation.

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CHAPTER 5

A Continuous Stability Margin Monitor for DC Microgrid

A Continuous Stability Margin Monitor for DC Microgrids

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Abstract—Emerging dc microgrids incorporating renewable energy and energy storage are presenting new challenges in system design and stability analysis. Several methods have been proposed in literature for online stability evaluation of such dc microgrids using impedance-based analysis. This paper presents a new method for continuous online monitoring of system stability that uses a small, single-frequency perturbation in the system to measure the system impedance minor loop gain cross-over frequency and phase margin. The method can be added as a supplemental function to existing converters in the system so that no additional power hardware is required. The proposed method evaluates stability continuously and can be used as a proactive approach for monitoring and maintaining system stability. System modeling and design of the monitor loop gains is presented. Hardware results are presented to validate the proposed continuous stability monitor, which shows its effectiveness in predicting the system stability margins under varying conditions.

Index Terms—impedance, stability, dc microgrids, monitoring

I. INTRODUCTION

OWING to the continued push towards electrified transportation and integration of renewables, the dc microgrids of the future are expected to be much more dynamic than they have been in the past. Future dc microgrids are expected to incorporate different kinds of sources such as renewable energy, energy storage, and fuel-based generators. They are expected to be re-configurable, have bidirectional converters interfacing energy storage, and may have constant power, intermittent or plug and play loads. Examples of such systems can be found in all-electric aircraft, electric ships and dc fast charging stations [1]–[3] and are expected to be configured as shown in Fig. 1. Stable operation of these microgrids is challenged by the negative incremental resistance behavior of the constant power loads as well as interactions among the controllers of the interconnected converters [4], [5].

Traditional methods of worst case design over all possible scenarios tends to lead to overdesigned systems, including oversized filters and slow controllers [6]. To avoid system overdesign, active stabilizing techniques and adaptive tuning techniques have been proposed. In [7]–[9], the authors used online measurements of system health [7] or frequency response [8], [9] to auto-tune the digital controllers of the converters and improve transient performance and stability. In [10], the authors propose an active stabilizer to add virtual damping in the system based on a measured oscillation frequency at the onset of instability. Application of these

auto-tuning and active damping techniques requires online measurement of system impedances or system health, for which several methods have been proposed.

These methods typically use wideband perturbation followed by a Fourier transform to measure impedances and derive the system stability or tuning parameters from them. In [11], the authors proposed using wideband perturbation to measure ac grid impedance for adaptive control. In [12], the authors used cross-correlation methods to find the input and output impedances of cascaded converters. [13] used an additional converter in a multi-source system to measure the source and load subsystem impedances and applied the Nyquist criterion to find the system stability. In [14], the authors proposed a medium voltage impedance measurement unit to measure the impedance of the source and load subsystem to evaluate stability in a multi-source multi-load system. A common drawback of the existing methods is that they are computationally intensive and, for microgrids with multiple sources and loads, require an additional converter to perform the analysis [13], [14].

This paper presents a novel system stability monitor that can be added to most existing converters in a system as an auxiliary function and that continuously monitors the stability margin of the interconnected system. The stability margin evaluation is enabled by Nodal Stability Analysis, which has been recently proposed as a generalized impedance-based stability analysis method especially suited for dynamic dc microgrids with various interconnected sources, loads and
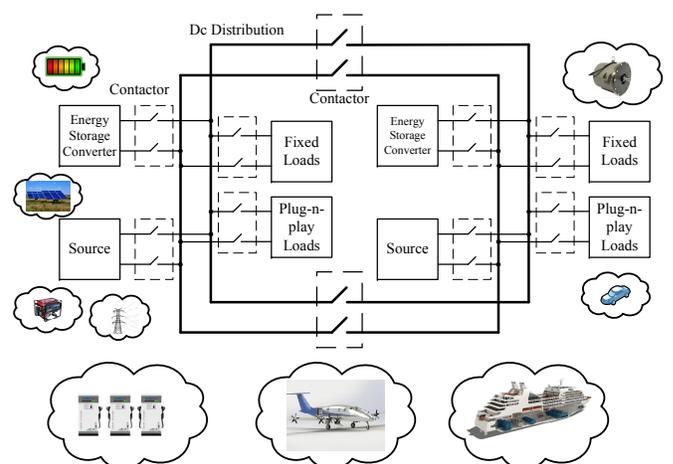

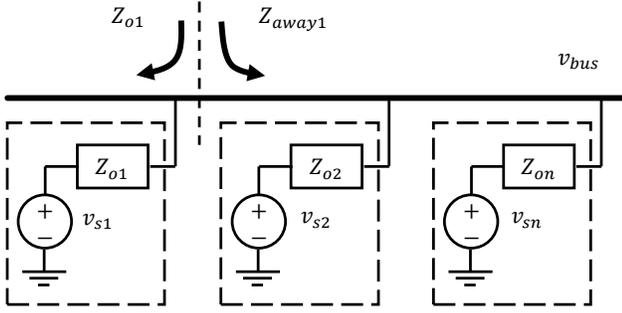Fig. 1. Representative future dc microgrid system [15]–[22].

Fig. 2. A generic dc microgrid showing an arbitrary partitioning of the system and defining the relevant impedances for the nodal stability analysis.

bidirectional converters [23]. The monitor itself is derived from a continuous monitoring method developed previously to monitor the phase margin of the loop gain internal to a power converter [24], [25]. The proposed continuous monitor injects a controlled single-frequency perturbation using one of the converters already in the system, with a small amplitude that does not affect the normal operation. The proposed method can be used in any interconnected system for proactively monitoring and maintaining the system stability, and, unlike existing monitoring methods, the continuous nature of the proposed method would enable development of new techniques in adaptive stability enhancement of dc microgrids.

The paper is organized as follows: Section II summarizes the nodal stability analysis method that enables the continuous monitor, Section III describes the continuous monitor and its various controllers, Section IV derives the small-signal model for the monitor and designs the controllers, Section V presents the experimental results to validate the proposed monitor and Section VI summarizes the findings.

II. NODAL STABILITY ANALYSIS

The proposed continuous system stability monitoring technique evaluates stability using measurements at the terminals of the converter that incorporates it. The approach relies on measurements directly available to the converter, namely the dc link voltage at its terminals and the current injected by the converter into the dc bus. This data provides information about the system impedance as seen from the terminals of the monitoring converter. The impedance that the monitoring converter sees is the parallel combination of all sources, loads and bidirectional converters connected to the system, and there is no way for it to distinguish sources from loads in the impedance measurement at its terminals. As a result, the traditional impedance-based stability analysis methods [26]– [28] that divide the system into source and load subsystems cannot be used with the proposed monitor. The Nodal Stability Analysis proposed by the authors in [23], which is summarized here, presents an impedance-based analysis method that does not require identification or grouping of sources and loads, making it the ideal candidate for such applications.

In this paper, all impedances beginning with 'Z', admittances beginning with 'Y', compensators beginning with 'G' and small-signal forms (e.g. $\hat{x}$) of signals (e.g. x in this

case) are functions of the Laplace variable 's'. Consider a dc microgrid comprising n converters connected to a common dc bus, where all converters are represented by their Thevenin equivalent, as shown in Fig. 2. The small-signal dc bus voltage is given by

$$\hat{v}_{bus} = \left(\sum_{i=1}^{n} \frac{\hat{v}_i}{Z_{oi}}\right) Z_{bus}, \tag{1}$$

where

$$Z_{bus} = (Z_{o1}//Z_{o2}//...//Z_{on}). \tag{2}$$

In (1) and (2), $\hat{v}_i$ and Z_{oi} are the Thevenin equivalent voltage and output impedance of the i-th converter, respectively, and Z_{bus} is the overall impedance that appears to the dc bus from the parallel combination of the impedances Z_{oi}. Assuming the converters are individually stable when connected to an ideal dc bus, which is typically true, the system stability is given by the stability of Z_{bus} [23].

The stability of the dc bus impedance Z_{bus} is determined in [23] by expanding (2). One such expansion of Z_{bus} is given by

$$Z_{bus} = \frac{Z_{o1}Z_{away,1}}{Z_{o1} + Z_{away,1}} = \frac{Z_{o1}}{1 + \frac{Z_{o1}}{Z_{away,1}}} = \frac{Z_{away,1}}{1 + \frac{Z_{away,1}}{Z_{o1}}}, \tag{3}$$

where $Z_{away,1}$ is the parallel combination of all converter impedances except Z_{o1}. The expansion shown in (3) corresponds to partitioning the system at the terminals of the monitoring converter, referred to as converter 1 in Fig. 2. Z_{bus} is expressed in the form of a closed loop system representing interactions of all interconnected converters with a minor loop gain represented by the ratio of the monitor output impedance Z_{o1} and the impedance of the rest of the system, $Z_{away,1}$. Here, monitor output impedance refers to the impedance of the monitoring converter as seen from the dc bus. From (3), the dc bus impedance is stable if the impedance minor loop gain (IMLG), $Z_{oi}/Z_{away,i}$, satisfies the Nyquist stability criterion [23]. It is shown through hardware results in [23] that the IMLG can be evaluated at the dc bus terminals of any converter in the system, and it is not necessary to group or identify source and load converters in Z_{away} to perform the analysis. This property is utilized in this paper to develop the continuous monitoring technique, which evaluates the system stability by continuously measuring the crossover frequency and phase margin of the IMLG.

III. CONTINUOUS STABILITY MARGIN MONITOR

From (3), it can be noted that if both impedances are perturbed using the same current perturbation $\hat{i}_o$, then the IMLG can be written as

$$IMLG = \frac{Z_o}{Z_{away}} = \frac{\hat{v}_s\hat{i}_o}{\hat{v}_o\hat{i}_o} = \frac{\hat{v}_s}{\hat{v}_o}, \tag{4}$$

where $\hat{v}_s$ is the response of Z_o to $\hat{i}_o$, and $\hat{v}_o$ is the response of Z_{away} to $\hat{i}_o$, respectively. Utilizing the freedom of system partitioning [23], any converter in a local region of a dc microgrid can be assigned the monitoring task. Larger systems may require one converter to be assigned in each local region. The assigned converter(s) then inject a current perturbation to

the system and directly measure v_o (the response of Z_{away}) and i_o, as indicated in the overall schematic of the continuous monitor in Fig. 3.

The measured i_o is used with the analytical model of the converter output impedance to calculate v_s. With v_s and v_o, the system stability margin can be determined since the frequency at which the amplitudes of v_s and v_o are equal is the minor loop gain crossover frequency, and the phase margin of the minor loop gain is given by how far the phase difference of v_s and v_o is from 180° at that frequency [24]. The process is described further in the following subsections.

A. Injection Response and Filtering

As shown in Fig. 3, a sine-wave generator outputs a single frequency perturbation with frequency f_{inj} and amplitude A, which is added on top of the base current reference i_{ref0} and fed into the converter current regulator, which may regulate the output or input current of the converter power stage. The injected current i_o and the response voltage v_o are measured and fed into a band-pass filter tuned at the injection frequency f_{inj}. The band-pass filter coefficients are computed online and the filter expression is given by

$$G_{bp}(s) = \frac{\left(\frac{2\pi f_{inj}}{Q}\right)s}{s^2 + \frac{2\pi f_{inj}}{Q}s + (2\pi f_{inj})^2}, \tag{5}$$

where Q is the quality factor of the filter (usually set high), and f_{inj} is the same frequency at which i_{inj} is generated. The dynamic parameter f_{inj} in (5) requires that the parameters of the band-pass filter be evaluated continuously as f_{inj} changes, making it essential that the rate-of-change of f_{inj} be much smaller than the value of f_{inj}. The response filter is further augmented with a quadrature generator with the transfer function

$$G_q(s) = \frac{(2\pi f_{inj} - s)}{(2\pi f_{inj} + s)}. \tag{6}$$

The band-pass filter output is fed into the quadrature generator, which outputs a 90° phase-shifted signal with the same frequency and amplitude as the band-pass filter output. Hence, the response filters output four signals where

$$\begin{aligned} \hat{v}_{od} = G_{bp}\hat{v}_o, &\quad \hat{v}_{oq} = G_q\hat{v}_{od}, \\ \hat{i}_{od} = G_{bp}\hat{i}_o, &\quad \hat{i}_{oq} = G_q\hat{i}_{od}. \end{aligned} \tag{7}$$

The filtered currents, i_{od} and i_{oq} are fed into the analytical model of Z_o to calculate v_{sd} and v_{sq}. These are then fed into the envelope tracking and phase detection algorithm, which outputs the phase margin and amplitudes of v_o and v_s at the frequency f_{inj}.

B. Envelope Tracking

The envelope tracking algorithm tracks the cycle-by-cycle maximum and minimum of the inputs, denoted by v_{omax}, v_{omin}, v_{smax} and v_{smin} in Fig. 4. The amplitudes and zero offsets are then computed as

$$\begin{aligned} v_{op} = \frac{v_{omax} - v_{omin}}{2}, &\quad v_{omid} = \frac{v_{omax} + v_{omin}}{2}, \\ v_{sp} = \frac{v_{smax} - v_{smin}}{2}, &\quad v_{smid} = \frac{v_{smax} + v_{smin}}{2}. \end{aligned} \tag{8}$$

The phase difference ϕ between v_o and v_s is computed by detecting the mid-point crossings with their respective dc offsets v_{omid} and v_{smid}. By using the filtered and quadrature signals, and utilizing all mid-point crossings, peaks and troughs, the amplitudes and phase of v_o and v_s are updated four times in every period. This gives us a sampling rate of amplitudes and phase of four times the injection frequency f_{inj}, which reduces the control delay when the regulators for frequency f_{inj} and amplitude A of the injection i_{inj} are enabled.

C. Injection Amplitude and Frequency Regulation

When a continuous perturbation is injected in a dc microgrid, it is desirable to minimize the amplitude of the perturbation so that the perturbation does not violate the voltage ripple constraint nor affect the normal operation of the system. At the same time, the perturbation and its response must be detectable for the monitor operation. The Amplitude Controller block shown in Fig. 3 controls the perturbation amplitude by using the amplitude feedback v_o of the bus voltage, and adjusts the amplitude A of the injection current i_{inj} based on a reference V_{pref}. V_{pref} is chosen to be a small percentage of the rated bus voltage to ensure that the perturbation amplitude is acceptable.

The Injection Frequency Controller block in Fig. 3 uses v_{op} and v_{sp} as the feedback signals, and adjusts the frequency of injection f_{inj} until the IMLG in (4) approaches one, i.e. $v_{op} = v_{sp}$. The system IMLG crossover frequency $f_{c,sys}$ is then given by

$$f_{c,sys} = f_{inj}\big|_{(v_{op}=v_{sp})}. \tag{9}$$

Furthermore, when (9) is satisfied, the phase margin of the system IMLG, hereby denoted as PM_{sys}, is given by

$$PM_{sys} = 180 - \phi\big|_{(f_{inj}=f_{c,sys})}, \tag{10}$$

where ϕ is the phase difference between v_o and v_s, as shown in Fig. 4.

IV. DESIGN OF THE STABILITY MARGIN MONITOR

Design of the injection amplitude and frequency controllers require knowledge of the dynamics of v_o and v_s to small-signal perturbations in A and f_{inj}. The modeling of the dynamics of such a system has been done in [24]. This paper re-visits the derivation of the continuous monitor loop dynamics with the goal of improving the regulator behavior. Small-signal modeling is presented, followed by analysis of variations in the dc gains. Then, a new control strategy based on the use of logarithms is proposed and analyzed.

A. Modeling of the Stability Monitor Loops

Consider the injection frequency regulator shown in Fig. 3. At an operating point where $f_{inj} = f_{s0}$, this would result in a steady-state injection current i_{s0} given by

$$i_{s0}(t) = A\cos(\phi_0(t)) = A\cos(w_{s0}t), \tag{11}$$

where $w_{s0} = 2\pi f_{s0}$, and A is the fixed amplitude of perturbation. Adding a small sinusoidal perturbation with a given frequency w_m into the frequency f_{s0}, we get

$$\begin{aligned} f_s(t) &= f_{s0} + \epsilon\cos(w_m t), \text{ and} \\ w_s(t) &= 2\pi f_s(t) = w_{s0} + \Delta w\cos(w_m t), \end{aligned} \tag{12}$$
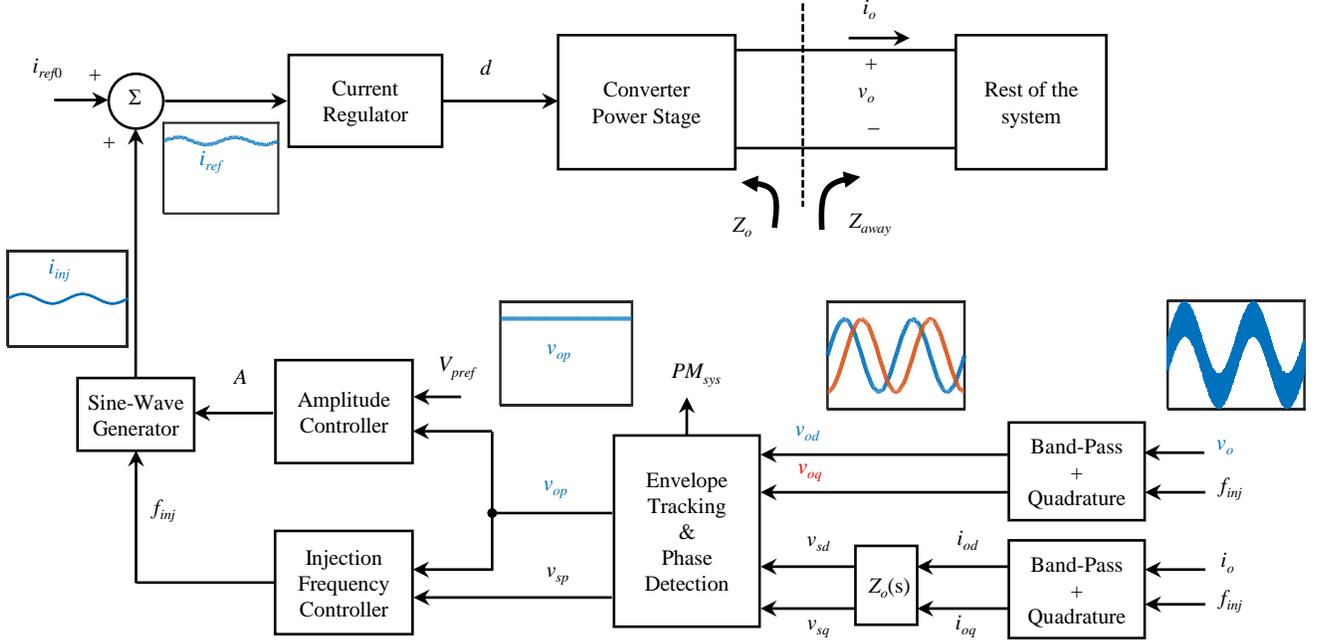
Fig. 3. Schematic of continuous stability margin monitor .

where $\Delta w = 2\pi\epsilon$ and $\epsilon << w_m$. The resulting phase $\phi(t)$ of $i_s(t)$ is given by

$$\phi(t) = \int w_s(t)dt = w_{s0}t + \frac{\Delta w}{w_m}\sin(w_m t). \quad (13)$$

Substituting (13) in (11), we get

$$i_s(t) = A\cos(w_{s0}t + \beta\sin(w_m t)), \quad (14)$$

where $\beta = \Delta w/w_m << 1$. Equation (14) can be expanded using Euler's identity and the Jacobi-Anger expansion [29]. Considering the zero-th and first order terms of the Jacobi-Anger expansion and ignoring the diminishing higher order terms, we get

$$\begin{aligned} i_s(t) = A\cos(w_{s0}t) &+ \frac{A\beta}{2}\cos((w_m + w_{s0})t) \\ &- \frac{A\beta}{2}\cos((w_{s0} - w_m)t). \end{aligned} \quad (15)$$
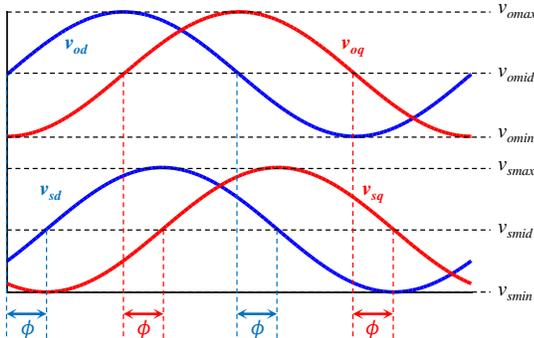
Fig. 4. Depiction of the envelope tracking algorithm.

The resulting form of $i_s(t)$ in (15) from the addition of small-signal perturbation in frequency is a well known response of frequency modulation, which results in sidebands $\pm w_m$ centered around the steady-state operating-point frequency w_{s0}. This perturbed injection $i_s(t)$ of (15) is then injected into the system through the current controller of the converter that implements it, as shown in Fig. 3. The remaining system in Fig. 3 from i_{inj} to v_o responds linearly to the three frequency components of (15), allowing us to use superposition to find the response of v_o to the perturbed i_s, which results in [30]

$$\begin{aligned} v_o(t) &= ||H||\cos(w_{s0}t + \angle H), \text{ where} \\ H &= H_0 + H_u e^{jw_m t} + H_l e^{-jw_m t}, \\ H_0 &= AG_{v_o}(jw_{s0}), \\ H_u &= \frac{A\beta}{2}G_{v_o}\big(j(w_{s0} + w_m)\big), \\ H_l &= -\frac{A\beta}{2}G_{v_o}\big(j(w_{s0} - w_m)\big). \end{aligned} \quad (16)$$

In (16), $G_{v_o}(jw)$ is the small-signal model of the plant from i_{ref} to v_o given by

$$G_{v_o}(jw) = \frac{\hat{v}_o(jw)}{\hat{i}_{ref}(jw)} = \frac{\hat{i}_o(jw)}{\hat{i}_{ref}(jw)}Z_{away}(jw). \quad (17)$$

Linearizing the amplitude $||H||$ of v_o from (16), we get

$$\begin{aligned} v_{op}(t) = ||H|| &\cong ||H_0|| \\ &+ \frac{||H_0^* H_u + H_0 H_l^*||}{||H_0||}\cos(w_m t + \angle(H_0^* H_u + H_0 H_l^*)). \end{aligned} \quad (18)$$

The first term in (18) is the response of the steady-state input $i_{s0}(t)$ from (11). The second term in (18) is the response of the perturbation in the injection frequency. Since the amplitude

of perturbation was Δw, the envelope transfer function from f_{inj} to v_o is found as [30]

$$
\begin{aligned}
G_{v_{op}f}(jw) &= \frac{H_0^* H_u + H_0 H_l^*}{||H_0||}, \text{ where} \\
H_0 &= A G_{v_o}(jw_{s0}), \\
H_u &= \frac{A}{2w} G_{v_o}(j(w_{s0} + w)), \\
H_l &= -\frac{A}{2w} G_{v_o}(j(w_{s0} - w)).
\end{aligned}
\tag{19}
$$

A similar derivation for the envelope transfer function from A to v_o leads to [30]

$$
\begin{aligned}
G_{v_{op}A}(jw) &= \frac{H_0^* H_u + H_0 H_l^*}{||H_0||}, \text{ where} \\
H_0 &= A G_{v_o}(jw_{s0}), \\
H_u &= \frac{1}{2} G_{v_o}(j(w_{s0} + w)), \\
H_l &= \frac{1}{2} G_{v_o}(j(w_{s0} - w)).
\end{aligned}
\tag{20}
$$

The transfer functions in (19) and (20) are the frequency responses of v_{op} to small-signal perturbations in f_{inj} and A respectively. The transfer functions from f_{inj} and A to v_{sp} are similarly derived as $G_{v_{sp}f}(jw)$ and $G_{v_{sp}A}(jw)$ respectively, with the plant transfer function given

$$
G_{v_s}(jw) = \frac{v_s(jw)}{i_{ref}(jw)} = \frac{i_o(jw)}{i_{ref}(jw)} Z_o(jw).
\tag{21}
$$

Using the derivations presented here, the overall open-loop transfer functions from control to error can be computed for the continuous monitor amplitude and frequency loops.

B. Analysis of Monitor Control Loops

Let the amplitude and frequency controllers in the continuous monitor shown in Fig. 3 be $G_{ca}(jw)$ and $G_{cf}(jw)$ respectively, such that

$$
\begin{aligned}
\hat{u}_A &= G_{ca}\hat{v}_{err,A}, \text{ and} \\
\hat{u}_f &= G_{cf}\hat{v}_{err,f},
\end{aligned}
\tag{22}
$$

where $v_{err,A}$, u_A, $v_{err,f}$, u_f are the input and output of the amplitude and frequency controller respectively. The control strategy used in [31] for deriving the small-signal model implies that

$$
\begin{aligned}
u_A &= A, \quad v_{err,A} = V_{pref} - v_{op}, \\
u_f &= f, \quad v_{err,f} = v_{sp} - v_{op}.
\end{aligned}
\tag{23}
$$

Following the derivation in Section IV-A, the open-loop transfer functions from u_A to $-v_{err,A}$ and from u_f to $-v_{err,f}$ are found as

$$
\begin{aligned}
G_{v_{err,A}}(jw) &= G_{v_{op}f}(jw), \text{ and} \\
G_{v_{err,f}}(jw) &= G_{v_{op}f}(jw) - G_{v_{sp}f}(jw).
\end{aligned}
\tag{24}
$$

In [31], it was shown that the dc gain of the open-loop transfer functions of (24) are given by

$$
G_{v_{err,A}}(0) = ||G_{v_o}(jw_{s0})||, \text{ and}
$$

$$
G_{v_{err,f}}(0) = A \left(\frac{\partial ||G_{v_o}(jw)||}{\partial w} - \frac{\partial ||G_{v_s}(jw)||}{\partial w} \right) \Bigg|_{w=w_{s0}},
\tag{25}
$$

where $G_{v_o}(jw)$ and $G_{v_s}(jw)$ are given in (17) and (21) respectively.

Assuming that the current control bandwidth of the converter chosen as the continuous monitor is higher than the injection frequency, (17) and (21) can be approximated as

$$
\begin{aligned}
G_{v_o}(jw) &\approx K Z_{away}(jw), \\
G_{v_s}(jw) &\approx K Z_o(jw),
\end{aligned}
\tag{26}
$$

where K is the conversion ratio from i_o to the current controlled by the converter, and $K = 1$ if the converter explicitly controls the output current. Equations (25) and (26) show that the dc gain for the amplitude loop is directly proportional to the magnitude of the impedance Z_{away}. For the impedances Z_o and Z_{away} to have a magnitude crossover in the frequency spectrum, one of them would have to behave inductive and the other capacitive. Using this fact, it can be shown that the dc gains approximately follow the relationships given by

$$
G_{v_{err,A}}(0) \propto \begin{cases} w_{s0} & \text{if } Z_o \text{ is inductive,} \\ \frac{1}{w_{s0}} & \text{if } Z_o \text{ is capacitive,} \end{cases}
\tag{27}
$$

and

$$
G_{v_{err,f}}(0) \propto A \frac{1}{w_{s0}^2}.
\tag{28}
$$

Equations (27) and (28) show that the dc gains of the continuous monitor loops change a lot with changes in operating injection amplitude and frequency. This can lead to unstable G_{ca} and G_{cf} if they are optimized for one operating point, or they can be too slow if designed for the worst case operating point. It is desirable to linearize the feedback loop in a way that reduces loop gain variation with respect to the operating point. In this work, feedback linearization is achieved by using logarithms.

C. Feedback Linearization Using Logarithms

The linear control strategy of (23) can be depicted in block diagram as shown in Fig. 5(a). This control strategy leads to variations in the loop gain given by (27) and (28). To reduce the variations in the loop gain, a new control strategy is proposed, where

$$
\begin{aligned}
u_A &= \log(A), \quad v_{err,A} = \log\left(\frac{v_{op}}{V_{pref}}\right), \\
u_f &= \log(f), \quad v_{err,f} = \log\left(\frac{v_{op}}{v_{sp}}\right).
\end{aligned}
\tag{29}
$$

The block diagram of the proposed control strategy is shown in Fig. 5(b). Both control strategies shown in Fig. 5 achieve the same objective, i.e. bring f to the system crossover frequency of (9) where $v_{op} = v_{sp}$, and bring the perturbation amplitude in the dc bus voltage v_o to V_{pref}. The benefits of the proposed control strategy is evaluated next.

Consider a derivation similar to the one used in Section IV-A. Adding a small sinusoidal perturbation with a given frequency w_m in the output of G_{cf}, we get

$$
\begin{aligned}
u_f(t) &= \log(f_{s0}) + \epsilon\cos(w_m t), \text{ which gives} \\
f_s(t) &= f_{s0} \times e^{\epsilon\cos(w_m t)}, \text{ and} \\
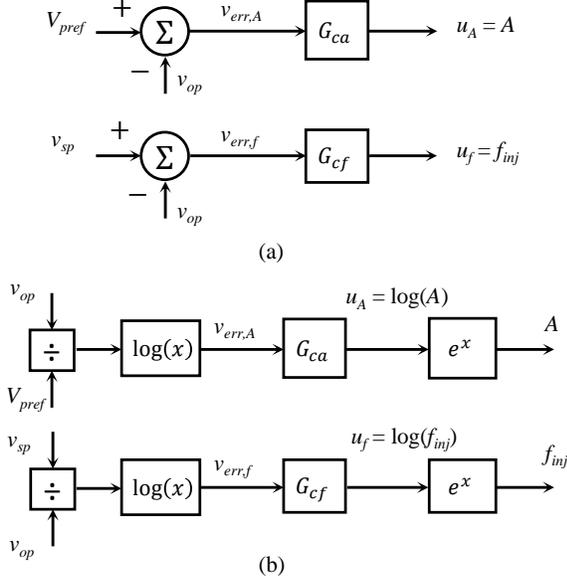w_s(t) &= w_{s0} \times e^{\epsilon\cos(w_m t)}.
\end{aligned}
\tag{30}
$$

Fig. 5. Realization of continuous monitor controllers; (a) linear, and (b) logarithmic.

Asserting that $\epsilon << 1$, $w_s(t)$ can be expanded as

$$w_s(t) = w_{s0} + w_{s0}\Delta w \cos(w_m t), \quad (31)$$

where $\Delta w = \epsilon$. The phase $\phi(t)$ is found as

$$\phi(t) = \int w_s(t)dt = w_{s0}t + \frac{w_{s0}\Delta w}{w_m}\sin(w_m t), \quad (32)$$

which results in the injection current $i_s(t)$ given by

$$i_s(t) = A\cos(w_{s0}t + \beta\sin(w_m t)), \quad (33)$$

where $\beta = w_{s0}\Delta w/w_m << 1$. Notice that (33) is the same as (14) with the only difference being the scaling factor β. The rest of the derivation follows similar to Section IV-A, resulting in v_{op} given by

$$v_{op}(t) \cong$$
$$AG_{v_o}(jw_{s0}) + ||G_{v_{op}f}(jw_m)||\cos(w_m t + \angle G_{v_{op}f}(jw_m)). \quad (34)$$

Similarly, v_{sp} can be found as

$$v_{sp}(t) \cong$$
$$AG_{v_s}(jw_{s0}) + ||G_{v_{sp}f}(jw_m)||\cos(w_m t + \angle G_{v_{sp}f}(jw_m)). \quad (35)$$

From (29), $v_{err,f}$ is computed by taking logarithm of the ratio of v_{op} and v_{sp}, which gives

$$v_{err,f}(t) =$$
$$\log\left(\frac{A||G_{v_s}(jw_{s0})|| + ||G_{v_{sp}f}(jw_m)||\cos(w_m t + \angle G_{v_{sp}f}(jw_m))}{A||G_{v_o}(jw_{s0})|| + ||G_{v_{op}f}(jw_m)||\cos(w_m t + \angle G_{v_{op}f}(jw_m))}\right). \quad (36)$$

Using the small-signal approximations

$$||G_{v_{sp}f}(jw_m)|| << A||G_{v_s}(jw_{s0})||, \text{ and}$$
$$||G_{v_{op}f}(jw_m)|| << A||G_{v_o}(jw_{s0})||, \quad (37)$$

Equation (36) can be expanded to find the overall open-loop transfer function for $G_{v_{err},f}$, resulting in

$$G_{v_{err},f}(jw) = G_{v_{op}f}(jw) - G_{v_{sp}f}(jw), \quad (38)$$

where

$$G_{v_{op}f}(jw) = \frac{H_0^* H_u + H_0 H_l^*}{||H_0||^2},$$
$$H_0 = G_{v_o}(jw_{s0}),$$
$$H_u = \frac{w_{s0}}{2w}G_{v_o}(j(w_{s0} + w),$$
$$H_l = -\frac{w_{s0}}{2w}G_{v_o}(j(w_{s0} - w)), \quad (39)$$

and

$$G_{v_{sp},f}(jw) = \frac{H_0^* H_u + H_0 H_l^*}{||H_0||^2},$$
$$H_0 = G_{v_s}(jw_{s0}),$$
$$H_u = \frac{w_{s0}}{2w}G_{v_s}(j(w_{s0} + w),$$
$$H_l = -\frac{w_{s0}}{2w}G_{v_s}(j(w_{s0} - w)), \quad (40)$$

Using a similar derivation for the amplitude loop, $G_{v_{err}A}$ is found as

$$G_{v_{err},A}(jw) = \frac{H_0^* H_u + H_0 H_l^*}{||H_0||^2}, \text{ where}$$
$$H_0 = G_{v_o}(jw_{s0}),$$
$$H_u = \frac{1}{2}G_{v_o}(j(w_{s0} + w),$$
$$H_l = \frac{1}{2}G_{v_o}(j(w_{s0} - w). \quad (41)$$

It can be shown that the dc gains of $G_{v_{err},f}$ and $G_{v_{err}A}$ are

$$G_{v_{err},f}(0) = \left(\frac{\frac{\partial||G_{v_o}(jw)||}{||G_{v_o}(jw)||}}{\partial w/w} - \frac{\frac{\partial||G_{v_s}(jw)||}{||G_{v_s}(jw)||}}{\partial w/w}\right)\Bigg|_{w=w_{s0}}, \text{ and}$$
$$G_{v_{err},A}(0) = 1. \quad (42)$$

Equation (42) shows that using logarithms as presented in (29), the amplitude loop transfer function has a fixed dc gain of one, making its controller completely independent of the operating point. The expression for $G_{v_{err},f}(0)$ in (42) can be interpreted as being the percent change in impedance magnitude resulting from a percent change in frequency. For highly inductive or capacitive impedances, $G_{v_{err},f}(0)$ becomes a constant. For other cases, $G_{v_{err},f}(0)$ is a function of impedances, but the variation is less than (28). Furthermore, unlike (25), $G_{v_{err},f}(0)$ in (42) is independent of variations in A.

In order to evaluate the models developed in this section, the next section presents a hardware setup, and uses small-signal models to show the design of the continuous monitor regulators. Furthermore, analytical models and measurements of the converter output impedances are used to predict the system stability, and then compared with the output of the continuous monitor to show its effectiveness in tracking stability of the dc microgrid as the system operating point varies.

V. EXPERIMENTAL RESULTS

This section presents a hardware setup designed for the purpose of evaluating the performance of the continuous monitor. A representative dc microgrid is formed with multiple converters that provide interfaces to the dc bus, including a voltage source converter (VSC), power load (Load) and energy storage converter (ESC). The continuous monitor function is
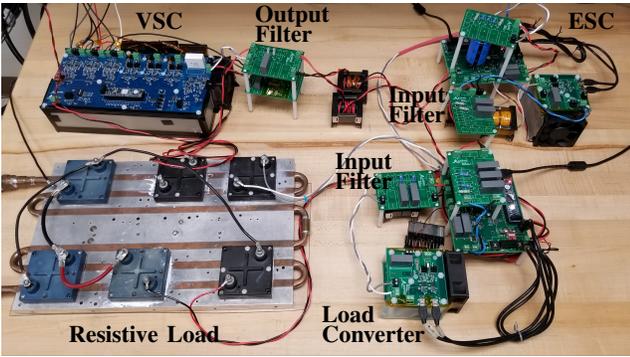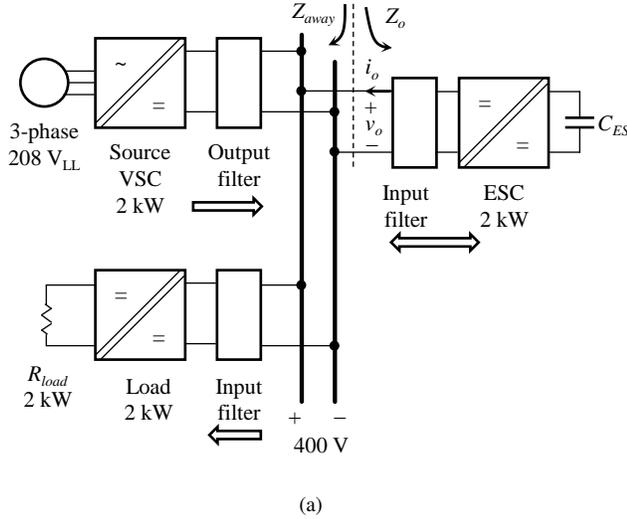
Fig. 6. Overall test setup for evaluating the continuous monitor: (a) block diagram and (b) experimental setup.

	VSC	Load	ESC
Topology	2-level 3-phase	Buck	Buck/Boost
I/O Voltage	208 V$_{LL}$/400 V	400 V/340 V	400 V/200 V
P_{rated}	2 kW	2 kW	2 kW
Switching Freq.	100 kHz	100 kW	100 kW
Main Inductor	630 μH	215 μH	300 μH
I/O filter (L, C, Rd, Cd)	N/A, 2.5 μF, 6 Ω, 3.3 μF	300 μH, 3.5 μF, 8 Ω, 6.6 μF	300 μH, 3.5 μF, 8 Ω, 6.6 μF
G_{ci} Bandwidth	150 Hz	10 kHz	10 kHz
G_{cv} Bandwidth	30 Hz	1 kHz	10 Hz

troller regulates the line currents and an outer loop regulates the dc bus voltage. On the dc bus, a capacitive output filter is employed along with an RC-branch similar to [23], to damp the resonance between the phase reactors and the dc output capacitor. With the control architecture described here, the analytical model for the source converter output impedance looking into the dc terminals, Z_{source}, is derived as

$$Z_{source} = \frac{Z_{dc}}{1 + Z_{dc}Y_s}, \tag{43}$$

where Z_{dc} is the impedance of the dc output filter including the dc bus capacitor and the RC-branch, and Y_s is given by [34]

$$Y_s = \frac{3}{2V_{dc}^2}\left\{\frac{(V_1 + sLI_1)[V_1 + V_{dc}^2 G_{ci}G_{cv}]}{sL + V_{dc}G_{ci}} - V_1I_1\right\}, \tag{44}$$

where G_{ci} is the current compensator, G_{cv} is the voltage compensator, and the remaining parameters are adopted from [34]. The impedance model of (43) and (44) is derived based on the assumption that the 3-phase 208 V$_{LL}$ power source is an ideal voltage source, thereby ignoring the dynamics of the phase-locked loop and the 3-phase power source [34].

The load converter is a traditional synchronous buck converter with an LC-filter at the input and an LC-filter at the output, both augmented with an RC-branch to damp the resonances of the LC filters. The load converter has a fast inner control loop regulating the buck-inductor current, and an output loop regulating the load resistor voltage. The input impedance, Z_{Load}, of the buck converter, with its control loops and filters, is given by

$$Z_{Load} = Z_{Lin} + \frac{Z_{conv}Z_{Cin}}{Z_{conv} + Z_{Cin}}, \tag{45}$$

where Z_{Lin} is the impedance of the input inductor, Z_{Cin} is the impedance of the input capacitor in parallel with the RC-branch, and Z_{conv} is given by

$$Z_{conv} = \frac{Z_L + Z_{RCload} + G_{ci}G_{cv}V_{dc}Z_{RCload} + G_{ci}V_{dc}}{D[D - G_{ci}G_{cv}I_LZ_{RCload} - G_{ci}I_L]}, \tag{46}$$

where Z_L is the impedance of the buck-inductor, Z_{RCload} is the impedance of the load resistance in parallel with output capacitor and RC-branch, G_{ci} is the current compensator, G_{cv} is the voltage compensator, V_{dc} is the dc bus voltage and I_L is the current of the load resistor.

added to the ESC. Well known converter topologies are used with known small-signal models, and direct measurements are used to account for deviations from analytical models. The stability of the dc microgrid test setup is evaluated and compared using three approaches: analytical models, direct measurements and the proposed continuous monitor. Evaluations are performed over a range of load power to demonstrate the effectiveness of the monitor in determining the system crossover frequency and stability margin.

A. Hardware Test Setup

The overall block diagram for the hardware test setup is shown in Fig. 6a. All three of the converters are built using the TI GaN devices with integrated gate drivers [32] and controlled using the CMOD A7 FPGAs [33]. All converters are rated for 400 V on the dc bus and 2 kW power. Fig. 6b shows a picture of the actual hardware setup. The converter topologies, passive components and control parameters are summarized in Table I.

The source converter shown in Fig. 6 is a two-level three-phase voltage source converter (VSC). Its controller board senses the three line currents, line-to-neutral voltages, the dc output current and the dc link voltage. A control architecture similar to [34] is employed, where a dq-domain current con-
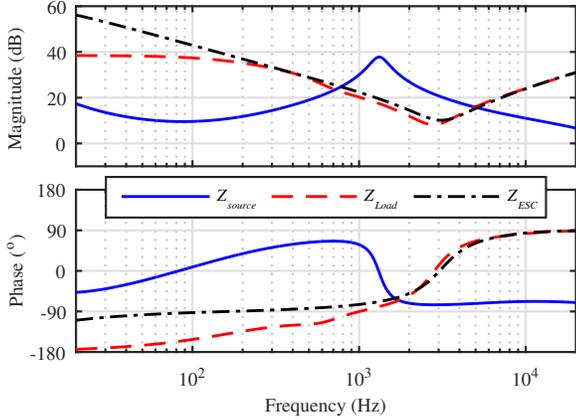
Fig. 7. Impedance response of Z_{source}, Z_{Load} and Z_{ESC}.
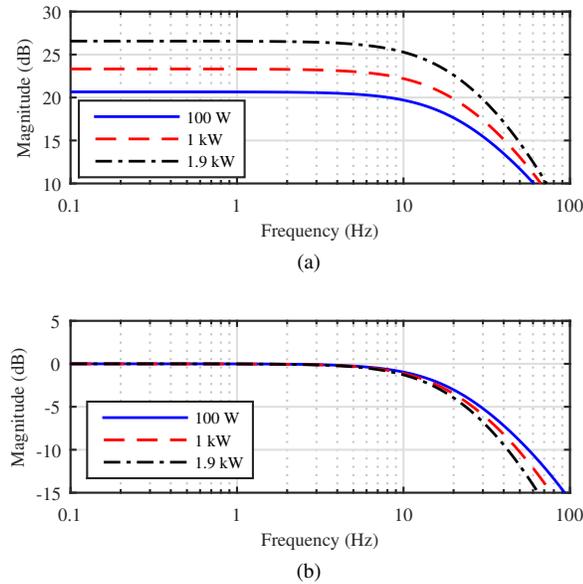

(a)

(b)

Fig. 8. Variation in $G_{v_{err},A}(jw)$ w.r.t changing load power; (a) with difference feedback, and (b) with logarithm feedback.

The Energy-Storage Converter (ESC) has the same topology, control architecture, and filters, as the load converter. Instead of a resistive load, the ESC has a bulk capacitance of 0.4 mF serving as the energy storage element. The current control bandwidth of the ESC is kept high (10 kHz) while the voltage control bandwidth kept very low (10 Hz), so that the ESC appears as a capacitive constant-current load on the dc bus. The analytical impedance model of the ESC, Z_{ESC} is exactly the same as that of the load converter, with only the bulk capacitor replacing the load resistor. The frequency responses of Z_{source}, Z_{Load} and Z_{ESC} with the load converter operating at 1900 W are presented in Fig. 7 based on the analytical models. It can be seen in Fig. 7 that the source impedance has a peak around 1.3 kHz resulting from a low control bandwidth. In this work, the source VSC control bandwidth has been kept low by design to emulate the source behavior in typical dc microgrids, where MW scale power sources use devices that switch up to a few kHz, limiting the

achievable control bandwidth. Furthermore, Fig. 7 shows that the load converter impedance behaves as a negative resistance, as indicated by its constant magnitude and $-180°$ phase at low frequencies.

The impedance models presented here are used to design the controllers of the continuous monitor, and a comparison is made between the loop gains resulting from the two control strategies shown in Fig. 5. For the control strategy of Fig. 5a, equation (24) is evaluated where $Z_o = Z_{ESC}$ and Z_{away} is the parallel combination of Z_{source} and Z_{Load}. For the control strategy of Fig. 5b, equations (38) and (41) are evaluated. These transfer functions are evaluated as the load power varies from 100 W to 1.9 kW. The results for the amplitude control loop, $G_{v_{err},A}(jw)$ are shown in Fig. 8. Fig. 8a shows that the variation in the amplitude loop due to operating point variation is about 6 dB for the difference control of Fig. 5a, while the variation is zero for the control using logarithms. The other loop gain variations are summarized in Table II. Table II shows that the variations in the amplitude and frequency loop dc gains are reduced significantly by using logarithms. Using these models, G_{cf} is designed with a bandwidth of 4 Hz and G_{ca} is designed with a bandwidth of 1 Hz.

B. Continuous Monitor Performance

The performance of the continuous monitor is evaluated by using the hardware setup shown in Fig. 6. At startup, the dc bus voltage is ramped up to 400 V with the VSC operating in closed loop. The ESC is then enabled and the voltage of the energy storage capacitor ramped up to 200 V. Next, the continuous injection and the continuous monitor controllers are enabled with the designed parameters. The FPGA controller of the ESC sends its continuous monitor outputs, $f_{c,sys}$ and PM_{sys} to the PC at 4 Hz rate using UART communication. The data is logged along with the timestamp for alignment with the data from other converters.

With the continuous monitor running, the load converter is enabled and the load power is ramped up slowly from 0 W to 1900 W and then back down to 0 W. The load converter sends its power reference to the PC for logging at 4 Hz rate with the timestamp using UART communication. Once the test is complete, the data from load converter and the ESC are aligned using the timestamp, and the variation of $f_{c,sys}$ and PM_{sys} w.r.t the load power is shown in Fig. 9. To validate the output of the continuous monitor, two methods are used: analytical model prediction and direct impedance measurement using psuedo-random binary sequence (PRBS)

TABLE II
VARIATIONS IN CONTROL LOOP DC GAINS.

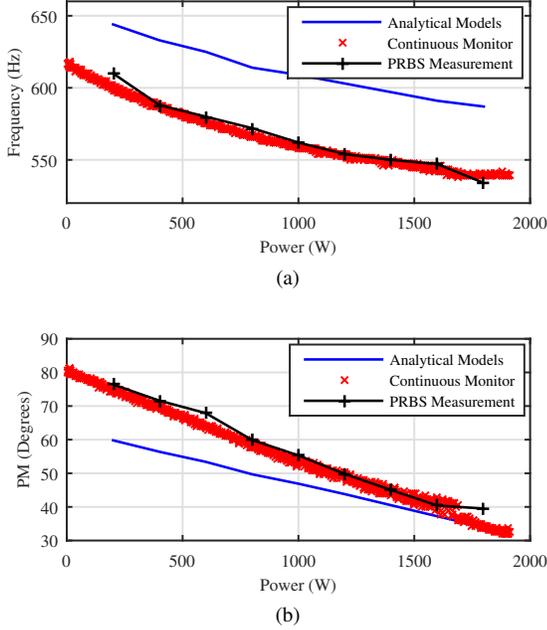|	Change in Operating Point (0.1 kW - 1.9 kW)		Change in Perturbation Amplitude (1 V - 3 V)	
	$G_{v_{err},A}(0)$	$G_{v_{err},f}(0)$	$G_{v_{err},A}(0)$	$G_{v_{err},f}(0)$
Difference control	6 dB	5 dB	0 dB	9.5 dB
Logarithm control	0 dB	3 dB	0 dB	0 dB

Fig. 9. Continuous monitor performance w.r.t changing load power; (a) identified system crossover frequency, and (b) identified system phase margin.

Fig. 10. Comparison of analytical model and direct impedance measurement.

injection [11]. For analytical model prediction, the impedance models presented in section V-A are evaluated at load power levels from 200 W to 1800 W, and the resulting Z_o and Z_{away} are plot together to find the crossover frequency and phase margin. For direct measurement, a 12-bit PRBS signal of length 4095 is injected at 25 kHz rate into the current reference of the ESC at nine operating points with load power ranging from 200 W to 1800 W. The current injected into the dc bus (i.e. the current driven into the parallel combination of Z_{source} and Z_{Load}) is recorded along with the dc bus voltage. Fast Fourier Transform (FFT) is performed on the injected current and response voltage to find the frequency spectra. Then the ratio of the voltage spectrum to the current spectrum is computed to calculate the frequency spectrum of the combined impedance Z_{away}. This measured impedance is used along with the analytical model of Z_{ESC} to determine the PRBS-based stability results shown in Fig. 9.

C. Evaluation of Continuous Monitor Results

Fig. 9a shows that $f_{c,sys}$ reduces from around 615 Hz to 540 Hz as the load power changes from 0 W to 1900 W. Similarly, Fig. 9b shows that PM_{sys} changes from 80° to 31°. This trend in $f_{c,sys}$ and PM_{sys} is expected as the negative incremental resistance behavior of the load converter becomes more dominant at higher power levels. The continuous monitor output matches well with the PRBS-based direct measurement; however, although the trends align with the analytical models, neither the continuous monitor output nor direct measurement result matches the analytical prediction. To understand this, the analytical model and direct measurements of Z_{away} are shown in Fig. 10 along with the analytical model of Z_{ESC} at load power of 400 W.
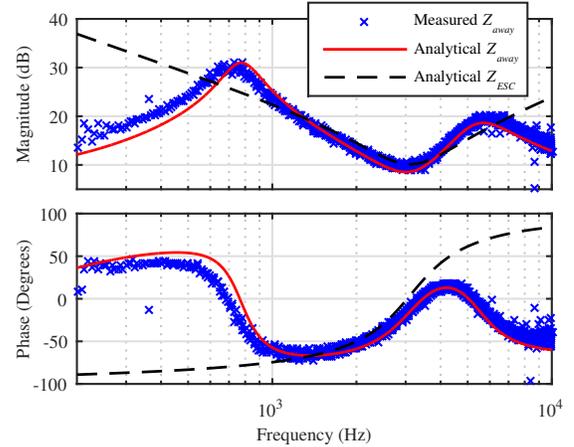
In Fig. 10, the analytical model response of Z_{away} is shown with a solid red curve, while measured Z_{away} is shown with blue cross, and the analytical model response of Z_{ESC} is shown with black dotted lines. Fig. 10 reveals that the magnitude response of the measured Z_{away} is shifted slightly to the left at lower frequencies and the phase is also lower compared to the analytical model. This is expected since the analytical model assumes that the 208 V$_{LL}$ three-phase source shown in Fig. 3 is a zero impedance voltage source, whereas the actual hardware of Fig. 6 uses a lab-scale power supply which has finite non-zero output impedance. This source output impedance affects Z_{away} at lower frequencies within the control bandwidths of the power source but not at higher frequencies where the impedance is dominated by the passive components of the converters. Furthermore, the analytical model does not account for losses in the converters, which add damping and lower the phase of the impedance response. The analytical model also assumes the passive components to be linear over the frequency range, which is never the case with real components. For instance, the phase inductors for the VSC in Fig. 6b are built using single strand AWG-16 laminated wire which resulted in 90 mΩ resistance at 60 Hz but the ac resistance increases rapidly with frequency, giving an R_{ac} of 16 Ω at 1 kHz. Thus, while it is easy to accurately model small systems (less than 100 W) with highly controlled passive components, it is nearly impossible to capture the dynamics of a medium to large scale power system using just analytical models. In such cases, the proposed continuous monitor provides a significantly more accurate measure of impedance and stability in the presence of uncertainties and a wide range of operating conditions.

VI. CONCLUSION

This paper presents a method for monitoring the stability of a dc microgrid, including the stability margin and the critical frequency. The proposed monitor injects a small perturbation into the system for monitoring stability, which does not affect normal operation of the system. This paper also presents detailed modeling of the continuous monitor dynamics, and

compares two control strategies for the design of the monitor. One control strategy uses difference feedback with linear output, resulting in low complexity and fewer resources to implement; however, its controller may suffer from variation of the operating points. It should be considered at design time whether the controller will be able to handle those variations. An alternative control strategy using logarithm feedback and logarithm output is also presented in this paper. It is shown that using logarithms result in controllers that do not suffer from operating point variations. The use of logarithms and exponential functions, however, come with higher resource usage.

The analytical development presented in this paper serves as a tool for the designer to pick a control strategy based on a compromise between implementation cost and design requirement. The proposed continuous monitor is implemented on to the energy-storage interfacing converter in a 2 kW lab scale dc microgrid. Its performance is evaluated by comparing the results to analytical model predictions and direct measurements. It is highlighted that, while analytical models are useful for designing the monitor, it cannot be relied upon for accurately capturing the damping of a real system and predicting stability as direct measurement can. The results show that the proposed monitor tracks stability in good agreement with direct measurement. The proposed method can be added to any existing converter in the dc microgrid as an auxiliary function. If there is no access to the control of the converters already in the system, another converter may be added with a fraction of the power rating and with capacitive energy storage to perform the monitoring task. In contrast to existing wideband identification methods, the proposed method outputs the stability measurement as a continuous signal, which opens up new possibilities of utilizing this for improving the stability of the dc migrogrid being monitored.

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CHAPTER 6

Active Stability Control of DC Microgrids using Dynamic Virtual Immittance

Active Stability Control of DC Microgrids using Dynamic Virtual Immittance

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Abstract—**Continued trend towards electrified transportation and integration of renewable energy presents new challenges in ensuring system stability. For systems where overdesign to meet stability requirements is not feasible, several methods have been proposed in literature for improving the system stability using control. This paper presents a method for actively controlling the stability of a dc microgrid by emulating a dynamic virtual immittance at the terminal of a converter interfacing energy storage. The proposed method utilizes outputs from a stability monitor in a feedback loop and actively regulates the system stability margin to a desired reference. Hardware tests performed on a lab scale 2 kW dc microgrid are used to validate the performance of the stability controller. It is shown that, with the proposed method, the system provides better damping to disturbances and proactively avoids becoming unstable.**

Index Terms—**impedance, stability, dc microgrid, monitoring, virtual immittance**

I. INTRODUCTION

AS the trend towards electrified transportation and integration of renewables into the electric grid continues, it is becoming more challenging to ensure system stability. Future dc microgrids are expected to incorporate different kinds of sources such as renewable energy and fuel-based generators. They are expected to be re-configurable, have bidirectional converters interfacing energy storage, and may have constant power, intermittent or plug and play loads. Furthermore, the future dc microgrids are expected to be higher power, and be scalable. Examples of such systems can be found in all-electric or more-electric aircraft, electric ships and dc fast charging stations [1]–[3]. Fig. 1 depicts a generic dc microgrid with sources, loads and bidirectional converters. Stability of such dc microgrids is deteriorated by the negative incremental resistance behavior of the constant power loads as well as interactions among the controllers of the interconnected converters as well as their filters [4], [5]. Traditional methods of ensuring stability through passive component design leads to oversized filter design and slow controllers [6]. Recent interest has been to investigate active methods for enhancing and ensuring stability of dc microgrids.

Active stabilization techniques can be classified as converter-level and system-level stabilization techniques. Converter-level stabilization targets stabilization of a converter control loop based on online measurement of loop gains [7]–[10], impedances [11] or detection of instability [12]. In [7], [8], the authors use single frequency continuous injection

to identify the crossover frequency and phase margin of a converter control loop, and then tune an adaptive filter continuously based on a desired phase margin. Authors in [9], [10] use wideband perturbation and identification methods to perform online identification of the converter loop gain frequency response, and then use it to re-tune the controller parameters for the desired stabilty margins. In [11], the authors use wideband perturbation to measure frequency response of nonlinear passive components in the power stage (e.g. iron-core inductor) and then re-tune the control parameters for optimal performance. Authors in [12] detect the oscillation frequency at the onset of instability and then re-program the compensator parameters to stabilize it. Converter-level stabilization techniques ensure the stability of a converter; however, when a converter is connected in a dc microgrid, stability of its local control loop does not guarantee stability of the interconnected system [13].

At the system-level, there has been a lot of recent development in active stabilization of dc microgrids. In [14], [15], the authors use passivity-based stability analysis and design feed-forward control to add damping into the dc bus impedance. Authors in [16], [17] measure the frequency and amplitude of oscillation at the onset of instability. Using that information, [16] tunes a virtual impedance emulated on the bus by an external current source and [17] adds phase around the critical frequency without changing the impedance magnitude. In [18], [19], the authors use the full system analytical model to design virtual impedance and use feedforward terms to emulate it. Most of the existing stabilization methods require apriori knowledge of the entire system [15], [18], [19]. The methods based on detection of instability [16], [17] can only be used as emergency measures, as normal operation of a dc microgrid
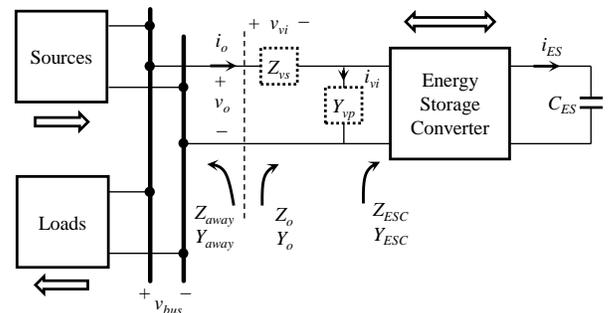

Fig. 1. A dc microgrid incorporating sources, loads, bidirectional energy storage and virtual impedance.

demands a certain stability margin. The measurement-based method in [14] overcomes the aforementioned challenges; however, it requires extensive computations for tuning or re-tuning of the feed-forward term.

This paper presents an active stabilization method for dc microgrids based on a dynamic virtual immittance (DVI), where immittance is used to combine impedance and admittance. The proposed DVI may be emulated at the terminal of one of the converters already in the dc microgrid, or emulated using an additional converter with a fraction of the power rating, added to the system and interfacing capacitive or battery energy storage. A feedback loop regulates the stability margin of the dc microgrid system in a similar manner as [7] does for a converter loop gain. The output of the stability regulator continuously adjusts parameters of the DVI to add just enough damping at the critical frequency as required to maintain the reference margin, thereby optimizing the reactive power required to support the system stability. In this paper, the stability margin and critical frequency are continuously evaluated using a continuous stability margin monitor [20], also implemented in the converter emulating the DVI. In general, however, application of the DVI can use any system stability monitor that provides information about the system stability and the critical frequency. The stability regulator, monitor and DVI are implemented in a single CMOD A7 field-programmable gate array (FPGA) [21] using fixed-point computations, along with the primary control functions of the converter, demonstrating low computational cost. Its performance is demonstrated on a lab scale 2 kW dc microgrid.

Throughout the paper, terms starting with 'Z', 'Y' and 'G' denote impedances, admittances and compensators respectively, and all are functions of the Laplace variable 's'. The paper is organized as follows: Section II describes the stabilization method and the DVI, Section III describes the design of the stability regulator and the monitor used in this paper, Section IV presents the hardware setup used for evaluating the stability regulator and the experimental results, and Section V summarizes the findings.

II. STABILITY ENHANCEMENT USING DYNAMIC VIRTUAL IMPEDANCE

The term dynamic virtual immittance (DVI) is used in this paper to distinguish it from traditional implementation of virtual impedance, as the coefficients of the DVI are continuously changing based on measurements at the terminal of the converter implementing it. Generally, virtual impedance may be implemented at the terminal of a converter as a series impedance, Z_{vs}, or parallel admittance Y_{vp}, as shown in Fig. 1. The bi-directional energy storage converter in Fig. 1 is chosen as the converter to implement the stability monitoring and regulation. A continuous stability margin monitor similar to [20] is used to determine the stability of the interconnected system. The monitor in [20] relies on Nodal Stability Analysis [13] to determine the system stability, which is summarized here.

A. Nodal Stability Analysis

The Nodal Stability Analysis [13] was proposed to overcome the requirement of grouping of sources and loads in impedance-based stability analysis methods [22]–[24]. For a dc microgrid such as that shown in Fig. 1, Nodal Stability Criterion states that the dc microgrid is stable if

- Individual converters are stable when connected to an ideal dc bus, and
- The dc bus impedance, Z_{bus}, is stable.

Here, Z_{bus} is the parallel combination of all of the converter output impedances. In [13], the authors have shown that the stability of Z_{bus} can be determined by partitioning the parallel combination at the terminal of one of the parallel-connected converter. For the partitioning shown in Fig. 1, this results in

$$Z_{bus} = \frac{Z_o Z_{away}}{Z_o + Z_{away,}} = \frac{Z_o}{1 + \frac{Z_o}{Z_{away}}} = \frac{Z_{away}}{1 + \frac{Z_{away}}{Z_o}}, \quad (1)$$

where Z_{away} is the parallel combination of all converter impedances except Z_o. Equation (1) shows Z_{bus} expressed in the form of a closed loop system representing interactions of all the interconnected converters and with a minor loop gain given by the ratio of the output impedance Z_o and the impedance of the rest of the system, Z_{away}. The closed loop system of (1) can equivalently be written as

$$Z_{bus} = \frac{Z_{o1}}{1 + \frac{Y_{away}}{Y_o}} = \frac{Z_{away}}{1 + \frac{Y_o}{Y_{away}}}, \quad (2)$$

where $Y_{away} = 1/Z_{away}$ is the total admittance of the converters except Y_o, which is the admittance of the energy storage converter. From (1) and (2), the impedance minor loop gain of the microgrid system is given by

$$\text{IMLG} = \frac{Z_o}{Z_{away}} = \frac{Y_{away}}{Y_o}. \quad (3)$$

The stability regulator developed in this paper measures the crossover frequency, $f_{c,sys}$, and phase margin, PM_{sys} of the IMLG and then regulates the phase margin at the desired reference by adding a DVI at the terminal of the chosen converter.

B. Dynamic Virtual Immittance

A virtual impedance at the terminal of a converter may be implemented by measuring the terminal output current i_o and adding a term v_{vi} in the voltage control loop, or by measuring v_o and adding a term i_{vi} in the current control loop, where v_{vi} and i_{vi} are given by

$$v_{vi} = Z_{vs} i_o, \text{ and}$$
$$i_{vi} = Y_{vp} v_o, \quad (4)$$

where Z_{vs} and Y_{vp} are shown in Fig. 1. The effect of these on the overall output impedance Z_o or admittance Y_o is given by

$$Z_o = Z_{vs} + Z_{ESC}, \text{ and}$$
$$Y_o = Y_{vp} + Y_{ESC}, \quad (5)$$

where Z_{ESC} and Y_{ESC} are impedance or admittance of the energy storage converter without the virtual impedance. The
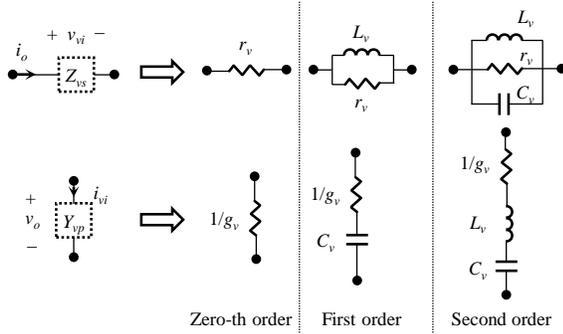
Fig. 2. Possible realizations of virtual impedance and admittance.

Fig. 3. Parameter variation in the realization of the DVI.

virtual impedance, Z_{vs}, or admittance, Y_{vp} may be realized using zero-th order, first order or second order filters as shown in Fig. 2. In Fig. 2, r_v is a virtual resistance, $g_v = 1/r_v$ is a virtual conductance, L_v is a virtual inductance and C_v is a virtual capacitance. Zero-th order virtual impedance leads to voltage or current droop characteristics, which affects dc-operating point as well as high frequency dynamics that can affect controller behavior. First order virtual impedance leads to droop with low-pass characteristics typical of practical passive damping implementations, which affects high frequency dynamics but does not affect dc operation. Second order virtual impedance leads to frequency-selective damping, which adds damping around target frequencies but neither affects dc-operation nor high frequency dynamics. This work uses second order virtual impedance as it achieves the objective with least impact on the system operation. Using parameters from Fig. 2 for Z_{vs}, we get

$$Z_{vs} = \frac{sw_0 r/Q}{s^2 + sw_0/Q + w_0^2}, \tag{6}$$

where r is the resistance, $w_0^2 = 1/LC$ and $Q = r/w_0 L$. Similarly, for Y_{vp}, we get

$$Y_{vp} = \frac{sw_0 g/Q}{s^2 + sw_0/Q + w_0^2}, \tag{7}$$

where g is the conductance, $w_0^2 = 1/LC$ and $Q = g/w_0 C$. Notice the similarity in the transfer functions (6) and (7). Combining (6) and (7) into a common representation, henceforth referred to as DVI, we get

$$G_v = \frac{sw_0 d_v/Q}{s^2 + sw_0/Q + w_0^2}, \tag{8}$$

where G_v corresponds to (6) or (7) depending on whether the input of G_v is i_o or v_o and the output v_{vi} or i_{vi} respectively. Equation (8) is a typical representation of a band-pass filter where w_0 is the center frequency, Q is the quality factor that has inverse relationship with the width of the band-pass region and d_v is the magnitude of G_v at w_0.

The DVI in (8) is parametric with three parameters that shape it. Fig. 3 shows the effect of parameter variation on the DVI, where the blue solid curve shows the baseline case with $w_0 = 2\pi(100)$, $Q = 0.25$ and $d_v = 1$. The pink dash-dot curve in Fig. 3 shows the effect of changing Q to 1, while the red dashed curve shows the effect of changing d to 10 and
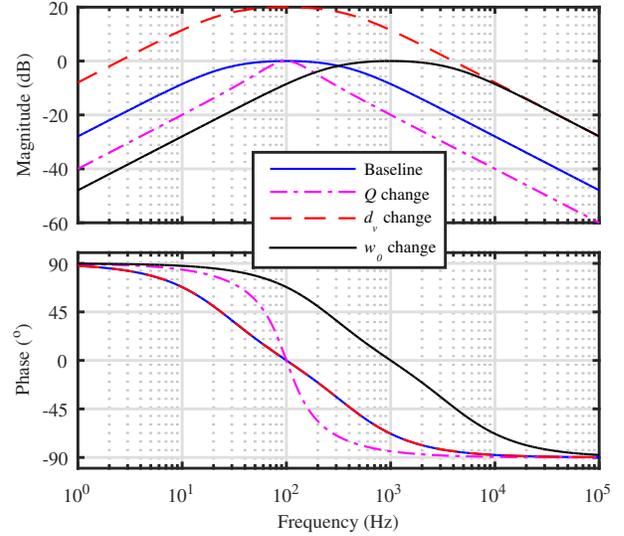
black solid curve shows the effect of changing w_0 to $2\pi(1000)$. It is evident that all three parameters affect different aspects of the DVI exclusively, i.e. Q changes the width of the band-pass region, w_0 shifts the DVI horizontally while d_v shifts the DVI vertically. Therefore, a controller may change one of the parameters in a feedback loop without affecting the other aspects, which may be changed by other control loops.

The DVI may be implemented into a micro-controller or an FPGA by discretizing it using the Tustin approximation [25]. For a generic input x and output y, this results in the difference equation given by

$$\begin{aligned} y[k] = K_{out} \big\{ 8y[k-1] - 4y[k-2] + K_0 y[k-2] \\ + K_0 d_v \big(x[k] - x[k-2] \big) \\ - K_1 \big(2y[k-1] + y[k-2] \big) \big\}, \end{aligned} \tag{9}$$

where K_0, K_1 and K_{out} are given by

$$\begin{aligned} K_0 &= \frac{2\omega_0 T_s}{Q}, \\ K_1 &= (\omega_0 T_s)^2, \text{ and} \\ K_{out} &= \frac{1}{4 + K_0 + K_1}. \end{aligned} \tag{10}$$

In (9) and (10), Q is the quality factor from (8), T_s is the sampling period of the converter implementing the DVI, d_v is the output of the stability regulator and $\omega_0 = 2\pi f_{c,sys}$ where $f_{c,sys}$ is the output of the stability monitor corresponding to the IMLG crossover frequency. The coefficients K_0, K_1 and K_{out} are computed based on the input $f_{c,sys}$, then used along with d_v to calculate the final coefficients at each time-step. These coefficients are then used to compute the k-th output of the DVI.

III. ACTIVE STABILITY CONTROL

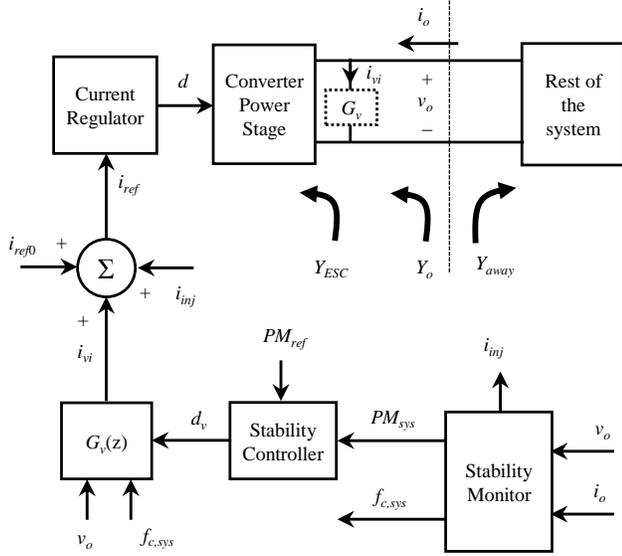This section describes the application of DVI in a dc microgrid as a closed loop system that actively regulates the

Fig. 4. Diagram of the stability regulator with DVI.

Fig. 5. Diagram of the stability margin monitor used in this work.

system stability margin.

A. Stability Regulation

In this work, admittance-based IMLG, Y_{away}/Y_o, is used and the DVI is implemented as shown in Fig. 4. The objective of the stability controller in Fig. 4 is to change d_v such that the modified IMLG given by

$$\text{IMLG} = \frac{Y_{away}}{Y_o} = \frac{Y_{away}}{Y_{ESC} + G_v} \tag{11}$$

has a phase margin at the crossover frequency, $f_{c,sys}$, that is equal to the desired phase margin, PM_{ref}. This is analogous to adding a series RLC branch, such as that shown in Fig. 2, tuned to provide a certain resistive loading at the resonant frequency, except that the resonant frequency and resistance is changing to track the reference margin as the system operating point changes.

While it is beneficial to use a stability monitor that outputs the system IMLG crossover frequency and phase margin continuously [20], it is not a necessity and does not limit the use of the stability regulator and DVI with other monitoring methods. For instance, wide-band perturbations [14], [26] can be used to periodically measure $f_{c,sys}$ and PM_{sys}. The only consideration would be the slow response time of the stability regulator with periodic wide-band measurement. In this work, the continuous stability margin monitor proposed in [20] is adapted to measure the admittance-based IMLG, and account for DVI in the impedance model of the converter performing regulation.

B. Continuous Stability Margin Monitor

The authors in [20] showed that the IMLG of (3) can be measured by using the ratio of voltages when both Z_o and Z_{away} are perturbed by the same current i_o. It can be seen
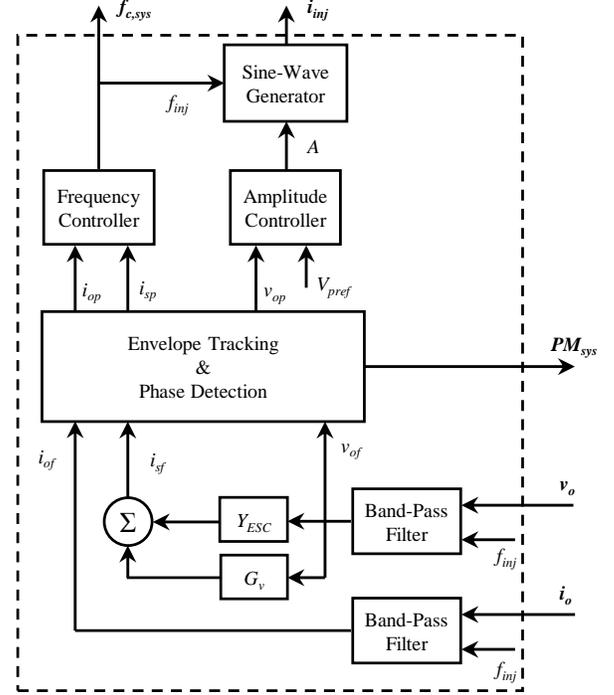
from (3) that if, instead of using current perturbation, the admittances Y_o and Y_{away} are perturbed by the same voltage perturbation, v_o, we get

$$\text{IMLG} = \frac{Y_{away}\hat{v}_o}{Y_o\hat{v}_o} = \frac{\hat{\hat{i}}_o}{\hat{\hat{i}}_s}, \tag{12}$$

where i_o is the response of Y_{away} to v_o, and i_s is the response of Y_o to v_o. Applying the same voltage perturbation in the presence of DVI, we get

$$\text{IMLG} = \frac{Y_{away}\hat{v}_o}{Y_o\hat{v}_o} = \frac{Y_{away}\hat{v}_o}{Y_{ESC}\hat{v}_o + G_v\hat{v}_o} = \frac{\hat{\hat{i}}_o}{\hat{\hat{i}}_s}, \tag{13}$$

where Y_{ESC} is the analytical model of the monitor converter admittance seen from the dc bus, and G_v is the DVI given by (8). Implementation of this strategy is shown in Fig. 5. The continuous monitor in Fig. 5 outputs a single frequency sine-wave perturbation i_{inj}, with amplitude A and frequency f_{inj}, that is added on top of the base current reference, i_{ref0}, as shown in Fig. 4. The perturbation travels through the converter and results in same-frequency perturbation in v_o and i_o, which are sensed at the terminal of the converter. As shown in Fig. 5, a bandpass filter, continuouysly tuned at f_{inj}, with a gain of 1 and quality-factor of 16, filters v_o and i_o and extracts their single-frequency components at f_{inj}, denoted by v_{of} and i_{of} respectively. Using superposition principle, the single-frequency component v_{of} is fed into the analytical models of Y_{ESC} and G_v, and their outputs are added to determine the total response, i_{sf}, as shown in Fig. 5.

The envelope tracking and phase detection block in Fig. 5 tracks the amplitudes of i_{of}, i_{sf} and v_{of}, denoted by i_{op}, i_{sp} and v_{op} respectively. The frequency controller uses i_{op} and i_{sp} as feedback signals and uses a compensator to change f_{inj}

until $i_{op} = i_{sp}$ [20]. This ensures that, in steady state, the injection frequency converges to the system IMLG crossover frequency given by

$$f_{c,sys} = f_{inj}\Big|_{i_{op}=i_{sp}}. \tag{14}$$

The phase margin of the IMLG, PM_{sys} is computed by measuring the phase difference of i_{of} and i_{sf} by using their zero crossings [20]. The phase margin is then given by

$$PM_{sys} = 180\big(1 - 2\Delta t_{zc}f_{inj}\big)\Big|_{f_{inj}=f_{c,sys}}, \tag{15}$$

where Δt_{zc} is the time difference between zero crossings of i_{of} and i_{sf}. Additionally, the amplitude controller in Fig. 5 uses v_{op} as the feedback signal and changes the amplitude A of perturbation i_{inj} in order to regulate the amplitude of voltage perturbation to a reference, V_{pref}. Design and details of these controllers is discussed in [20]. The control bandwidths of the monitor controllers are designed to be much higher than that of the stability regulator, such that the stability regulator always sees PM_{sys} and $f_{c,sys}$ at its input.

C. Stability Controller Design

In order to design the stability controller of Fig. 4, it is important to understand the plant, which is the transfer function from d_v to PM_{sys}. For the IMLG to have a crossover, one of the admittances from Y_o and Y_{away} must behave capacitive, while the other inductive, around the crossover frequency [20]. Taking a cross-section of the frequency response at the crossover frequency, it can be shown that the interconnection of Y_o and Y_{away} has a dominant second order behavior with certain damping characteristics. For instance, if Y_{ESC} behaves capacitive, the equivalent circuit including DVI is shown in Fig. 6a, where $Y_{away} = 1/sL$, $Y_{ESC} = sC$ and $G_v = g$. The effect of DVI is to increase the conductance value at this frequency, adding more damping in the process. For this cross section, the IMLG is found as

$$\text{IMLG} = \frac{Y_{away}}{Y_o} = \frac{1}{s^2LC + sLg}. \tag{16}$$

The crossover frequency of IMLG in (16) can be found by equating the absolute magnitude to 1, which results in

$$f_{c,sys} = \frac{1}{2\pi}\sqrt{\frac{-Lg^2 + C\sqrt{4 + L^2C^2}}{2LC^2}}. \tag{17}$$

Similarly, phase margin of the IMLG in (16) can be found as

$$PM_{sys} = \arctan\Big(\frac{g}{2\pi f_{c,sys}C}\Big). \tag{18}$$

For some arbitrary values $L = 2.5$ mH and $C = 35$ μF, Fig. 6b shows the behavior of phase margin, PM_{sys}, with respect to conductance g. It is evident from Fig. 6b that the relationship is linear except close to 90°. This is expected in the assumed system of Fig. 6a since the system tends towards a first order system as conductance increases and the phase margin can never exceed 90°. In an actual system, though, Y_{away} and Y_{ESC} will have resistive components, and it is possible to achieve a phase margin of over 90°. To design the controller gains, the cross section parameters may be estimated from continuous monitor measurements, the dc gain may be measured directly using the continuous monitor, or wide-band perturbation may be used to explicitly measure the system admittances and the parameters estimated from there. In this work, the dc gain was estimated from the analytical models of converter admittances, presented in the next section. The plant dynamics from the current reference to the phase margin evaluation output are dominated by the high-Q band-pass filter. In [20], the authors showed that the plant transfer function shows dominant pole behavior with a pole frequency, ω_1, given by

$$\omega_1 = \sqrt{2}w_{inj}\sqrt{1 - \sqrt{1 - \frac{1}{4Q^2}}}, \tag{19}$$

where w_{inj} is the injection frequency as well as the resonance frequency of the band-pass filter. For $Q >> 1$, this expression can be approximated by

$$\omega_1 \approx \frac{w_{inj}}{2Q}\Big|_{Q>>1}. \tag{20}$$

The bandwidth of the stability controller can be designed to be much less than the pole frequency given by (20).

IV. EXPERIMENTAL RESULTS

The stability regulator developed in this paper is evaluated on a lab scale 2 kW dc microgrid. A representative dc microgrid is formed, including converters interfacing power source (VSC), power load (Load) and energy storage (ESC). Well known converter topologies are used with known small-signal models, and direct measurements are used to account for deviations from analytical models. The stability enhancement from the use of DVI is evaluated through models and direct measurements. Phase margin regulation is recorded as the constant power load increases, demonstrating the effectiveness of the stability regulator in enhancing the system stability using the DVI.

A. Hardware Test Setup

The overall block diagram for the hardware test setup is shown in Fig. 7a. All three of the converters are built using the TI GaN devices with integrated gate drivers [27] and controlled using the CMOD A7 FPGAs [21]. All converters are rated for 400 V on the dc bus and 2 kW power. Fig. 7b shows a picture of the actual hardware setup. The converter
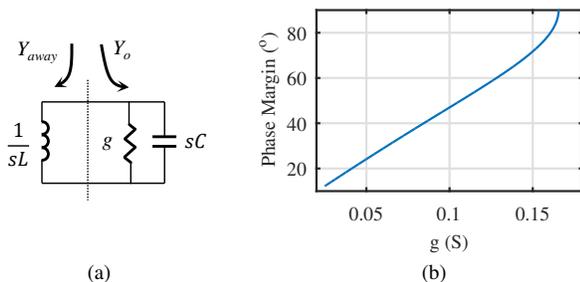

Fig. 6. Behavior of IMLG at the crossover frequency; (a) equivalent circuit, and (b) phase margin characteristics with respect to conductance.
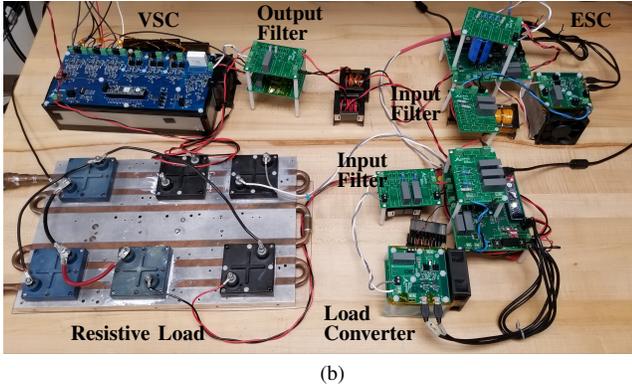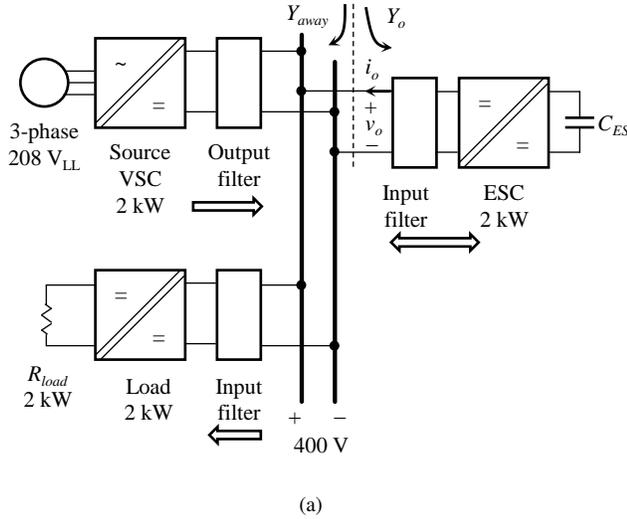
(a)

(b)

Fig. 7. Overall test setup for evaluating the stability regulator; (a) Block diagram, and (b) experimental setup.

TABLE I
PARAMETERS OF THE CONVERTERS IN THE HARDWARE TEST SETUP.

	VSC	Load	ESC
Topology	2-level 3-phase	Buck	Buck/Boost
I/O Voltage	208 V_{LL}/400 V	400 V/340 V	400 V/200 V
P_{rated}	2 kW	2 kW	2 kW
Switching Freq.	100 kHz	100 kW	100 kW
Main Inductor	630 μH	215 μH	300 μH
I/O filter (L, C, Rd, Cd)	N/A, 2.5 μF, 6 Ω, 3.3 μF	300 μH, 3.5 μF, 8 Ω, 6.6 μF	300 μH, 3.5 μF, 8 Ω, 6.6 μF
G_{ci} Bandwidth	150 Hz	10 kHz	10 kHz
G_{cv} Bandwidth	30 Hz	1 kHz	10 Hz
G_v Bandwidth	N/A	N/A	1 Hz

topologies, passive components and control parameters are summarized in Table I.

The source converter shown in Fig. 7 is a two-level three-phase voltage source converter (VSC). Its controller board senses the three line currents, line-to-neutral voltages, the dc output current and the dc link voltage. A control architecture similar to [28] is employed, where a dq-domain current controller regulates the line currents and an outer loop regulates the dc bus voltage. On the dc bus, a capacitive output filter is employed along with an RC-branch similar to [13], to damp

the resonance between the phase reactors and the dc output capacitor. With the control architecture described here, the analytical model for the source converter output admittance looking into the dc terminal, Y_{source}, is derived as

$$Y_{source} = Y_{dc} + Y_s, \qquad (21)$$

where Y_{dc} is the admittance of the dc output filter including the dc bus capacitor and the RC-branch, and Y_s is given by [28]

$$Y_s = \frac{3}{2V_{dc}^2} \left\{ \frac{(V_1 + sLI_1)[V_1 + V_{dc}^2 G_{ci} G_{cv}]}{sL + V_{dc} G_{ci}} - V_1 I_1 \right\}, \qquad (22)$$

where G_{ci} is the current compensator, G_{cv} is the voltage compensator, and the remaining parameters are adopted from [28]. The admittance model of (21) and (22) is derived based on the assumption that the 3-phase 208 V_{LL} power source is an ideal voltage source, thereby ignoring the dynamics of the phase-locked loop and the 3-phase power source [28].

The load converter is a traditional synchronous buck converter with an LC-filter at the input and an LC-filter at the output, both augmented with an RC-branch to damp the resonances of the LC filters. The load converter has a fast inner control loop regulating the buck-inductor current, and an output loop regulating the load resistor voltage. The input admittance, Y_{Load}, of the buck converter, with its control loops and filters, is given by

$$Y_{Load} = \frac{(Y_{conv} + Y_{Cin})}{1 + Z_{Lin}(Y_{conv} + Y_{Cin})}, \qquad (23)$$

where Z_{Lin} is the impedance of the input inductor, Y_{Cin} is the admittance of the input capacitor in parallel with the RC-branch, and Y_{conv} is given by

$$Y_{conv} = \frac{D[D - G_{ci}G_{cv}I_L Z_{RCload} - G_{ci}I_L]}{Z_L + Z_{RCload} + G_{ci}G_{cv}V_{dc}Z_{RCload} + G_{ci}V_{dc}}, \qquad (24)$$

where Z_L is the impedance of the buck-inductor, Z_{RCload} is the impedance of the load resistance in parallel with output capacitor and RC-branch, G_{ci} is the current compensator, G_{cv} is the voltage compensator, V_{dc} is the dc bus voltage and I_L is the current of the load resistor.

The Energy-Storage Converter (ESC) has the same topology, control architecture, and filters, as the load converter. Instead of a resistive load, the ESC has a bulk capacitance of 0.4 mF serving as the energy storage element. The current control bandwidth of the ESC is kept high while the voltage control bandwidth kept very low (10 Hz), so that the ESC appears as a capacitive constant-current load on the dc bus. The analytical admittance model of the ESC, Y_{ESC} is exactly the same as that of the load converter, with only the bulk capacitor replacing the load resistor.

In this work, the source VSC control bandwidth has been kept low by design to emulate the source behavior in typical dc microgrids, where MW scale power sources use devices that switch only up to a few kHz, limiting the achievable control bandwidth. The control bandwidth of G_v was chosen to be 1 Hz based on the estimated crossover from models of around 400 to 600 Hz and a Q of 16, giving an estimated w_1 between 12.5 to 18.75 Hz according to (20).

B. Stability Regulator Performance

The performance of the stability regulator is evaluated by using the hardware setup shown in Fig. 7 and the continuous monitor shown in Fig. 5. At startup, the dc bus voltage is ramped up to 400 V with the VSC operating in closed loop. The ESC is then enabled and the voltage of the energy storage capacitor ramped up to 200 V. Next, the continuous injection and the continuous monitor controllers are enabled with the designed parameters. The FPGA controller of the ESC sends its continuous monitor outputs, $f_{c,sys}$ and PM_{sys} to the PC at 4 Hz rate using UART communication. The data is logged along with the timestamp for alignment with the data from other converters.

With the continuous monitor running, the load converter is enabled and load power ramped up slowly from 0 W to 1900 W and then back down to 0 W. The load converter sends its power reference to the PC for logging at 4 Hz rate with the timestamp using UART communication. Two test runs are performed. In the first run, the stability regulator is not enabled and the stability parameters, PM_{sys} and $f_{c,sys}$ are recorded as the load power ramps up to 1900 W and back down to 0 W. In the second test, the stability regulator is enabled with DVI and a reference of $100°$, and then the same load profile is run. For the second test, the output of stability regulator, d_v, is also recorded. Once the test is complete, the data from load converter and the ESC are aligned using the timestamp, and the variation of d_v, $f_{c,sys}$ and PM_{sys} with respect to the load power is shown in Fig. 8.

Fig. 8a shows that without the DVI enabled, as the load power goes from 0 W to 1.9 kW, $f_{c,sys}$ goes from 615 Hz to 540 Hz, while PM_{sys} goes from $80°$ to $33°$. When the DVI and stability regulation is enabled, Fig. 8b shows that PM_{sys} jumps from $80°$ to $100°$ and is regulated there, while $f_{c,sys}$ goes to 575 Hz and d_v goes to 0.022 S. Once the system phase margin is regulated, as the load power increases, PM_{sys} stays regulated at $100°$, while d_v increases to compensate for additional damping requirement. As d_v increases to 0.073 S and re-shapes the ESC admittance, Y_o, $f_{c,sys}$ also shifts further down to 415 Hz. To see the effect of DVI on load transients, a load power step response from 1.4 kW to 1.8 kW is shown in Fig. 9 with, and without, the DVI tuned at $d_v = 0.073$ S at 415 Hz.

To validate the performance of the stability regulator, two methods are used: analytical model prediction and direct impedance measurement using psuedo-random binary sequence (PRBS) injection [29]. For analytical model prediction, the admittance models presented in section IV-A are evaluated at load power levels from 200 W to 1800 W along with the DVI evaluated with the test output values. The resulting Y_o and Y_{away} are plot together to find the crossover frequency and phase margin. For direct measurement, a 12-bit PRBS signal of length 4095 is injected at 25 kHz rate into the current reference of the ESC at nine operating points with load power ranging from 200 W to 1800 W. The current injected into the dc bus (i.e. the current driven into the sum of Y_{away} and Y_{Load}) is recorded along with the dc bus voltage. Fast Fourier Transform (FFT) is performed on the injected current and
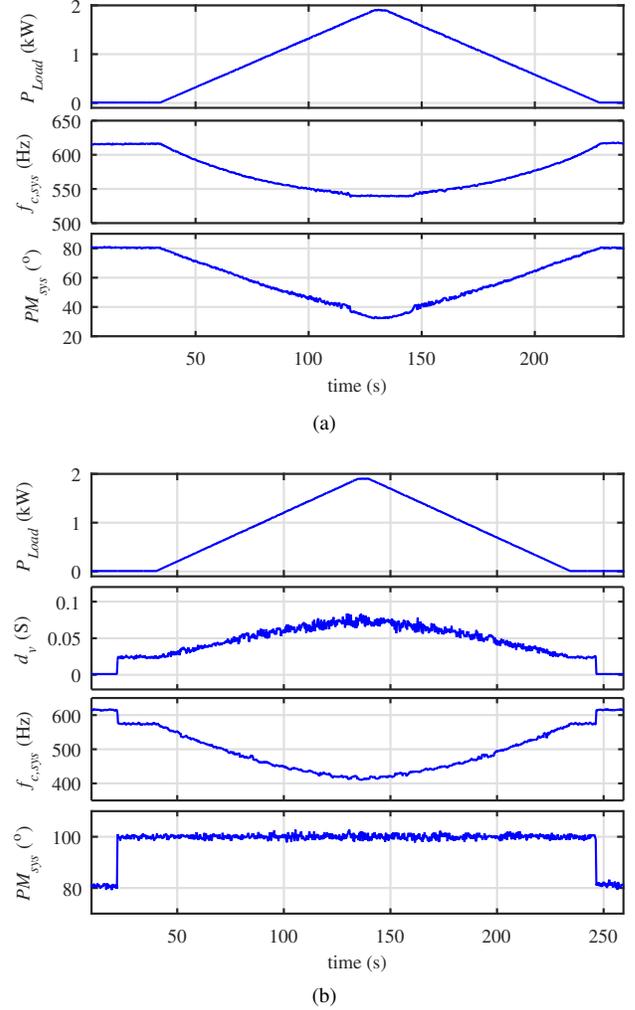

(a)

(b)

Fig. 8. Performance of the stability regulator over the load profile; (a) without DVI, and (b) with DVI and stability regulator.
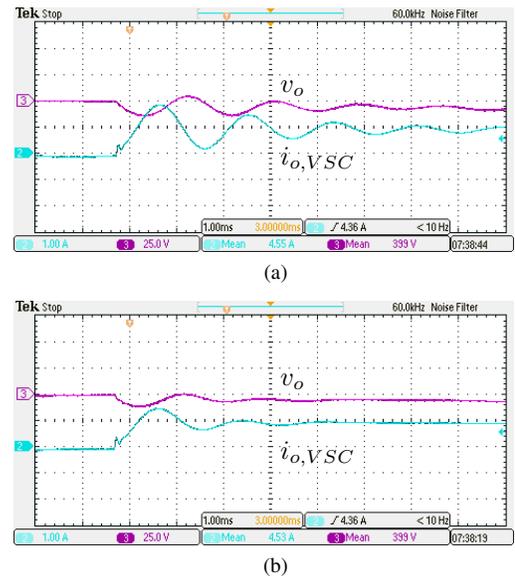

(a)

(b)

Fig. 9. Load transient from 1.4 kW to 1.8 kW; (a) without DVI, and (b) with DVI.
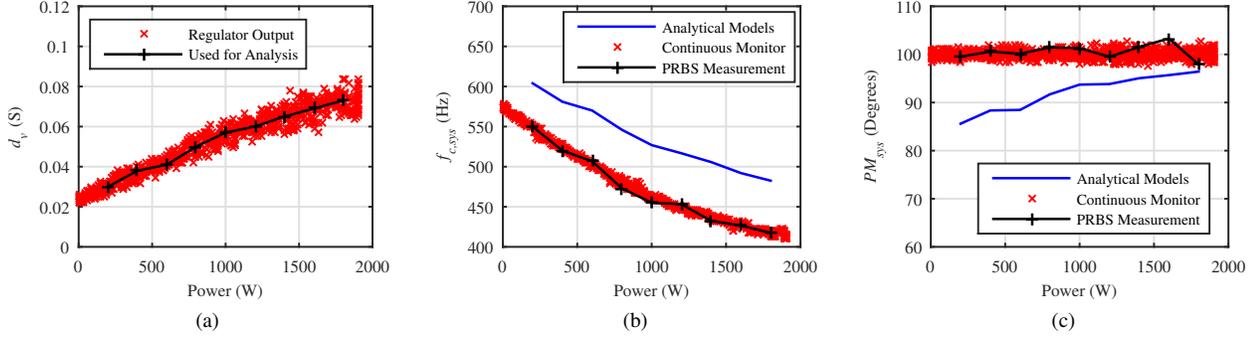
Fig. 10. Performance of the stability regulator over the load range; (a) d_v, (b) $f_{c,sys}$, and (c) PM_{sys}.

response voltage to find the frequency spectra. Then the ratio of the current spectrum to the voltage spectrum is computed to calculate the frequency spectrum of the combined admittance Y_{away}. This measured admittance is used along with the analytical model of $Y_o = Y_{ESC} + G_v$ to determine the PRBS-based stability results. The results from analytical models, PRBS measurement and continuous monitor and regulator are shown in Fig. 10.

C. Evaluation of Continuous Monitor Results

The trends shown in Fig. 10 for d_v, $f_{c,sys}$ and PM_{sys} are expected. At higher power, the negative incremental resistance behavior of the load converter becomes more dominant and requires more involvement from the DVI to achieve the desired damping. The monitor outputs, PM_{sys} and $f_{c,sys}$ match well with the PRBS-based direct measurement; however, neither the monitor output nor direct measurement result matches well with the analytical prediction. To understand this, the analytical model and direct measurements of Y_{away} at load power of 400 W are shown in Fig. 11 along with the analytical model of Y_o (with DVI) and Y_{ESC} (without DVI).

In Fig. 11, the analytical model response of Y_{away} is shown with a solid red curve, while measured Y_{away} is shown with blue cross, and the analytical model responses of Y_o and Y_{ESC} are shown with black dashed lines and magenta dash-dot lines respectively. Fig. 11 reveals that the magnitude response of the measured Y_{away} is shifted slightly to the left at lower frequencies and the phase is also closer to zero compared to the analytical model. This is expected since the analytical model assumes that the 208 V_{LL} three-phase source shown in Fig. 7a is a zero impedance voltage source, whereas the actual hardware of Fig. 7b uses a lab-scale power supply which has finite non-zero output impedance. This source output impedance affects Y_{away} at lower frequencies within the control bandwidths of the power source but not at higher frequencies where the admittance is dominated by the passive components of the converters. Furthermore, the analytical model does not account for losses in the converters, which add damping and lower the phase of the impedance response. The analytical model also assumes the passive components to be linear over the frequency range, which is rarely true for real components. For instance, the phase inductors for the VSC
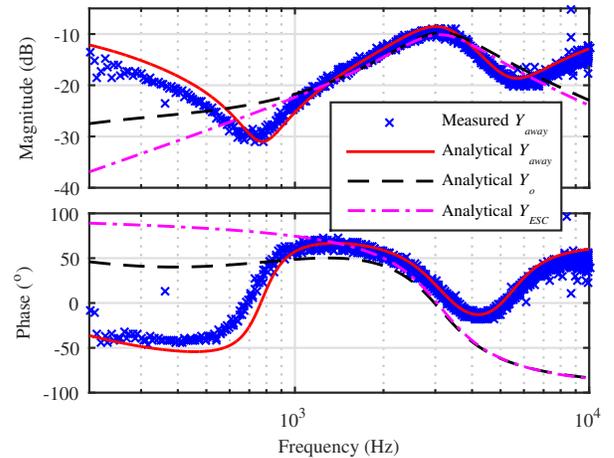

Fig. 11. Comparison of analytical models and PRBS measurement.

in Fig. 7b are built using single strand AWG-16 laminated wire which resulted in 90 mΩ resistance at 60 Hz but the ac resistance increases rapidly with frequency, giving an ac resistance of 16 Ω at 1 kHz. Thus, while it is easy to accurately model small systems (less than 100 W) with highly controlled passive components, it is nearly impossible to capture the dynamics of a medium to large scale power system using just analytical models. In such cases, direct measurement is used as an alternative method to find the impedance or admittance response that accounts for modeling uncertainties and avoids any simplifying assumptions.

V. CONCLUSION

This paper proposes a novel method for explicitly regulating the stability of a dc microgrid by using a small reactive power to add just enough damping at target frequencies as needed to maintain desired system stability margin. The stability regulation uses a dynamic virtual immittance concept whereby the admittance or impedance of the regulating converter is augmented by a second order virtual filter that is continuously tuned at the system impedance minor-loop-gain crossover frequency. The proposed stability regulator may be used with any system stability monitor designed to provide measurement

of system IMLG crossover frequency and phase margin, be it continuous as used in this work, or periodic such as wideband measurement. The stability regulator and DVI can be implemented onto any converter in the system with a high control bandwidth and ability to inject perturbation in the dc microgrid, or a dedicated converter may be added into the dc microgrid with capacitive or battery energy storage and a fraction of the system power rating. The proposed stability regulator is implemented onto an FPGA along with the continuous monitor functions and complete functionality of the energy storage converter including UART communication, protection, ADCs, PWM and current and voltage controllers, demonstrating low cost of implementation. Guidelines are provided for designing the gains and bandwidth of the stability regulator. Hardware results on a lab scale 2 kW dc microgrid system, which are validated through analytical models and direct measurements, demonstrate the effectiveness of the proposed stability regulator.

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CHAPTER 7

Conclusion

Stability of dc microgrid systems such as those found in electric ships, more-electric aircraft and dc fast charging stations has been a topic of renewed interest. Designing such systems require deep understanding of dynamic behavior of dc microgrids with various types of sources and loads interfacing together. As the size and power level of these systems increase, it becomes nearly impossible to capture all non-linearities and parasitic elements in the system modeling. To account for modeling uncertainties, and for systems where prior knowledge of components is not available, online measurement of system dynamics has been shown to be effective. However, methods proposed in literature that can identify system stability online, and provide stability enhancement through control, have a high implementation cost and in most cases require additional hardware. To overcome these challenges, and to provide additional stability support for a dc microgrid, this thesis proposes a new stability analysis method, a novel online stability monitoring method, and a novel explicit stability controller for a dc microgrid system.

The novel method for analyzing stability of dc microgrid, proposed in this thesis, is based on nodal analysis. It was shown through analysis and hardware results that stability of a dc microgrid can be evaluated at the terminal of any of the parallel-connected converters, regardless of the power flow configurations. Furthermore, it was shown that the proposed method provides necessary and sufficient conditions for system stability. The proposed nodal impedance-based stability analysis can be used to a great advantage by selecting a source converter or an energy storage converter as the terminal of choice for analysis and using it to measure the combined impedance of the rest of the system. The measured impedance would account for parameter variations, capture the effects of cable impedances and contact impedances, and adapt to the dynamically changing system. The measured impedance would then be used along with the dc bus interfacing impedance of the measuring

converter to perform the online stability analysis. If the converter performing the online impedance measurement is intended to be used to enhance stability, it would require a high control bandwidth, which can be a design consideration for the converter performing stability analysis. Another application of the proposed method would be to analyze if an existing system would remain stable after the addition of a new converter in the system. The impedance of the system looking into the dc bus where the new converter is to be inserted would be measured or evaluated. This would be used along with the dc bus interfacing impedance of the new converter to analyze the stability. The proposed nodal impedance-based stability analysis method can be further utilized in providing active damping where needed. The analysis performed at the terminal of a converter, for example, could be used to determine the stability margin which indicates the amount of damping in the system. The high-bandwidth controller of the converter could then be used to provide active damping in the system by targeting the critical frequencies identified in the minor loop gain.

The Nodal Stability Analysis proposed in this work applies to a node in the dc microgrid, with multiple parallel-connected sources, loads and energy storage. As the size of the dc microgrid increases, cable impedance becomes significant, in which case the definition of a 'node' in the dc microgrid needs to be broadened. For a large-scale dc microgrid, a node would be defined as the collection of all the loads and sources in the proximity of the converter interface chosen for stability analysis. A converter is considered to be in proximity if the combination of the converter input impedance and the impedance of the cable connecting the converter to the interface for stability analysis, is dominated by the converter impedance in the frequency range of interest (typically 10's of Hz to a few kHz). A long dc cable with significant impedance would then divide the dc microgrid into two nodes, one on either end of the cable. In this case, stability analysis would need to be performed at both ends of the long cable, where the total impedance of the sources, loads and cable impedance at one end of the cable are lumped into the cable impedance as seen from the other end of the cable. This scaling of the analysis for larger dc microgrids also applies directly to the other two contributions of the thesis.

This thesis utilizes the proposed nodal stability analysis to develop a novel method for monitoring the stability of a dc microgrid, including the stability margin and the critical frequency. The proposed monitor injects a small perturbation into the system for monitoring stability, which does not affect normal operation of the system. Detailed modeling of the continuous monitor dynamics are presented, and a comparison of two control strategies is carried out for the design of the monitor. One control strategy using the difference feedback and linear output has low complexity and requires fewer resources to implement; however, its controller may suffer from variation of the operating points. It should be considered at design time whether the controller will be able to handle those variations. An alternative control strategy using logarithm feedback and logarithm output is also presented in this paper. It is shown that using logarithms results in controllers that do not suffer from operating point variations. The use of logarithms and exponential functions, however, comes with higher resource usage for implementation, and may require complex iterative algorithms for implementation in a fixed-point processor such as an FPGA. The analytical development presented in this thesis serves as a tool for the designer to pick a control strategy based on a compromise between implementation cost and design requirement. The proposed continuous monitor is implemented on the energy storage interfacing converter in a 2 kW lab scale dc microgrid. Its performance is evaluated by comparing the results to analytical model predictions and direct measurements. It is highlighted that, while analytical models are useful for designing the monitor, it cannot be relied upon for accurately capturing the damping of a real system and predicting stability as direct measurement can. The results show that the proposed monitor tracks stability in good agreement with direct measurement. The proposed method can be added onto any existing converter in the dc microgrid as an auxiliary function. If there is no access to the control of the converters already in the system, another converter may be added with a fraction of the power rating and with capacitive energy storage to perform the monitoring task. In contrast to the existing wide-band identification methods, the proposed method outputs the stability measurement as a continuous signal, which opens up new possibilities of utilizing this for improving the

stability of the dc migrogrid being monitored.

Utilizing the continuous nature of the stability monitor proposed in this thesis, a novel method is developed for explicitly regulating the stability of a dc microgrid by emulating a dynamic virtual immittance at the terminal of the converter performing the stability monitoring function. The proposed method uses a small reactive power of the converter to add just enough damping at target frequencies as needed to maintain desired system stability margin. The stability regulation uses a dynamic virtual immittance concept whereby the admittance or impedance of the regulating converter is augmented by a second order virtual filter that is continuously tuned at the system impedance minor-loop-gain crossover frequency. The proposed stability regulator may be used with any system stability monitor designed to provide measurement of system IMLG crossover frequency and phase margin, either continuous as used in this work or periodic such as wide-band measurement. The stability regulator and DVI can be implemented onto any converter in the system with a high control bandwidth and ability to inject perturbation in the dc microgrid, or a dedicated converter may be added into the dc microgrid with capacitive or battery energy storage and a small fraction of the system power rating. The proposed stability regulator is implemented in an FPGA along with the continuous monitor functions and complete functionalities of the energy storage converter including UART communication, protection, ADCs, PWM, and current and voltage controllers, demonstrating low cost of implementation. Guidelines are provided for designing the gains and bandwidth of the stability regulator. Hardware results on a lab scale 2 kW dc microgrid system, which are validated through analytical models and direct measurements, demonstrate the effectiveness of the proposed stability regulator.

The work presented in this thesis opens up a lot of opportunities for future research in the stability monitoring and enhancement of dc and ac microgrids. The Nodal Stability Analysis has the potential to be applied to ac microgrids as well as dc microgrids. A future researcher could investigate its applicability and challenges in extending this to ac microgrids. The continuous stability monitoring was implemented for dc microgrids by

perturbing the dc current and measuring the response voltage. It could be investigated for ac microgrids by perturbing the positive and negative sequence networks with orthogonal single frequency perturbations, and measuring the response voltages, thereby measuring both positive and negative sequence IMLG of the ac microgrid. We have shown continuous monitor application in an energy storage interfacing converter; however, the continuous monitor can be implemented in any of the converters in the system. A future researcher could explore continuous monitoring implemented at the source and load converter and investigate the pros and cons of implementing the monitor at these converter interfaces. For larger dc microgrids in which cable impedance creates an impedance network instead of a common dc bus, a future researcher could investigate the feasibility of having a continuous monitor at each node in the dc microgrid, where a node is defined based on the proximity of the converters.

A lot of the efforts towards continuous monitoring research could be extended to include stability regulation. For instance, the DVI may be implemented at the source or the load converter within their control bandwidths. A future researcher could explore implementing the stability regulator at a high bandwidth load converter interface and adding damping right at the constant power load. Another extension could investigate multiple stabilizers in the dc microgrid system in case the dc microgrid is large enough to have significant cable impedances. Furthermore, the stability regulation and DVI concept could be extended to the ac microgrid, in a similar manner to the continuous monitor.

CURRICULUM VITAE

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Published Journal Articles

- R. Hassan, H. Wang and R. Zane,"*A Continuous Stability Margin Monitor for DC Microgrids*," *in submission.*

- R. Hassan, H. Wang and R. Zane,"*Active Stability Control of DC Microgrids using Dynamic Virtual Immittance*," *in submission.*

Published Conference Papers

- R. Hassan, H. Wang, M. M. Ur Rehman, B. Riar and R. Zane, "Nodal Impedance-Based Stability Analysis of Dc Nanogrids" *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Padua, Italy, 2018, pp. 1-7.

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