Space Dynamics LABORATORY
Utah State University Research Foundation

Distributed Electrical Power Systems in CubeSat Applications

Small Satellite Conference
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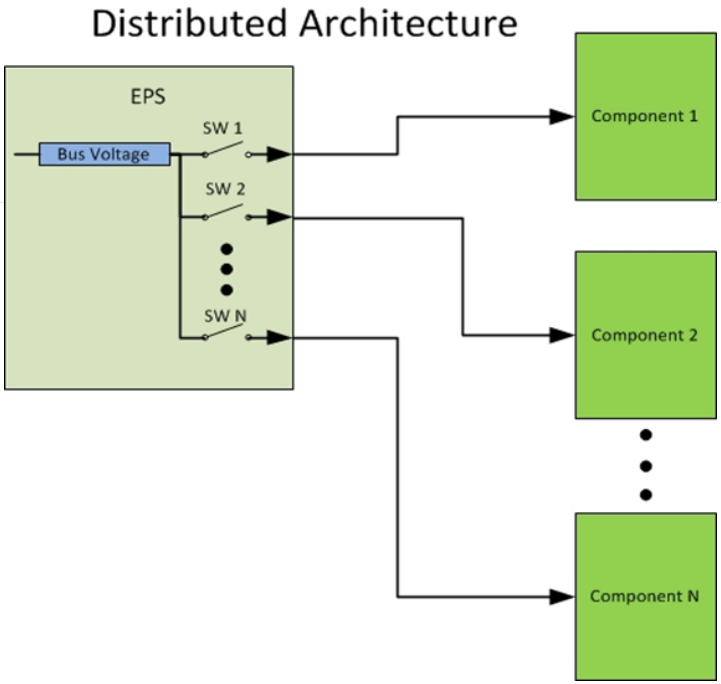
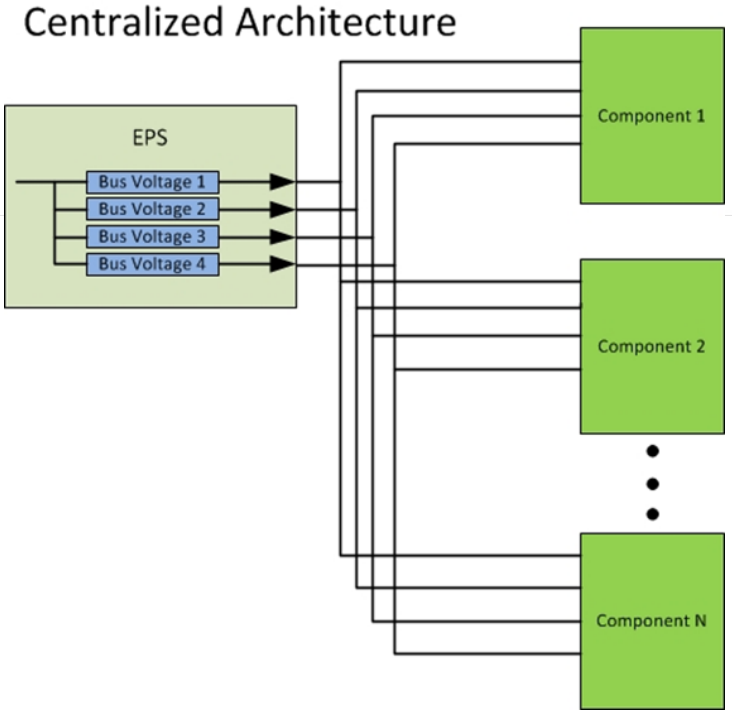
Can a Distributed Architecture work in CubeSat or Nanosat Application?

Traditional Large Sat EPS



Traditional CubeSat EPS



- Can you build an EPS with the following characteristics?
  - Very Power Efficient
  - Reusable for multiple missions (Non-custom)
  - Small and compact

Research Focus Activities

- EPS Survey
  - Determine current state of the art
- Point-of-Load DC-DC Converters
  - Device availability
  - Test Board
    - Board real estate and layout impacts
    - Actual efficiencies
    - Ease of implementation
- Analysis
  - Efficiency comparison for both distributive and centralized designs

EPS Survey

- Total of 52 CubeSat EPS designs reviewed
- Primary Goal:
  - Determine how many were centralized
  - Determine how many were distributed
- Secondary Goal:
  - Peak power tracking or direct energy transfer
  - Number of buses and bus voltage used in designs
- Lastly: Battery types, capacity, voltages, solar cells, etc.

Survey Results

EPS Architecture Type	Quantity
Centralized	20
Distributed	5

- Data available for 25 designs
  - Twenty designs conform to the classical definition of centralized
  - Five do not fit the classic centralized description and are, therefore, classed as distributed.
  - Only one of the five distributes a single bus
  - None of the EPS designs distributes a single unregulated battery bus

Survey Results Summary

EPS Architecture Type	Quantity
Direct Energy Transfer	13
Peak Power Tracking	15
Other	1

Number of Buses	Quantity
One Bus	3
Two Buses	2
Three Buses	10
Four Buses	4
Five Buses	1
6 Buses	2

Common Regulated Bus Voltages	Quantity
3 Volt Regulated	2
3.3 Volt Regulated	13
3.6 Volt Regulated	1
5 Volt Regulated	17
-5 Volt Regulated	2
6 Volt Regulated	3
-6 Volt Regulated	1
7.4 Volt Regulated	1
8 Volt Regulated	1
12 Volt Regulated	1

Common Battery Bus Voltages	Quantity
4.1 Volt Battery	5
8.3 Volt Battery	6
12.3 Volt Battery	2

Centralized / Peak Power Tracking / 3 Buses / 3.3V Reg, 5V Reg, and 8.3V Battery

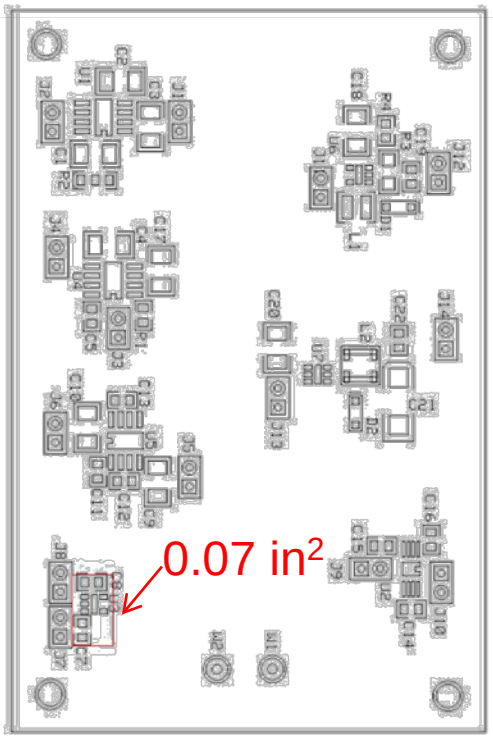
Point-of-Load (POL) DC-DC Converter

- Key to distributed architecture
- Explosion of commercial DC-DC converters over the last decade
- Two main types: inductor and charge pump
- A POL converter test board was assembled to:
  - Develop a working knowledge of POL converters
  - Measure “as designed” efficiencies
  - Get a feel for board space requirements

POL Converters &Test Board

- Footprints are very small
- Monolithic Switching Element
- Capacitor and Inductor will typically be largest components
- Ceramic caps are ideal for this class of converter and help reduce size

Device	Type	Function	Efficiency Percent	Ripple (mV P-P)
MAX1680	Charge Pump	Doubler	96%	170
MAX1044	Charge Pump	Inverter	93%	28
LTC1503	Charge Pump	LDO Replacement	78%	160
TPS60400	Charge Pump	Inverter	93%	14
MAX1595	Charge Pump	Buck-Boost	66%	330
LT1615-1	Inductor	Boost	87%	NA
MAX1837	Inductor	Buck	87%	147

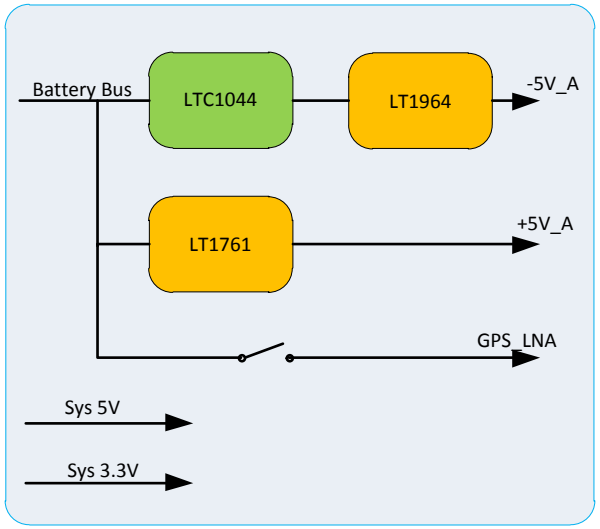


- Unregulated charge pumps are very efficient.
  - Small input voltage range (<6V)
- Tremendous selection of inductor based converters.
  - Wide input / output / power ranges

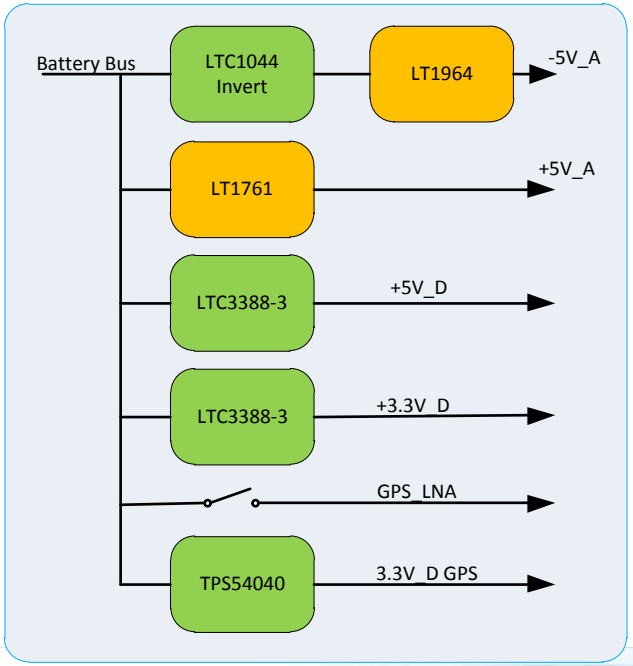
Analysis & Distributed Design

- DICE EPS was used as the analysis baseline.
- Equivalent distributed design was created
  - Battery bus is distributed to each card
  - Point-of-load converters are implemented on each card

Centralized Design

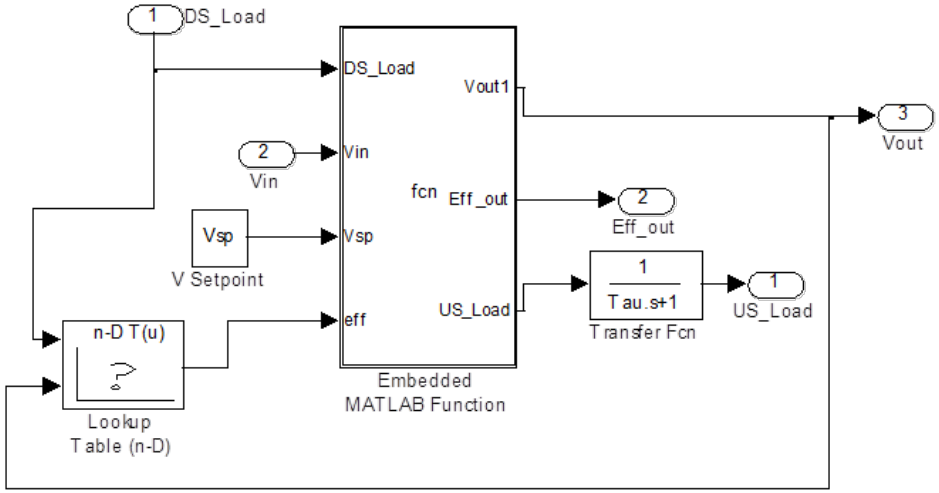


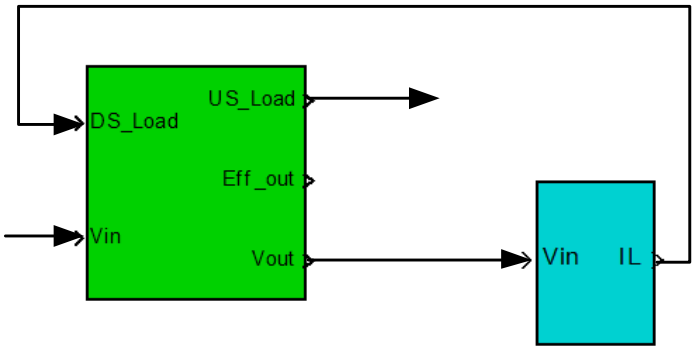
Distributed Design



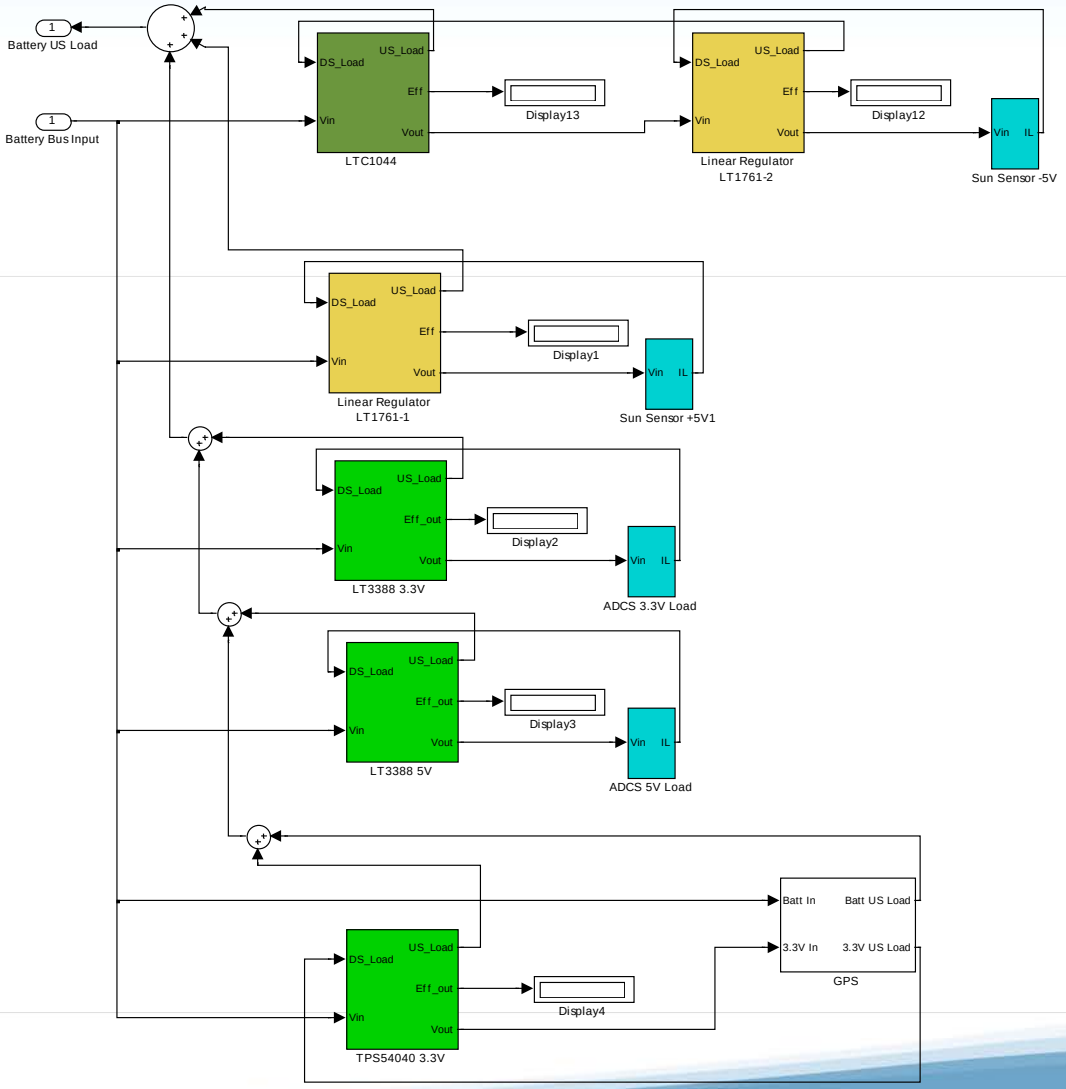
Analysis Tool

- A SimuLink model is created for each converter in both the distributed and the centralized designs.
- Actual power loads, based on DICE lab measurements, are used in the analysis

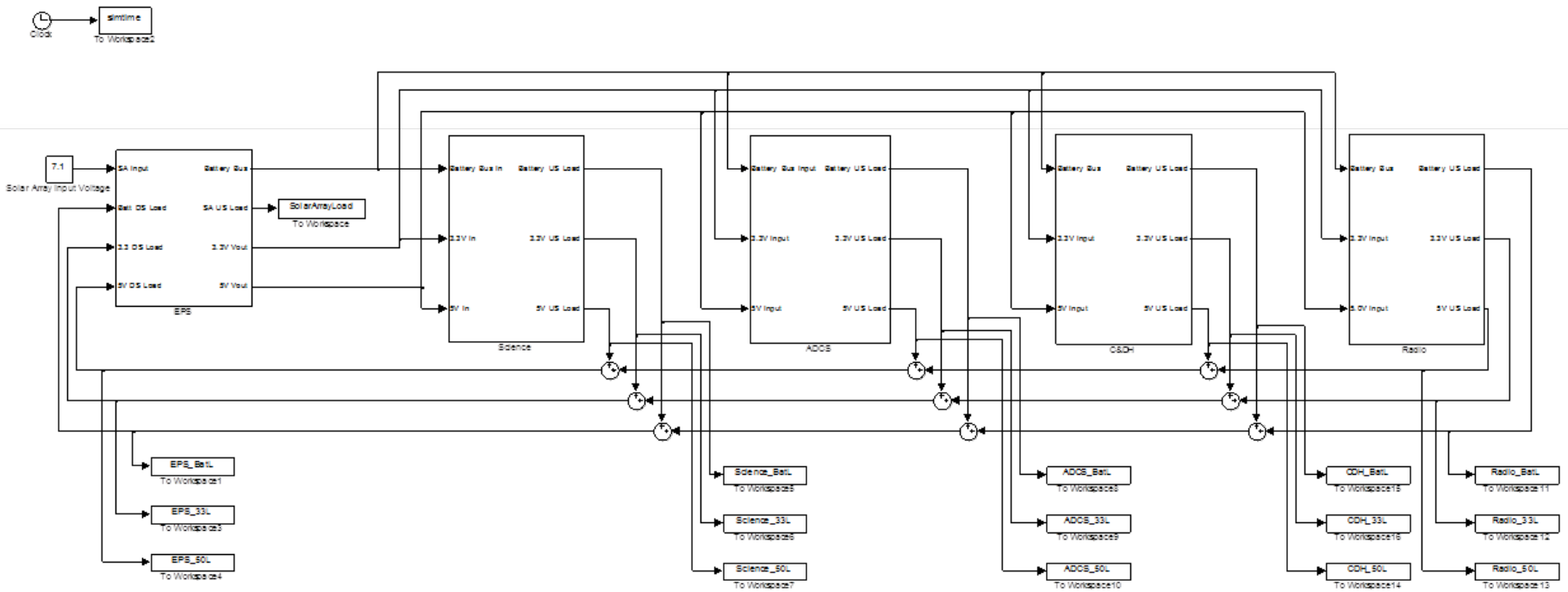




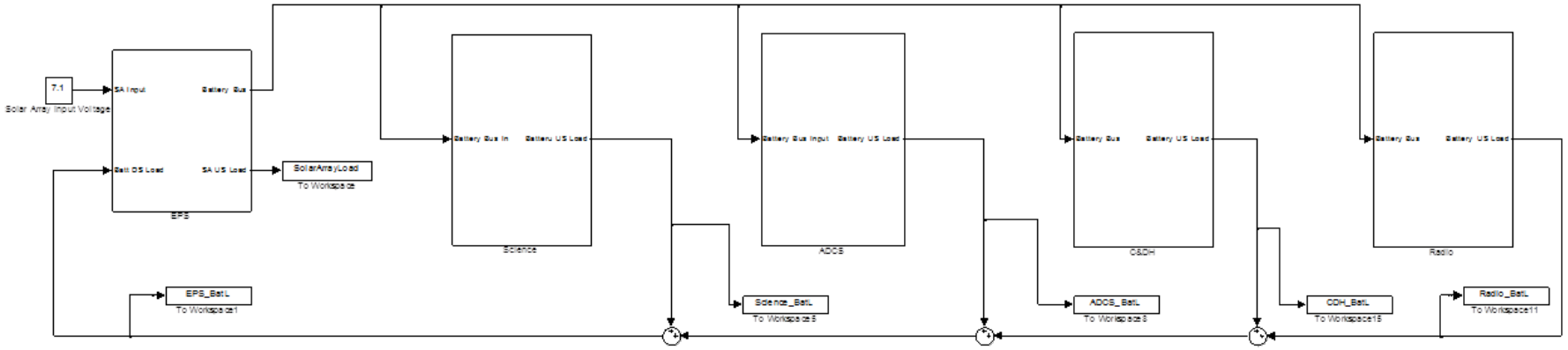
Simulink Model: ADCS Board



Centralized DICE Analysis: System Level



Distributed DICE Analysis: System Level



Analysis Results

Centralized Analysis Results

	Fixed Load (W)	Case 1 Load (W)	Case 2 Load (W)	Case 3 Load (W)	Case 4 Load (W)	Case 5 Load (W)
C&DH	0.065	0.065	0.065	0.065	0.065	0.065
ADCS	0.158	0.198	0.198	0.198	0.198	0.198
GPS	1.022	OFF	1.022	OFF	OFF	OFF
Comm Tx	10.271	OFF	OFF	OFF	10.271	10.271
Comm Rx	0.117	0.117	0.117	0.117	0.117	0.117
Science Digital	0.12	0.193	0.193	0.193	0.193	0.193
Science Analog	0.175	OFF	OFF	0.338	OFF	0.338
Total System Load	12.045	0.573	1.595	0.911	10.844	11.182
Solar Array Load PWR		2.961	4.277	3.337	14.42	14.8248

BCR Efficiency	Pct.	83%	84%	84%	84%	84%
3.3V Efficiency	Pct.	87%	88%	87%	88%	88%
5.0V Efficiency	Pct.	15%	15%	15%	88%	88%

Distributed Analysis Results

	Fixed Load (W)	Case 1 Load (W)	Case 2 Load (W)	Case 3 Load (W)	Case 4 Load (W)	Case 5 Load (W)
C&DH	0.065	0.068	0.068	0.068	0.068	0.068
ADCS	0.158	0.207	0.207	0.207	0.207	0.207
GPS	1.022	OFF	1.099	OFF	OFF	OFF
Comm Tx	10.271	OFF	OFF	OFF	10.323	10.323
Comm Rx	0.117	0.125	0.125	0.125	0.125	0.125
Science Digital	0.12	0.154	0.154	0.154	0.154	0.154
Science Analog	0.175	OFF	OFF	0.252	OFF	0.252
Total System Load	12.045	0.554	1.653	0.806	10.877	11.129
Solar Array Load PWR		1.984	3.124	2.188	14.12	14.422

BCR Efficiency	Pct.	83%	84%	84%	84%	84%

Fixed loads are identical

Cases represent different power configurations

Distributed design has overall best performance

Analysis Results Summary

- Distributed design has better efficiency performance
  - We expect higher local loads for the distributed design
    - Higher loads on every card except for the science board
      - Indicates poor converter optimization on the science board
  - EPS 3.3 / 5 volt regulators are not operating at peak efficiencies
    - They are optimized for higher loads
    - Manufacture stated efficiencies are based on the peak loads and are seldom if ever reached

Conclusions

- Distributed EPS Architecture
  - Flexible
  - High degree of utility / re-use
  - Efficiency is equal to, or greater than an optimized centralized design for switched load designs
- Small, efficient point-of-load converters enable single bus distributed architectures
  - Large selection in the commercial market
  - POL regulation requires more board space at the load
    - Monolithic devices eliminate the pass element
    - Charge pumps eliminate the inductor
    - Use ceramic caps whenever possible (low ESR, small size)
  - POL regulation allows for highly efficient optimization at the load

A single bus, distributed architecture is a highly efficient design for CubeSats and NanoSats and provides a high degree of design re-use for a standalone EPS