Simulation-Based Testing of Embedded Attitude Control Algorithms of an FPGA based Micro Satellite

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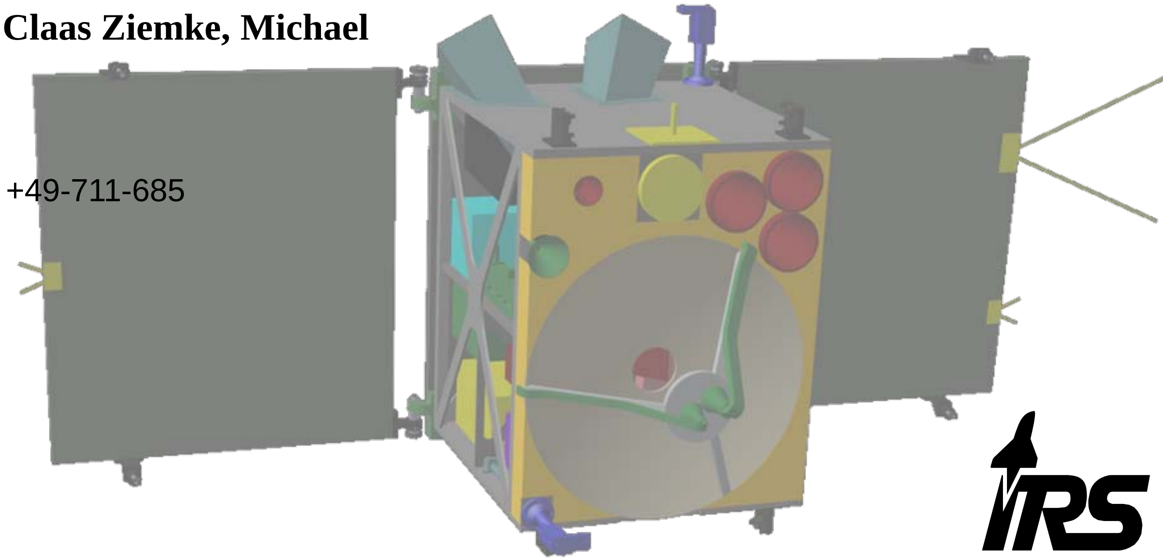


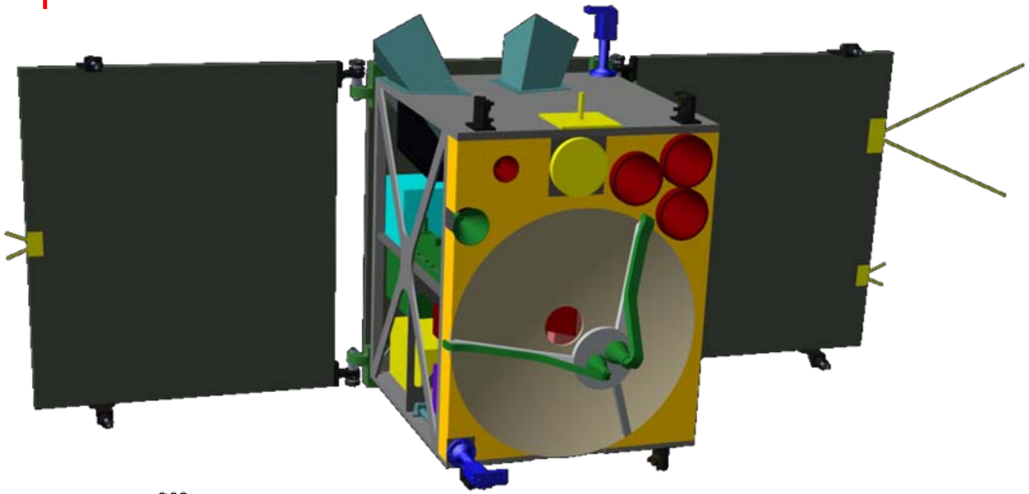
Small Satellite Conference,

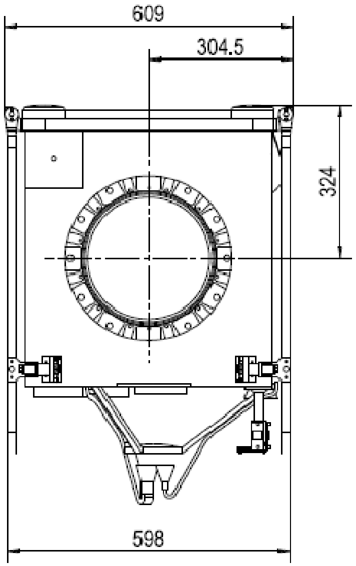
August 10-13, 2009

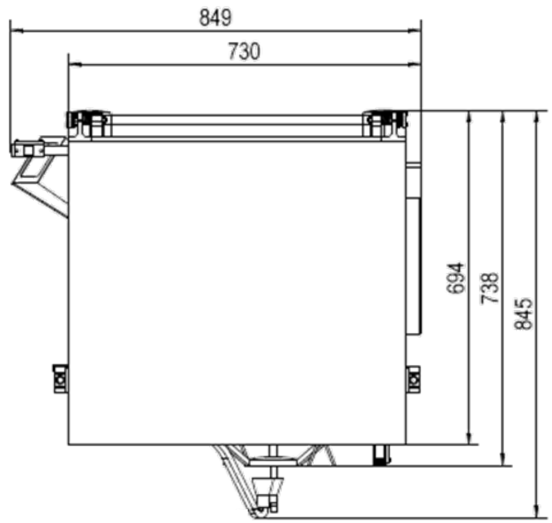
Overview

- Introduction
- OBC Hardware Configuration
- Implementation of ACS Algorithms
- Simulation Environment
- Results
- Conclusions

Mission Facts







Polar, sun-synchronous orbit, 500-900 km
Nodal time passage 9:30-11:00h LTAN
3-axis stabilized
Mass ~120 kg
Design lifetime: 2 years

TM&TC: VHF, UHF, S-band
Ka-band (Experimental)

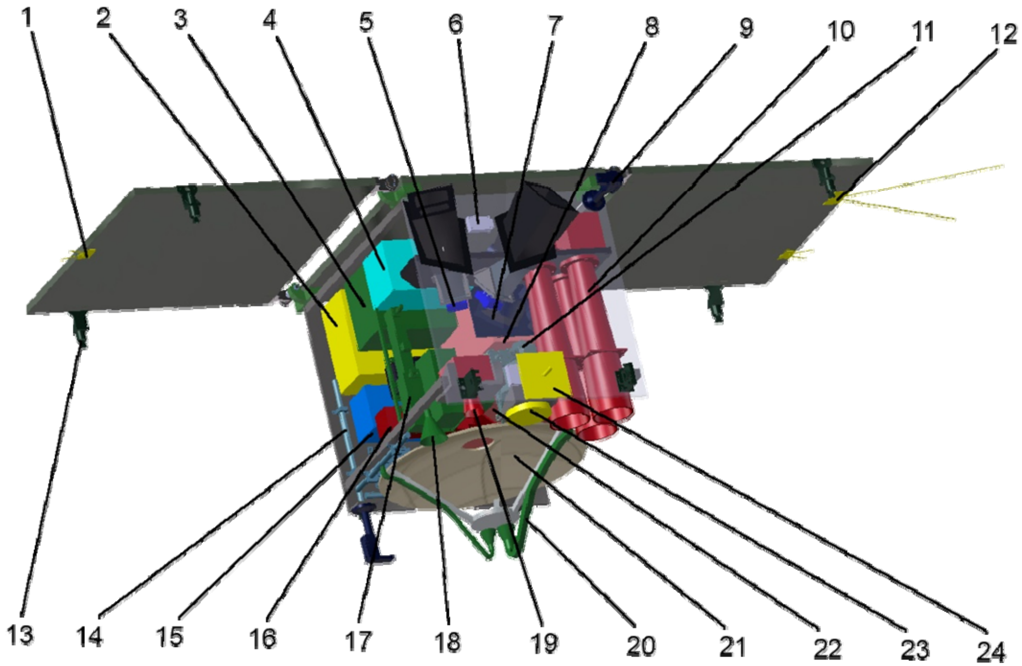
Down-link: 2.2 GHz / 20 GHz
Up-link: 2.0 GHz / 30 GHz

Solar panels: GaAs cells, 0.9 m^2, 200 W
Peak power consumption: 300 W

Quad self-controlling FPGA architecture based on Xilinx Vertex II with
4 million system gates, up to 200 MHz clock,
256 MB RAM, 1 GB Ext. Flash
(Re-)loadable FPGA/OBC

Launch: compatible with PSLV, 2012

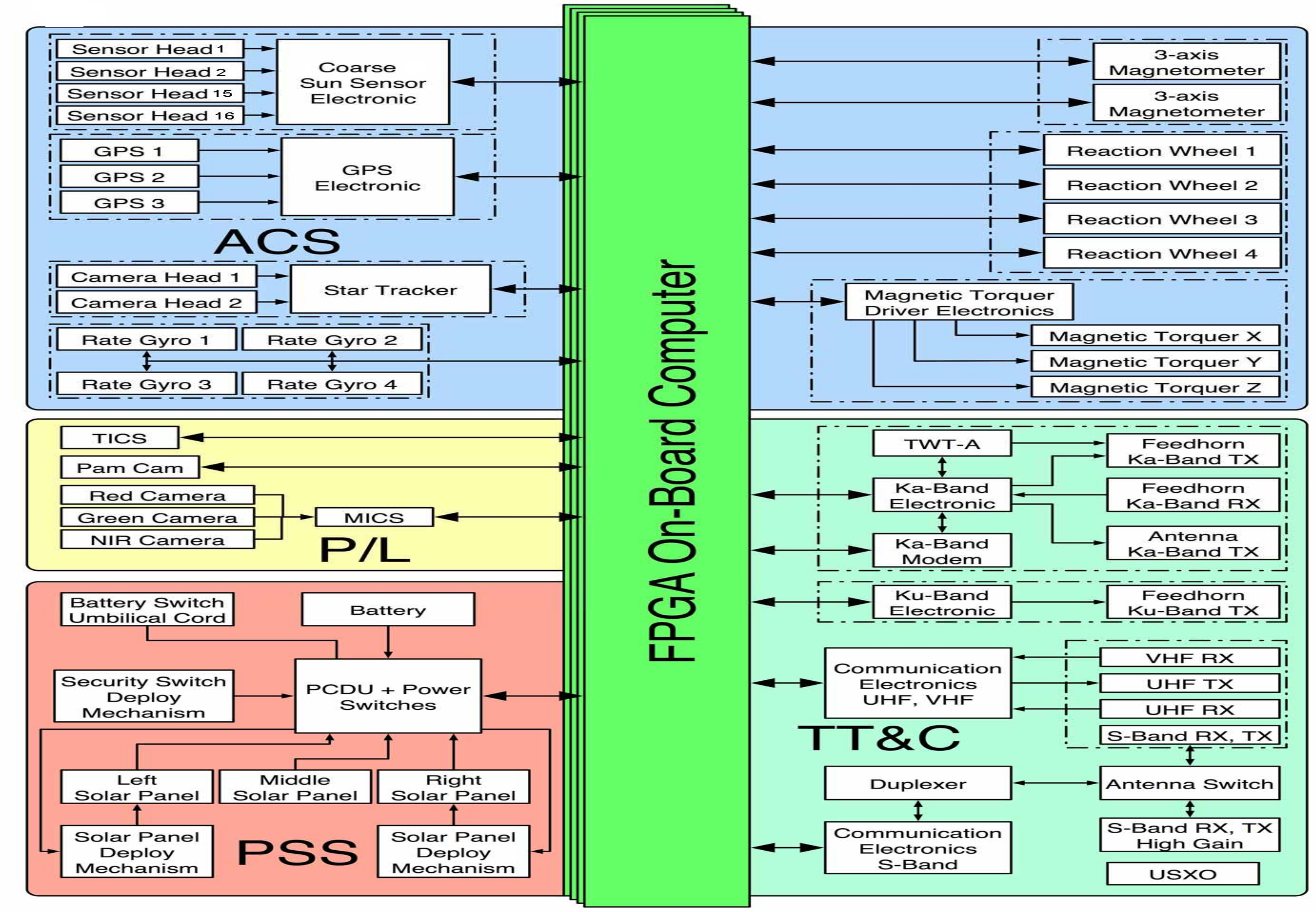
FLP Primary Mission Objectives



Technology demonstration:

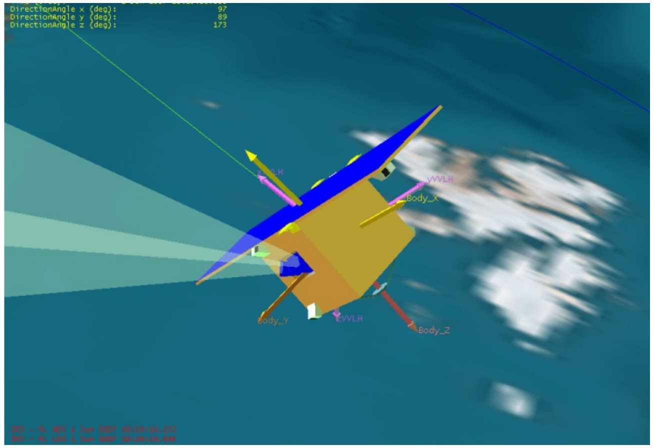
- FPGA On-Board Computing System
- High speed Ka-band communication
- Accurate and agile attitude control system (7.5 arcseconds, Abs.)
- GENIUS – GPS Experiment
- NEA detection using the Star Tracker
- 'Rent-A-Sat' mode
- Fiber Optical Gyros
- Solar Cells

1 S-band Antennas (LG)
2 Communication Unit
3 Ka-band Electronic
4 On-board Computer
5 Star Tracker
6 Magnetometers
7 Reaction Wheels
8 Power Control Unit
9 Sun Sensor
10 MICS
11 Gyros
12 VHF Antenna
13 Deployment Device
14 Magnetic Torquer
15 Ultra Stable Oscillator
16 TICS
17 Travelling Wave Tube
18 Ka-band Feed Horn (LG)
19 PamCam
20 Feed Horns
21 Cassegrain Mirror
22 Li-Ion Batteries
23 S-band Antenna (HG)
24 UHF-Antenna


Sensor Head 1
Sensor Head 2
Sensor Head 15
Sensor Head 16
Coarse Sun Sensor Electronic
GPS 1
GPS 2
GPS 3
GPS Electronic
ACS
Camera Head 1
Camera Head 2
Star Tracker
Rate Gyro 1
Rate Gyro 2
Rate Gyro 3
Rate Gyro 4
3-axis Magnetometer
3-axis Magnetometer
Reaction Wheel 1
Reaction Wheel 2
Reaction Wheel 3
Reaction Wheel 4
Magnetic Torquer Driver Electronics
Magnetic Torquer X
Magnetic Torquer Y
Magnetic Torquer Z
FPGA On-Board Computer
TICS
Pam Cam
Red Camera
Green Camera
NIR Camera
MICS
P/L
TWT-A
Ka-Band Electronic
Ka-Band Modem
Feedhorn Ka-Band TX
Feedhorn Ka-Band RX
Antenna Ka-Band TX
Ku-Band Electronic
Feedhorn Ku-Band TX
Communication Electronics UHF, VHF
VHF RX
UHF TX
UHF RX
S-Band RX, TX
TT&C
Duplexer
Antenna Switch
S-Band RX, TX High Gain
Communication Electronics S-Band
USXO
Battery Switch Umbilical Cord
Battery
Security Switch Deploy Mechanism
PCDU + Power Switches
Left Solar Panel
Middle Solar Panel
Right Solar Panel
Solar Panel Deploy Mechanism
PSS
Solar Panel Deploy Mechanism

ACS Hardware

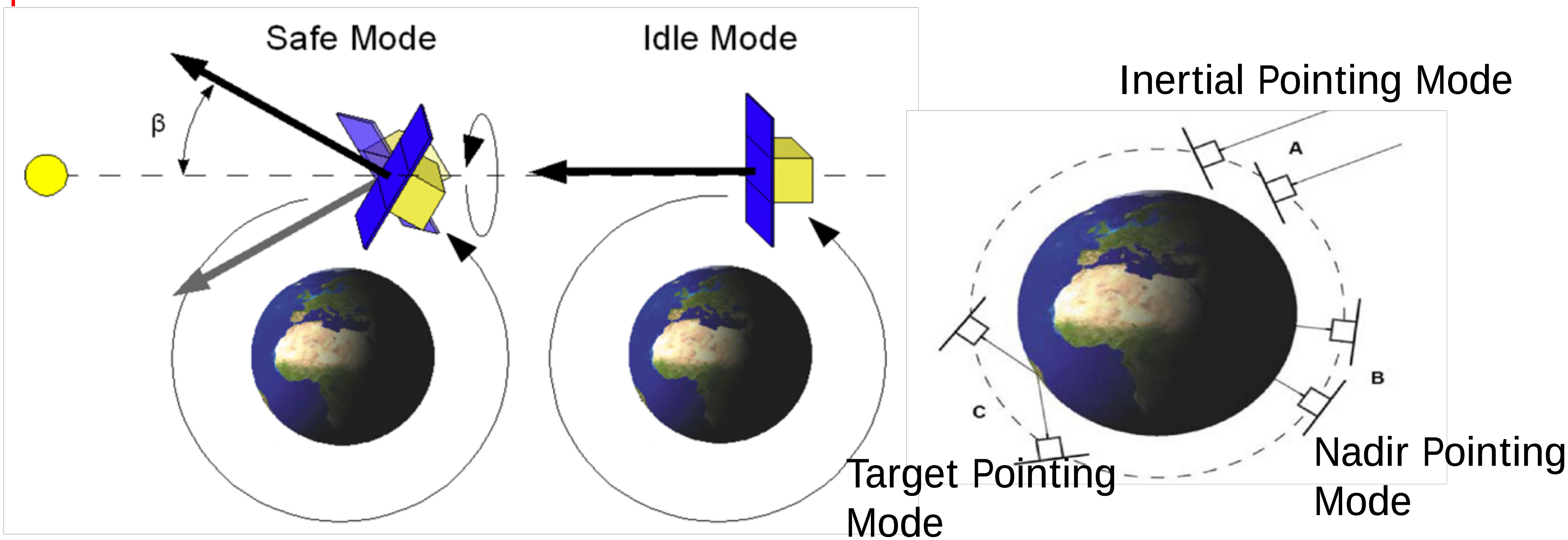
Attitude Control System



ACS Components	Number
Reaction Wheels	4
Magnetic Torquer	3
3-axis Magnetometer	2
Coarse Sun Sensor	16
GPS	3
Star Tracker Camera Heads	2
Single axis rate gyro	4

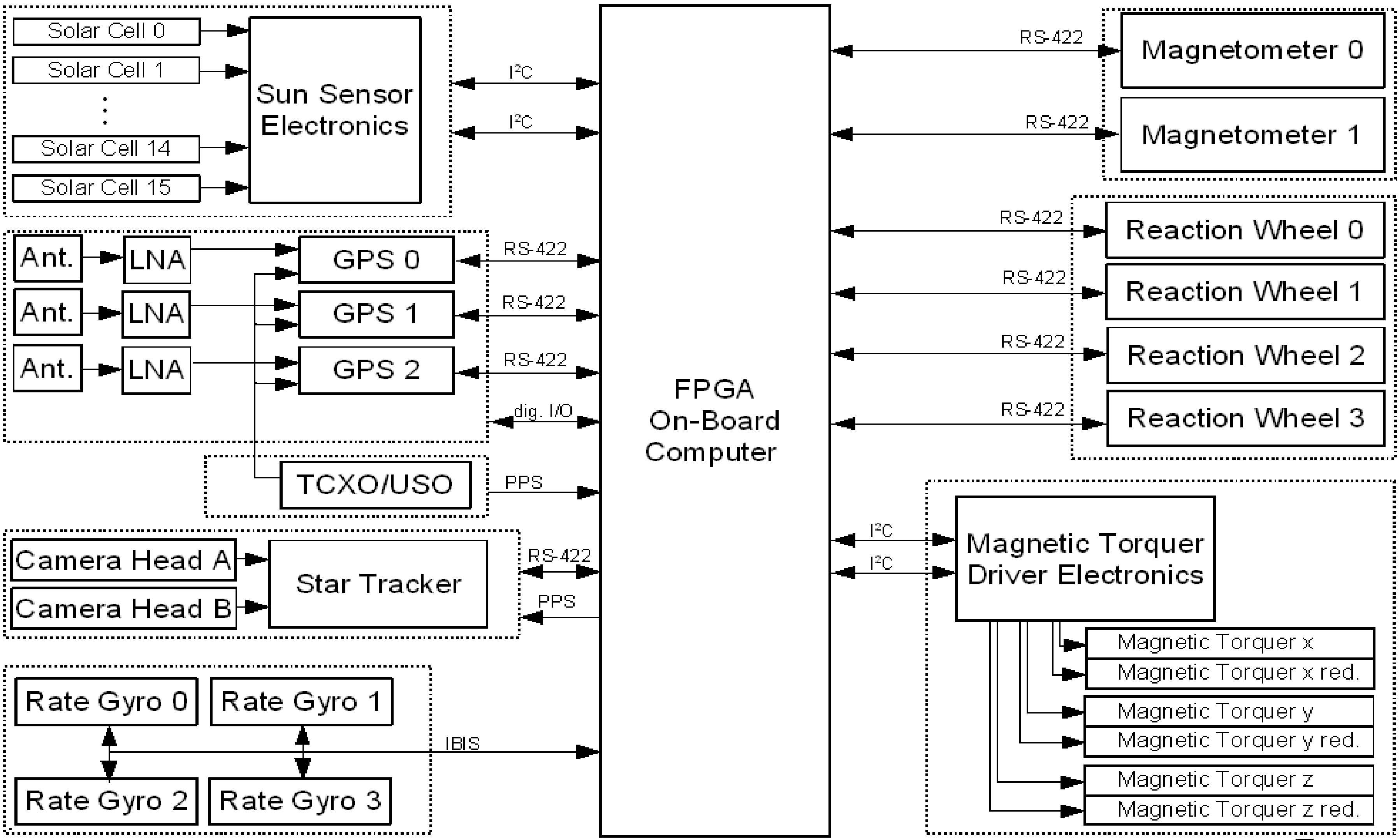
Pointing knowledge, absolute	±7 arcsec (±1 pixel)
Pointing knowledge, relative	±2.5 arcsec (±1/3 pixel)
Pointing accuracy	±150 arcsec (± 20 pixel)

Attitude Control Mode



Mode	RW	MGT	MGM	GPS	STR	FOG	SuS
Detumblimg		√	√				
Safe		√	√				√
Idle	√	√	√		√	√	√
Target P.	√	√	√	√	√	√	
Nadir P.	√	√	√	√	√	√	
Inertial P.	√	√	√		√	√	

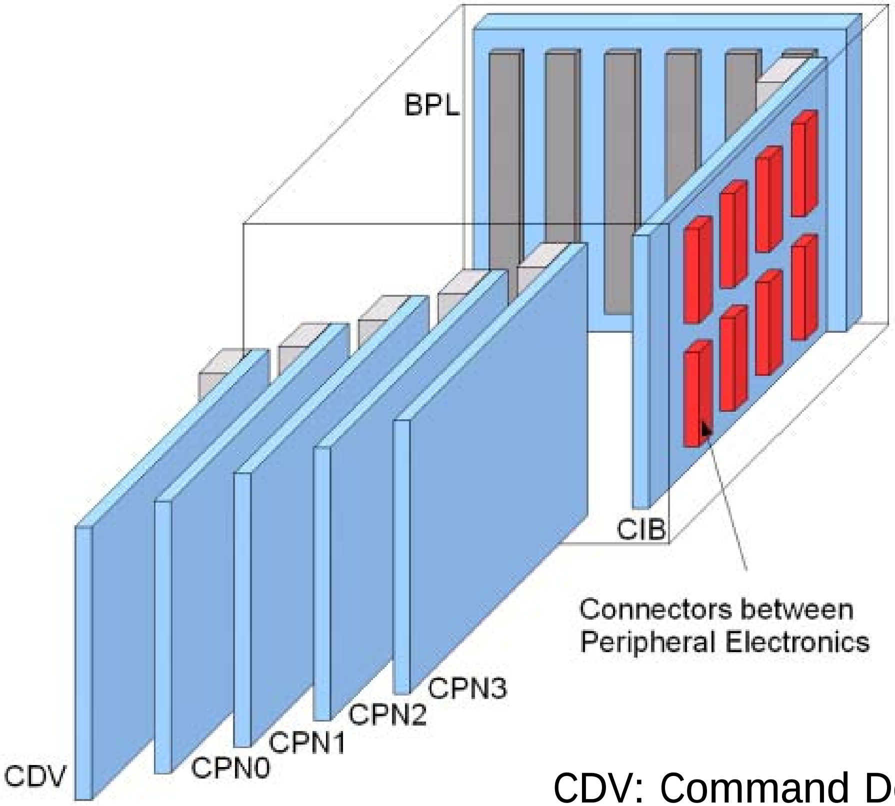
Hardware Connections

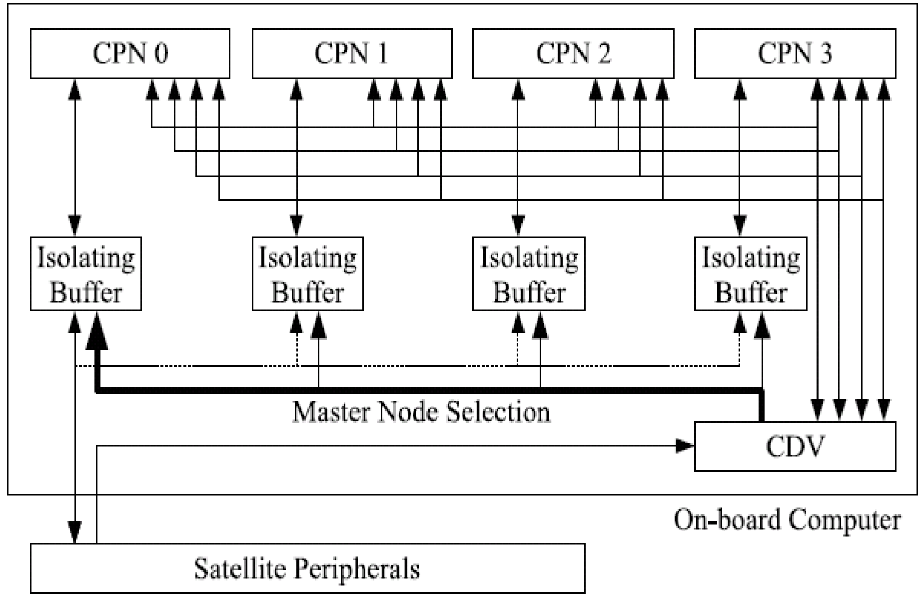


FPGA On-Board Computer

- FPGA: Field Programmable Gate Array
  - Programmable Logic
  - Reconfigurable
  - No software
  - Parallel executable processes
- Advantages against traditional Microprocessor-based Computing System
  - Reconfigurable
  - Start-up und reset within ms order
  - No interference between parallel processes
  - Precise timing
  - Reduction of hardware interface

On-board Computing System (OBC) Hardware Configuration

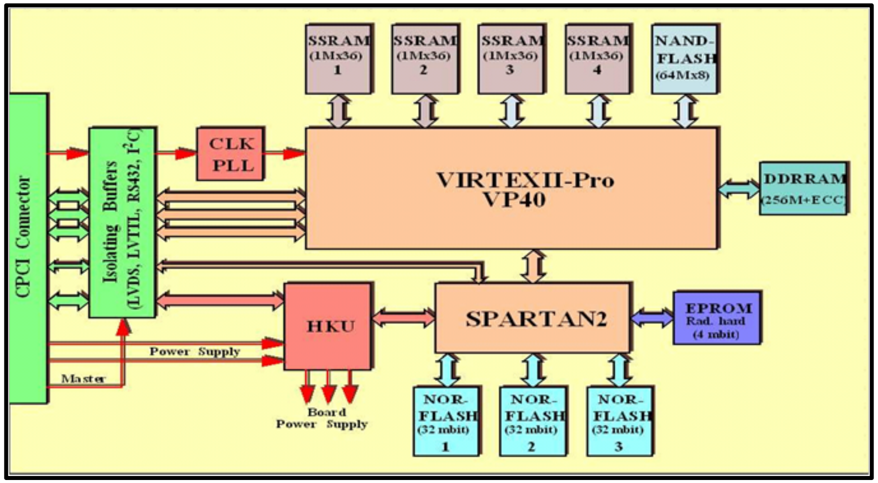




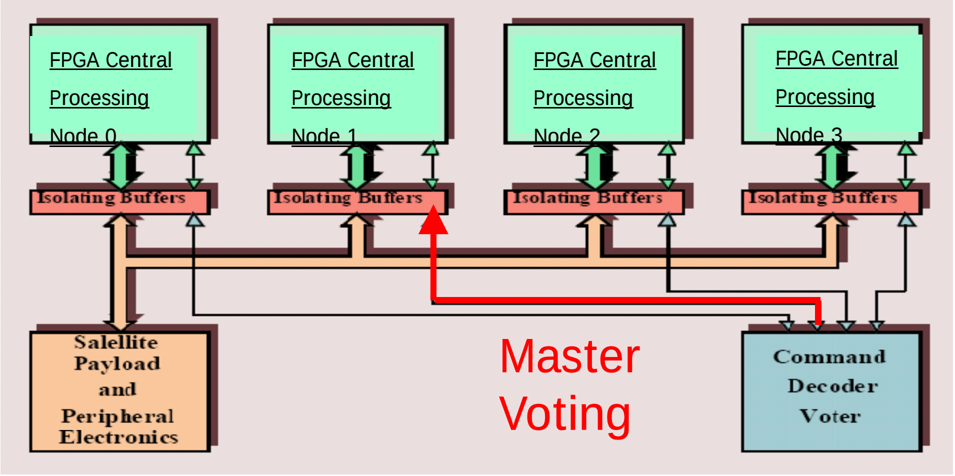
CDV: Command Decoder and Voter
CPN: Central Processing Node
BPL: Back Plane
CIB: Connector Interface Board

OBC Configuration (Quad FPGA Architecture)

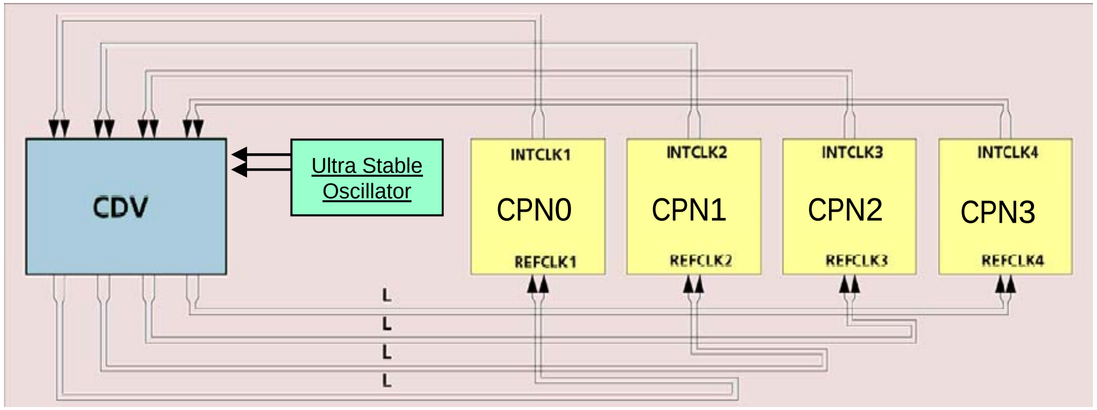
CPN Block Diagram



OBC Architecture

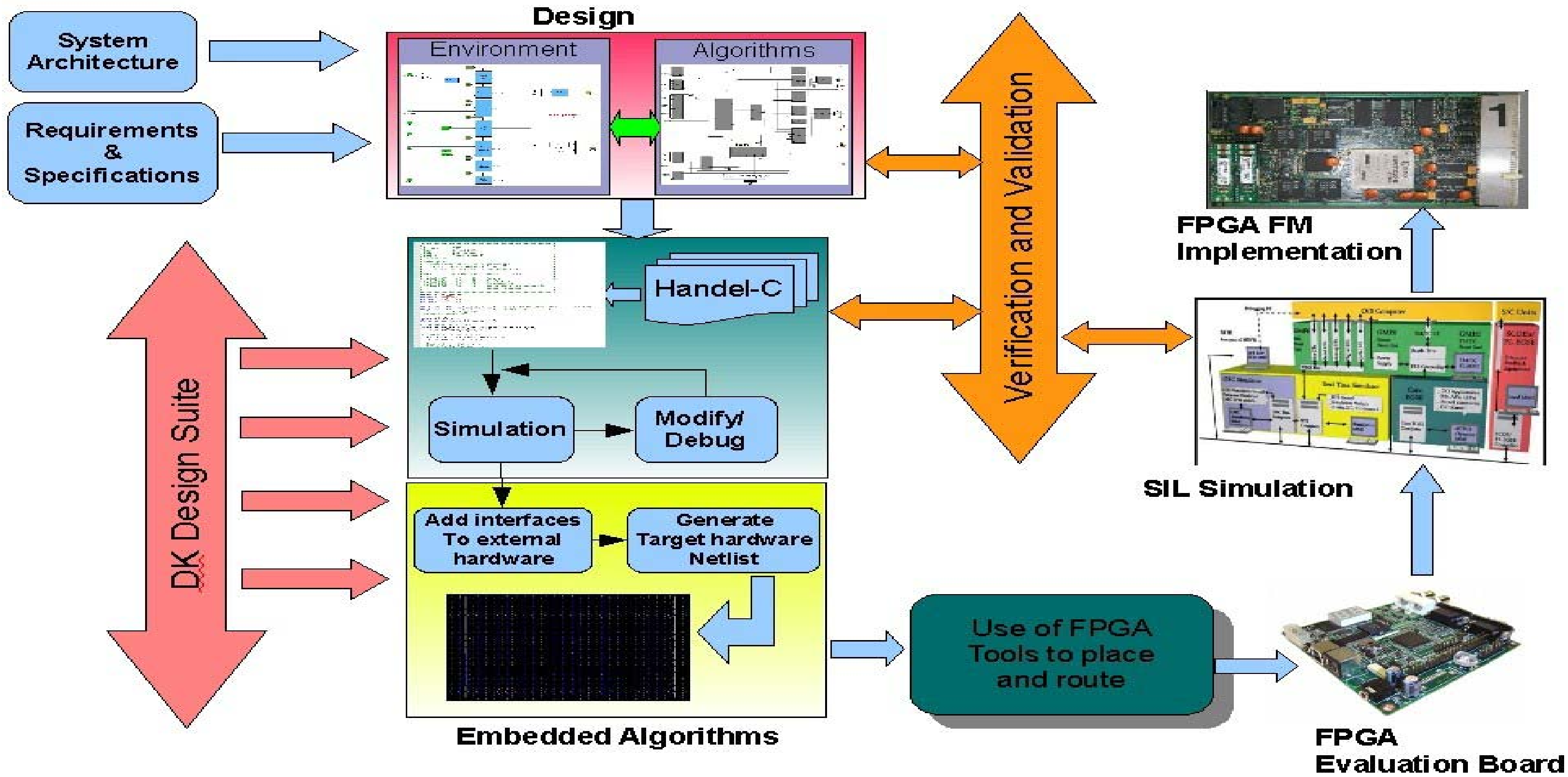


Clock Distribution

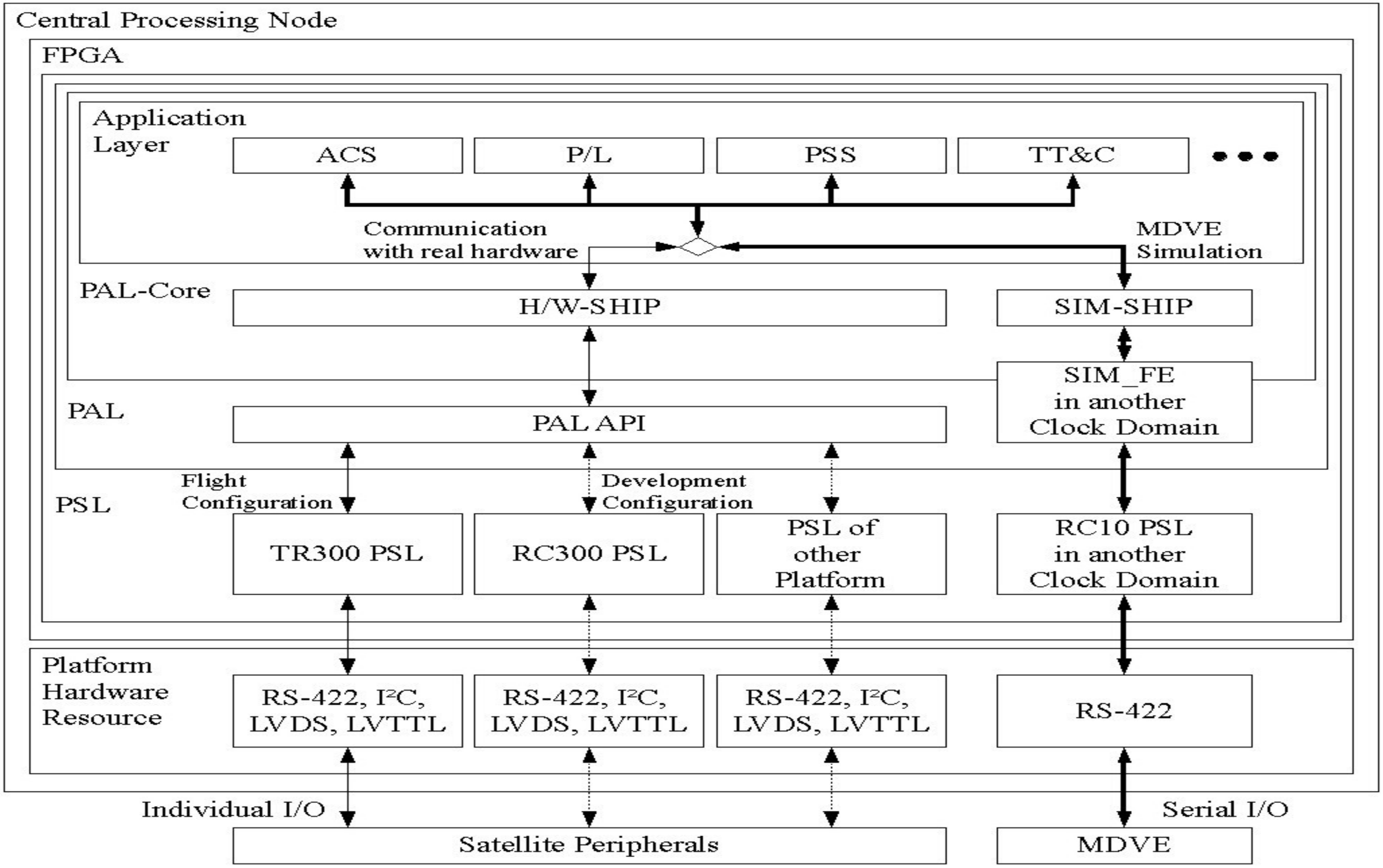


- 4 million system gates
- 200MHz clock
- 256 MB RAM
- 4 Banks of 1Mx36 SSRAMs (indep. access)
- Triple redundant config. Flash

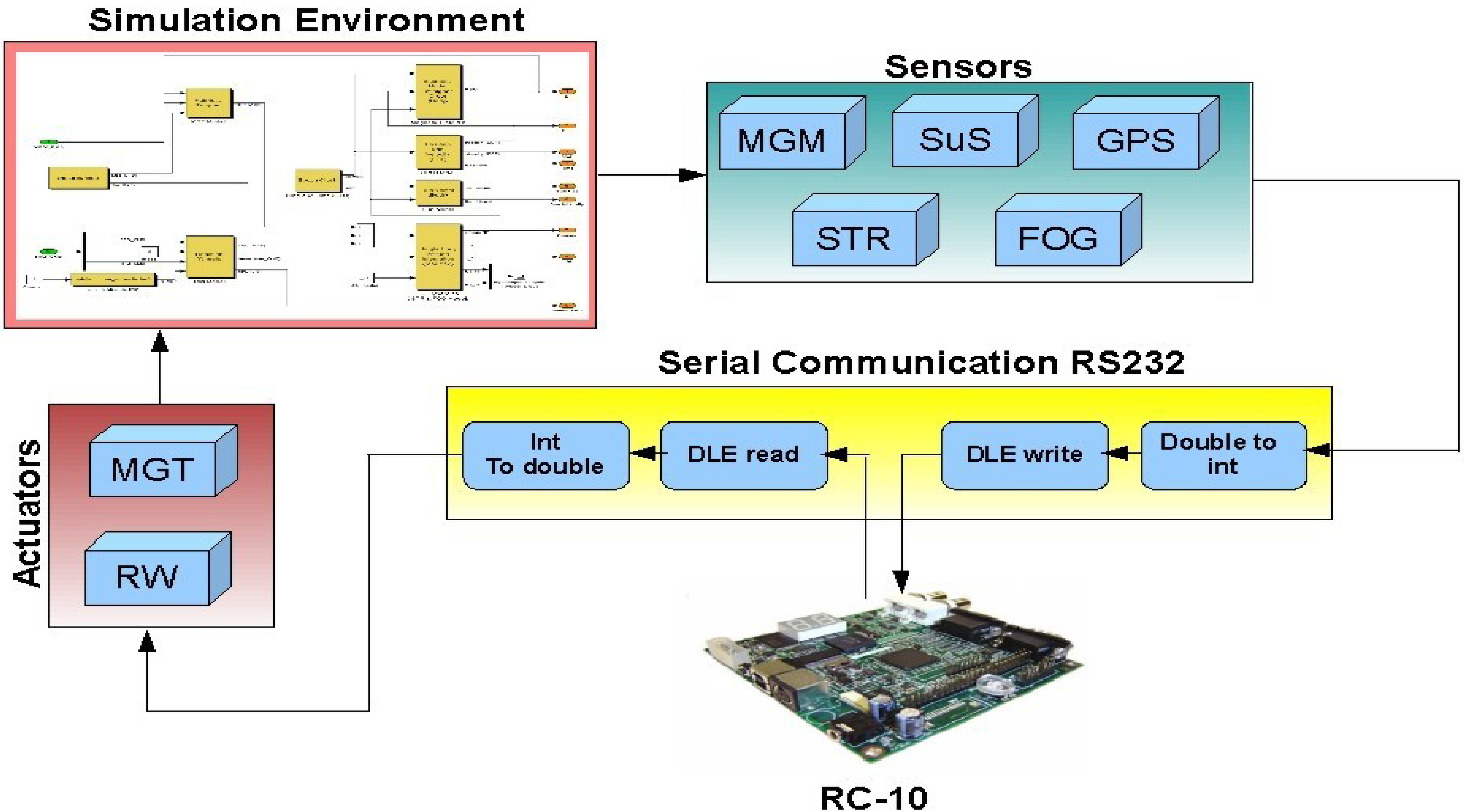
Algorithms Development and Testing



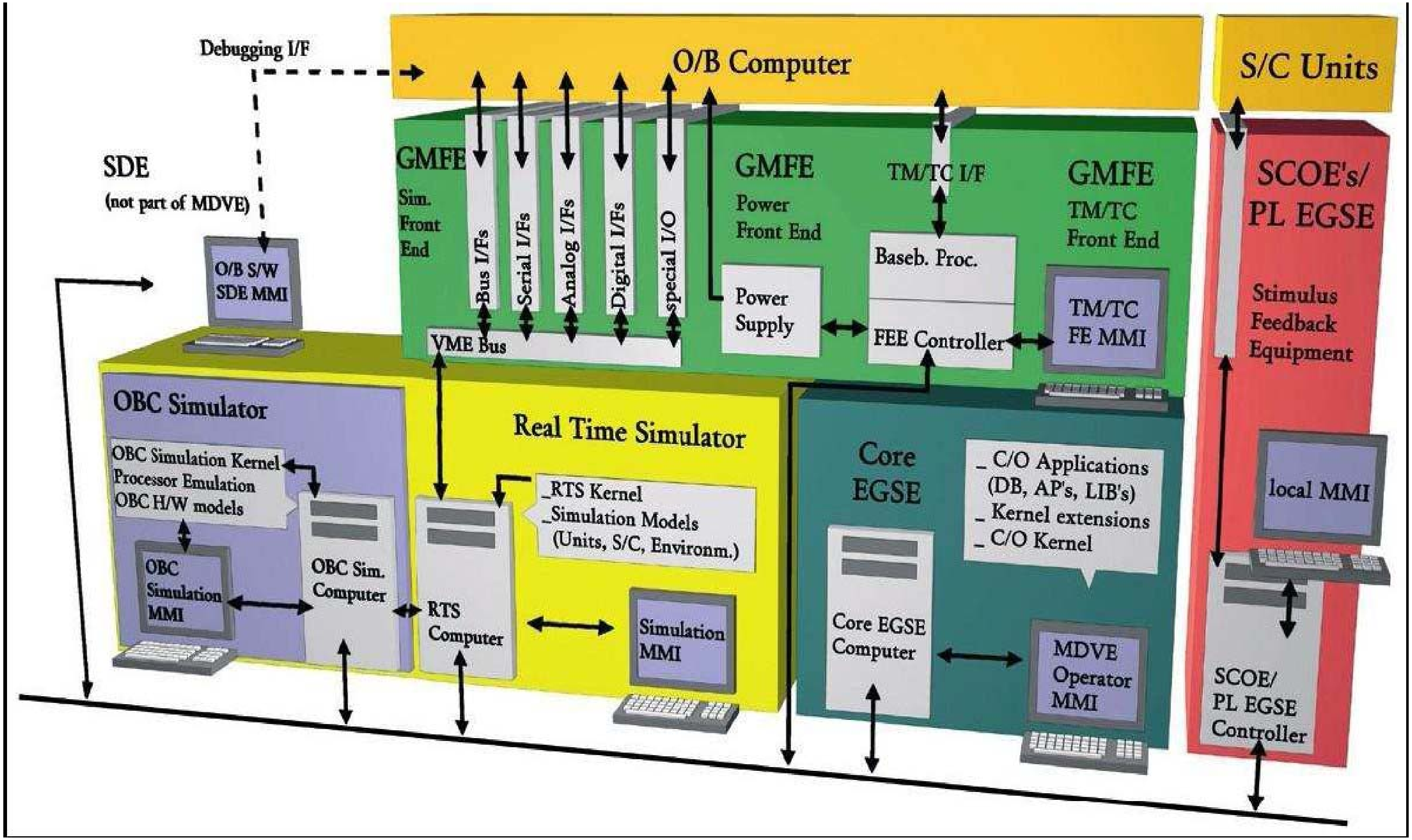
Layered Structure of Algorithms Implementation



Matlab Simulation Environment

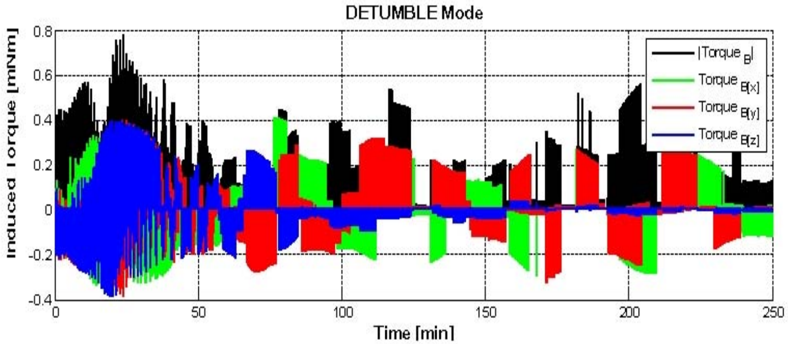


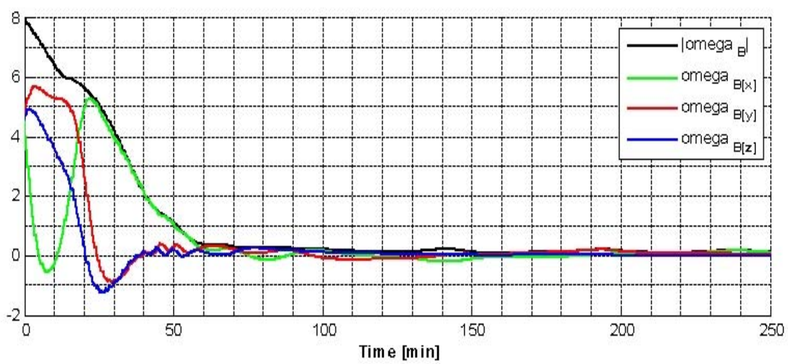
MDVE


Debugging I/F
O/B Computer
S/C Units
SDE
(not part of MDVE)
O/B S/W SDE MMI
GMFE Sim. Front End
Bus I/Fs
Serial I/Fs
Analog I/Fs
Digital I/Fs
special I/O
VME Bus
GMFE Power Front End
Power Supply
TM/TC I/F
Baseb. Proc.
FEE Controller
GMFE TM/TC Front End
TM/TC FE MMI
SCOE's/ PL EGSE
Stimulus Feedback Equipment
local MMI
SCOE/ PL EGSE Controller
OBC Simulator
OBC Simulation Kernel
Processor Emulation
OBC H/W models
OBC Simulation MMI
OBC Sim. Computer
Real Time Simulator
_RTS Kernel
_Simulation Models
(Units, S/C, Environm.)
RTS Computer
Simulation MMI
Core EGSE
_ C/O Applications
(DB, AP's, LIB's)
_ Kernel extensions
_ C/O Kernel
Core EGSE Computer
MDVE Operator MMI

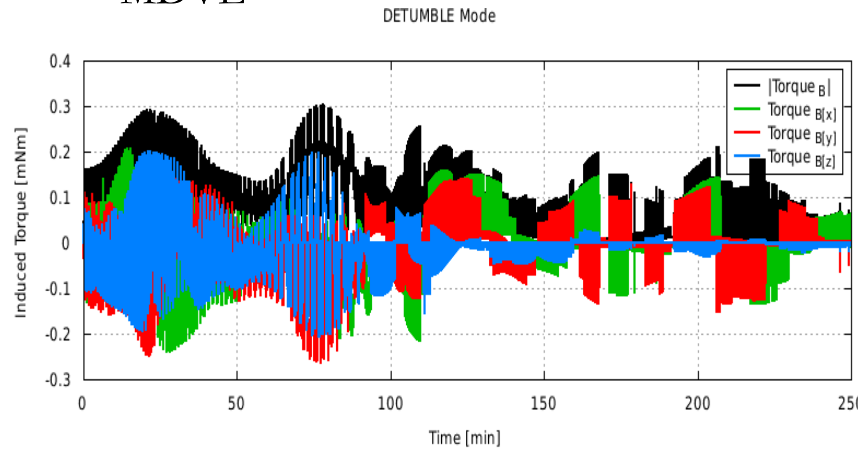
Results

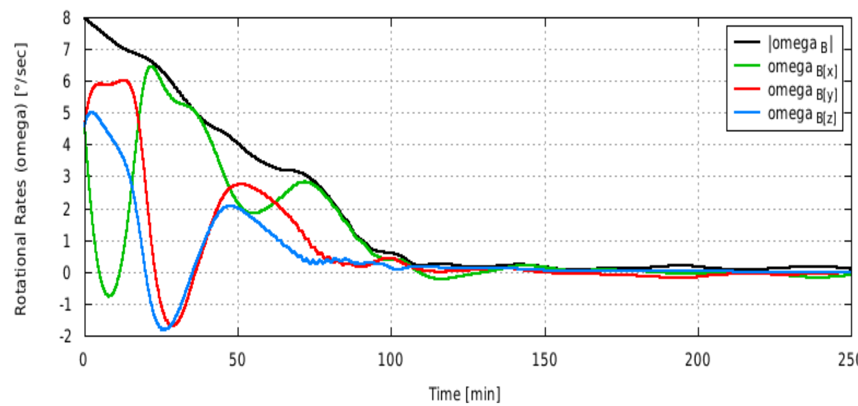
Matlab Simulator



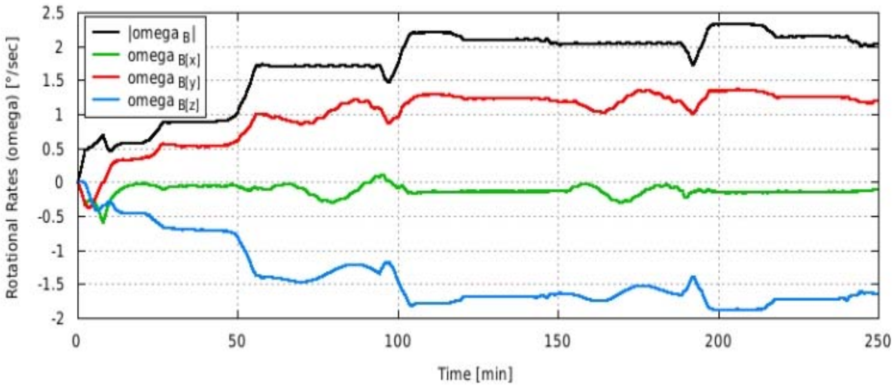


MDVE

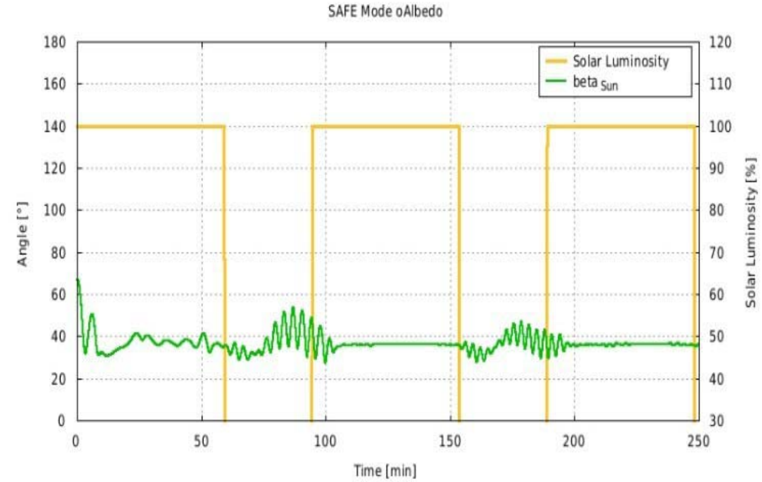




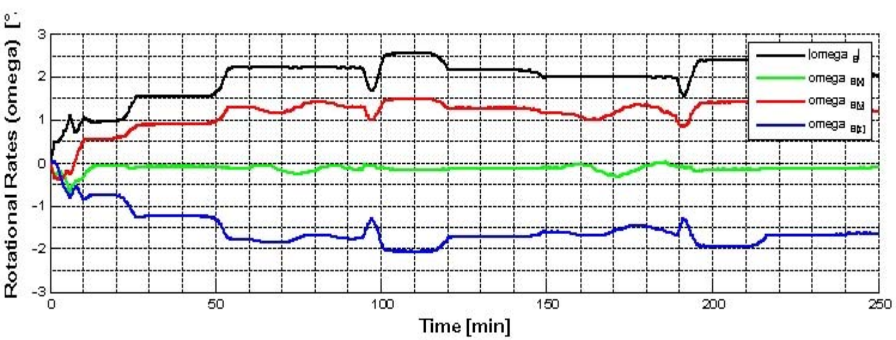
Safe mode



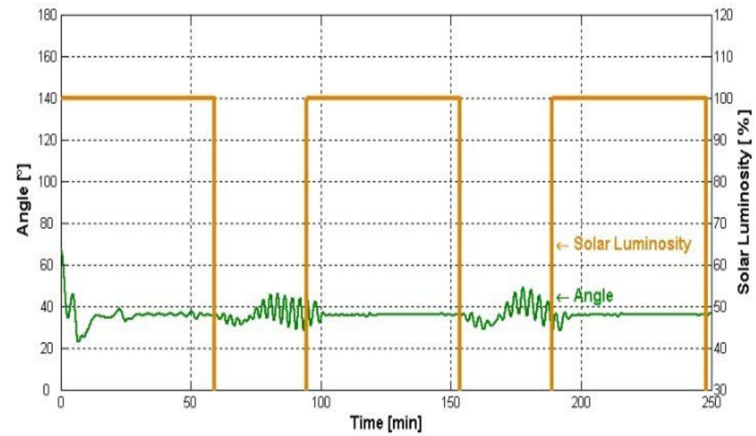
(a) Rotational Rates (MDVE)



(a) Angle between solar panel normal and sun vector (MDVE)

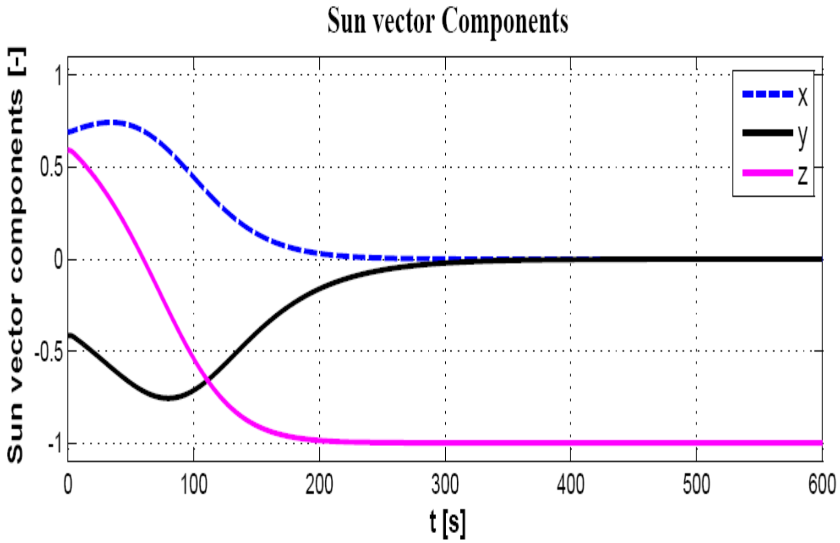


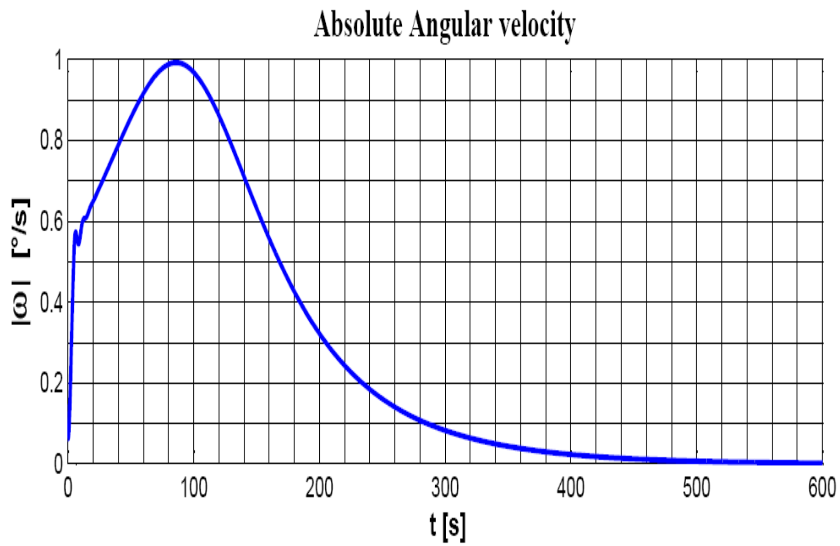
(b) Rotational Rates (Matlab Simulator)



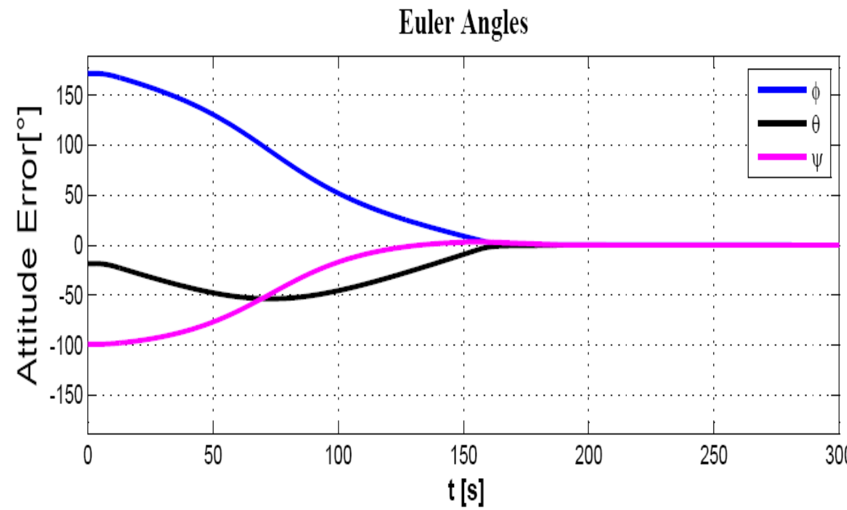
(b) Angle between solar panel normal and sun vector (Matlab Simulator)

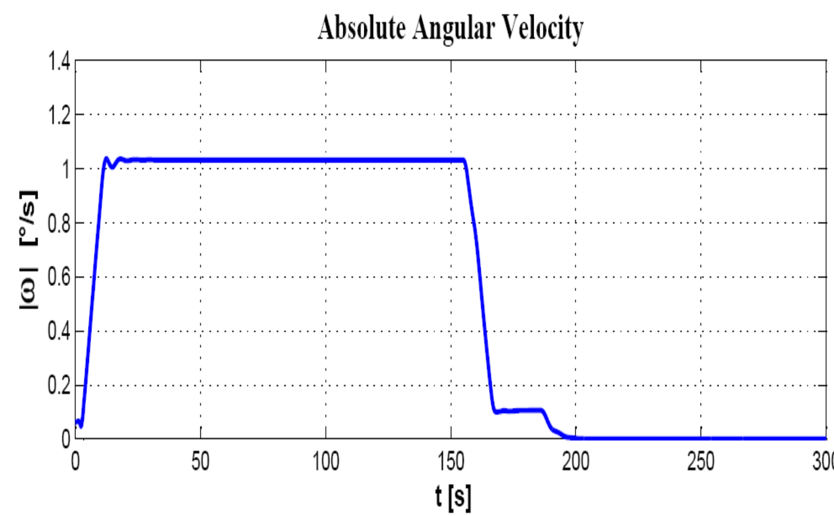
Idle mode





Inertial Pointing Mode





Conclusions

- In this paper the entire ACS algorithms are implemented in a FPGA-based OBC. The implementation of the interface between the simulator and OBC is described. The conducted work shows that building an ACS entirely in hardware is possible. The performance of embedded ACS algorithms is verified through the simulation in the loop tests. The use of two different kinds of simulation environments further increase the credibility of these tests. The results of MDVE are compared with the results of the Matlab Simulator. Both results are consistent and they also verify the developed simulation environment.
- The established simulation environment could further be utilized for the development and verification of the on-board algorithms of the FPGA-based OBC as well as this could be further used in the Hardware-in-the-loop tests by using the satellite hardware components.

THANKS