Rapid Development of Experimental LEON 3FT Controller Board (LCB)

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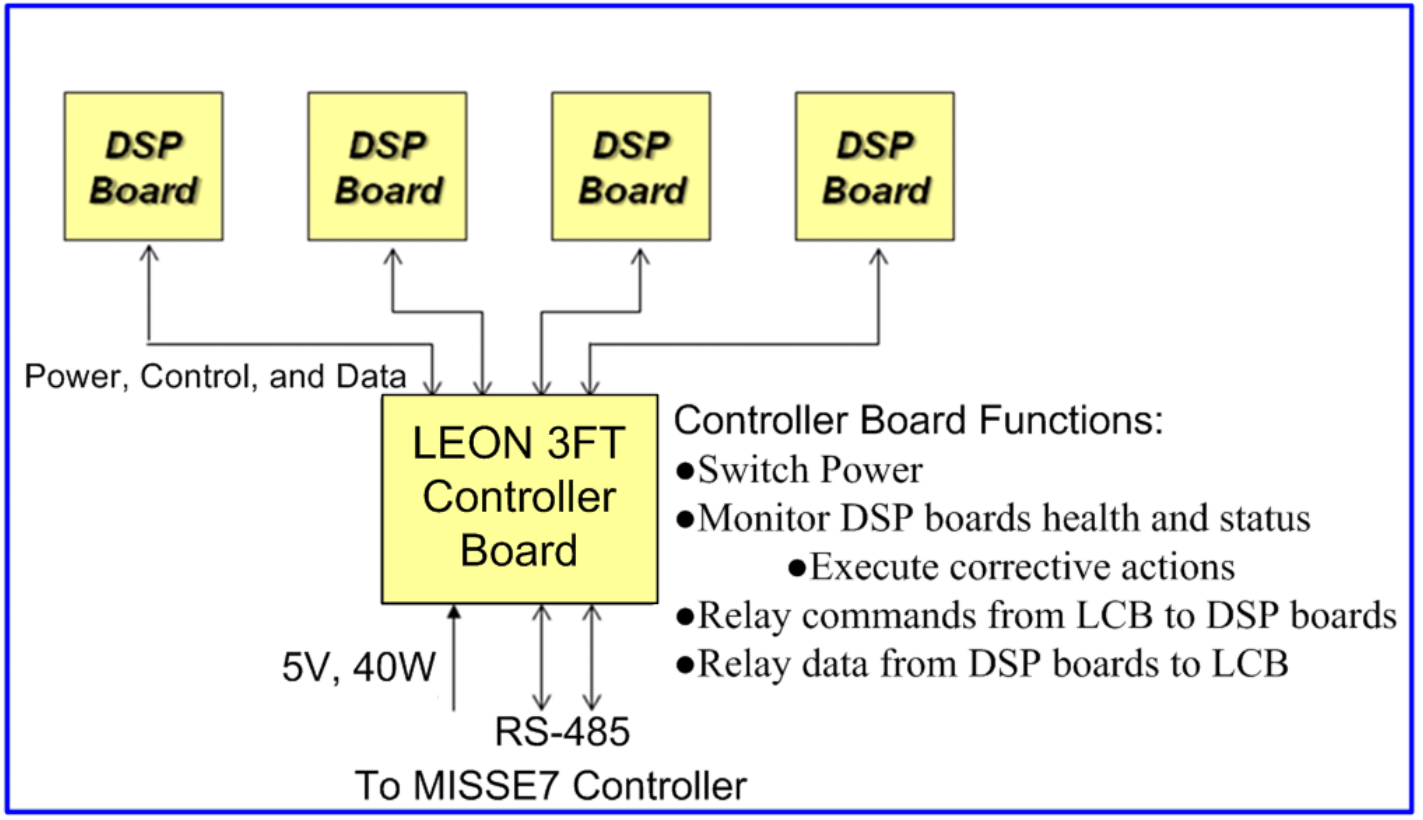
Background

- **The LCB is part of the Materials International Space Station Experiment (MISSE) Program**
  - **Characterize Experimental Materials in a Space Environment**
  - **Six experiments have been deployed to date**
- **MISSE-7: First to support active payloads**
  - **Includes the capability to remotely command and monitor experiments**
  - **Scheduled to launch in November of 2009**

NASA Image ISSO13E63407: Image of MISSE-3 following deployment on the outside of ISS on August 3, 2006

Initial Concept

- **The LCB will Monitor and Control 4 Experimental DSP Boards**
  - **Provide 2A/5V to each DSP Board**
  - **Clocking to each experiment**
  - **4 Channels each of A to D Conversion**
  - **8 Watchdog signal inputs (2 per DSP Board)**
  - **RS-485 for Ground Communication**



The Problem?

- **Technical**
  - Develop a complex 32 bit processor board design with all of the functionality from the initial concept
- **Schedule**
  - Delivery of two EM units 5 months from the start date
  - Flight unit delivery one month after the two EM Units
- **Start Date**
  - July 2008

Critical Aspects To Consider

- **Assess the goals of the program**
  - **Is there a reasonable probability of success???**
    - **Experience level of the team?**
    - **Complexity?**
    - **Clock Speeds vs. chosen technology?**
- **No specification provided**
  - **The LCB team had only the previous "Initial Concept" as a starting point for the design**
    - **Spec development will need to occur while the design is being implemented**
    - **Maintain close contact between all parties involved**
      - **Aeroflex Colorado Springs – LCB**
      - **Coherent Logix – DSP Boards**
      - **Goddard Space Flight Center – Ground Com**

Critical Aspects To Consider

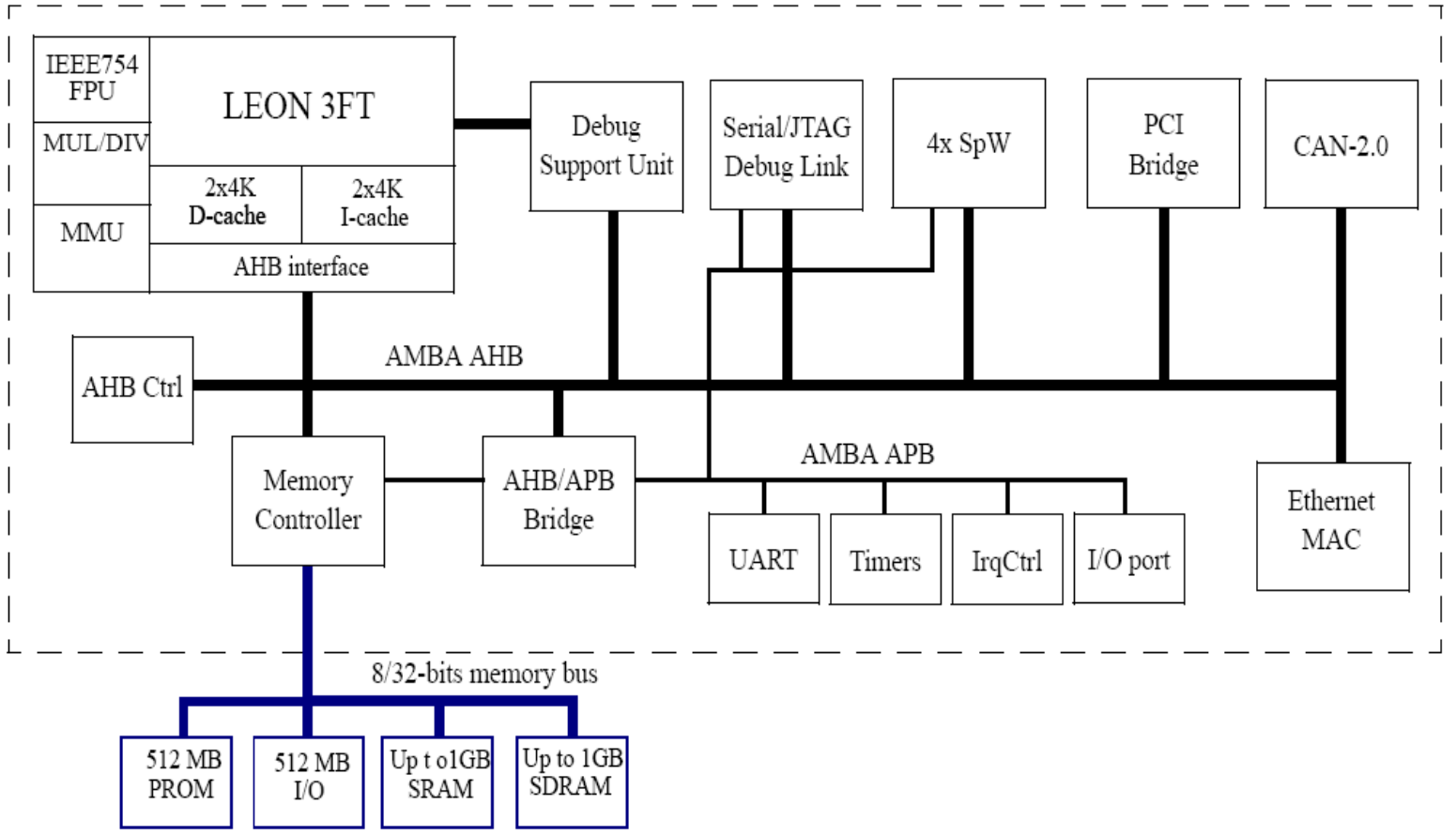
- **Original approach had a separate module for the 5V power switching**
  - **Early in the program it was decided to include this functionality on the LCB**
    - **Mixing high current circuits with digital can be difficult**
- **Assessing Device Availability**
  - **Must occur before a design approach can be solidified**
    - **Flight suitable devices typically have long lead times**
    - **Often it is the small discrete transistors or diodes that are the most problematic**
  - **Processor memory requirements particularly important**

Critical Aspects To Consider

- **Approach must be flexible**
  - Design changes may come late
  - Consider using an FPGA with a path to flight
    - Board and FPGA design can progress at the same time
    - Allows late occurring changes
- **Software Development?**
  - Decide on responsibilities
- **Designed for flight but not tested to flight levels**
  - Qualification testing would have a significant impact on schedule
  - Testing performed at the unit level

LEON 3FT Processor Introduction

- **32 Bit Processor**
  - **SPARC V8 Architecture**
  - **IEEE-754 FPU**



Design Approach

- Begin with draft of LCB Specification
  - Subsequent spec modifications to occur during development
  - Plan for numerous tele-cons per week
- LCB team allowed to define the board interfaces
  - LVDS for DSP Board Communication
- Implement an FPGA for the LEON 3FT to DSP Board Interface
  - Easiest and most flexible
    - Socket for engineering units
  - Register based approach
    - Simple decode of address and control signals
    - LEON 3FT performs transactions to and from registers in the FPGA
- Software
  - LCB team to develop Application Programming Interface (API)
  - NASA Goddard and Coherent Logix to develop application
- Discrete Power switching design with current limit
  - Current trip to FPGA at 2A

FPGA Design Considerations

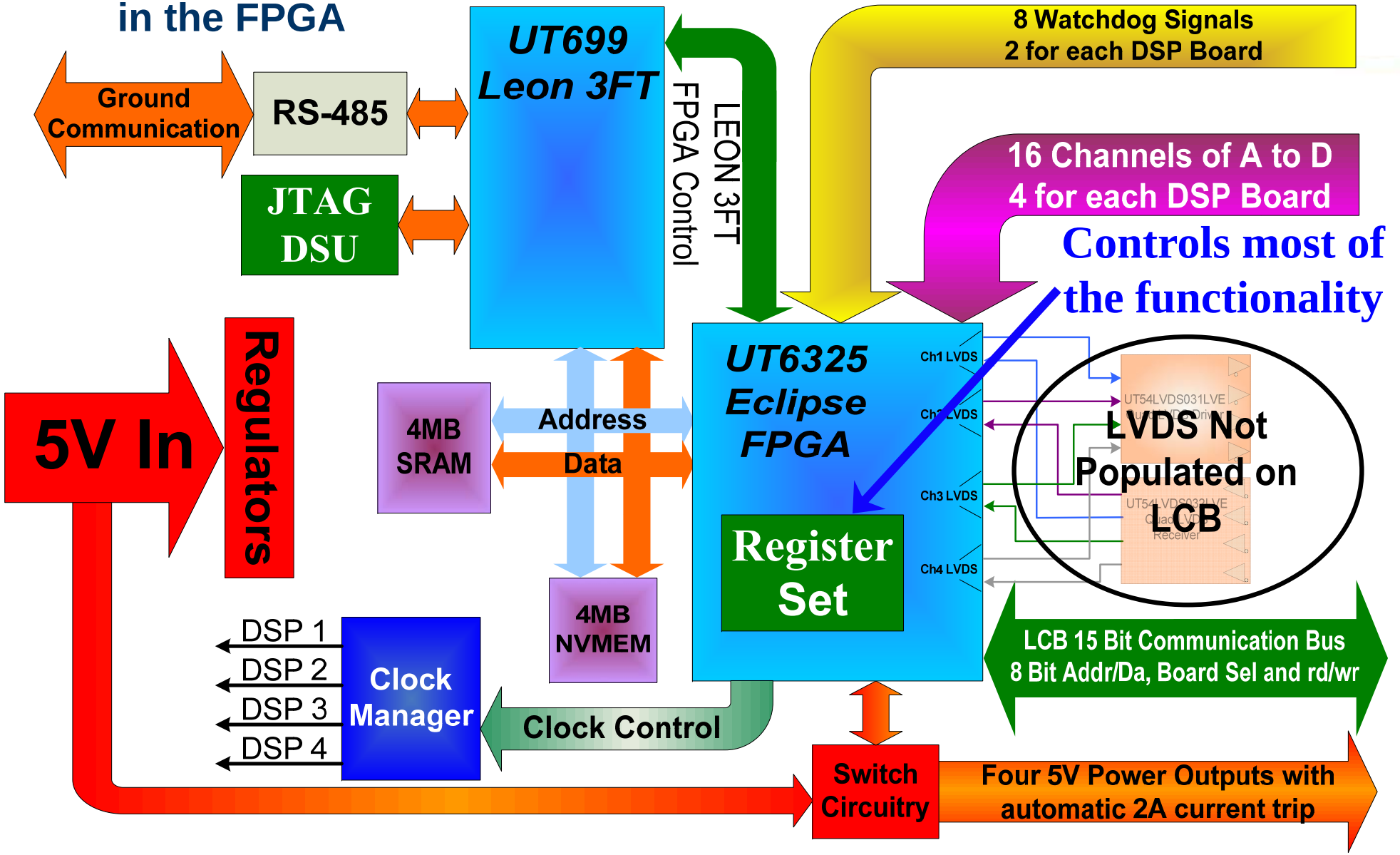
- Insure LEON 3FT and FPGA single clock domain
  - Match clock trace signals to LEON 3FT and FPGA
  - Simplifies the interface by data not having to cross clock boundaries
- Current Trip signals generated by analog circuits
  - Signals must be synched into digital clock domains
    - Implement voting circuits to help prevent glitches from causing a trip
- Inrush current from DSP board could be higher than the 2A trip
  - Implement a timer to wait before sampling input signal
    - Timer set at 2ms

Design Tradeoffs/Changes

- **LVDS Serial bus vs. 8 bit Addr/data bus**
  - **LVDS was the approach proposed by the LCB team**
    - **Design files supplied from the LCB team to the DSP Board team**
      - **Considerable effort still needed by DSP Design Team**
      - **Design had FIFO requirement**
        - **FIFO's can be tricky to implement and could be a perceived risk**
  - **The DSP Board Team suggested a preference for an 8 Bit Addr/Data bus in place of LVDS**
    - **Implementation was very simple**
      - **Verilog code written in less than 4 hours**
    - **Added risk in the event of a failure on the bus**
      - **Addr/data bus common to all 4 DSP boards**
      - **Failure could disable communication to all boards**
  - **Ultimately it was agreed to use the 8 bit Addr/Data bus**
    - **In this case the DSP Board Team is the customer**
    - **Sometimes the simplest approach is not the least risky**

Final LCB Architecture

- The Leon 3FT interfaces to the 4 DSP boards through registers in the FPGA

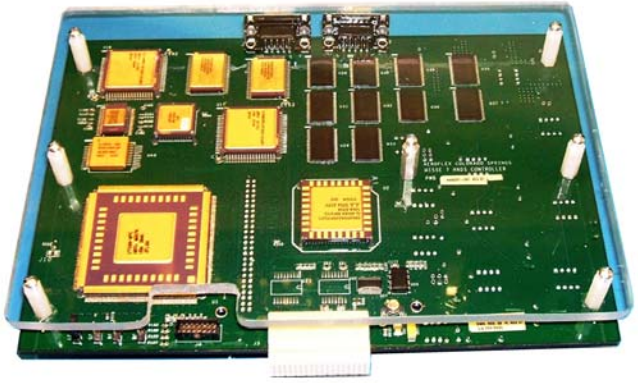


Delivery

- **The Team was able to deliver the two EM units on time**
  - **The power switching circuits needed some modifications**
    - **Manufacturing assured the team that the rework was flight worthy**
- **Schedule relief occurred around the first of 2009**
  - **Gave the team approximately 1½ months of additional time**
    - **The team decided to re-spin the PWB and give NASA a clean board for flight**
- **Flight board delivered in February of 2009**

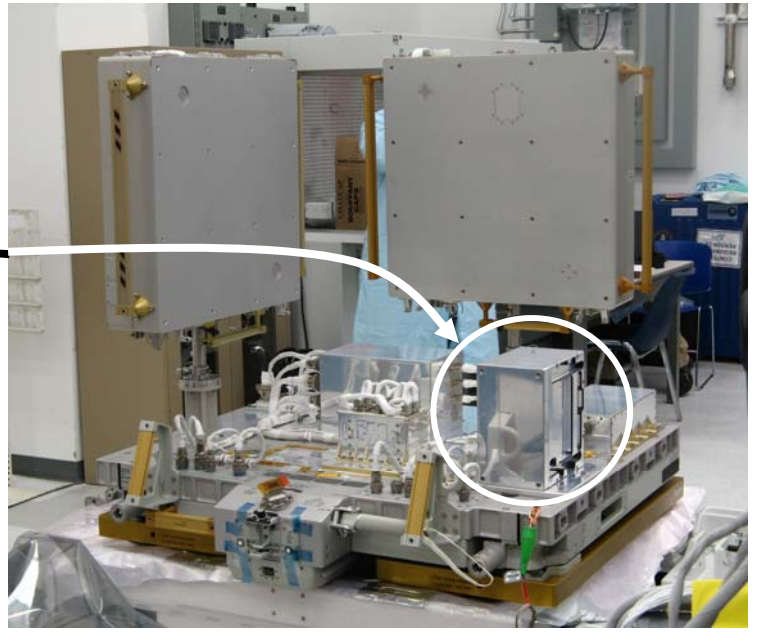
Status

- **The experiment has passed all tests and been integrated onto the payload**
- **The Payload is ready for launch on Space Shuttle mission STS-129 in November 2009**



LCB Flight Board
(6U Form Factor)

LCB and DSP Boards in Unit Configuration



MISSE-7 Pallet
(NASA Photo)

MISSE-7 Website
http://www.nasa.gov/mission_pages/station/science/experiments/MISSE-7.html#description

Keys to Success

- **Open Communication**
  - **The three teams stayed in close contact during the entire program**
    - **Specification and design allowed to progress in a very timely manor**
- **FPGA Design required no timing constraints**
  - **Timing analysis of digital logic can have a significant impact on schedule**
- **All parties involved were very dedicated and professional**
  - **Issues were worked concurrently**
    - **Solutions for most issues were arrived at very quickly**
- **There is no shortcut for experience**