Single Event Effects (SEE) Mitigation of Reconfigurable FPGAs

David R. Czajkowski, Manish P. Pagey,
Murat Goksel, David J. Bozek

Space Micro Inc.
10401 Roselle Street STE 400
San Diego, CA 92121
858-332-0700

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Reconfigurable FPGAs in SmallSats

- Development Advantages
  - Ability to reconfigure (reprogram) aids in rapid development and testing
- On-Mission Reconfiguration
  - Changes in flight hardware needed
  - Updates or fixes required
  - Example: Change encryption algorithms/methods
- Xilinx *Virtex II, IV* Reconfigurable FPGAs
  - High capacity - gate count
  - High clock speed
  - TID & SEL are non-issues

  - *Single Event Effects are the challenge*

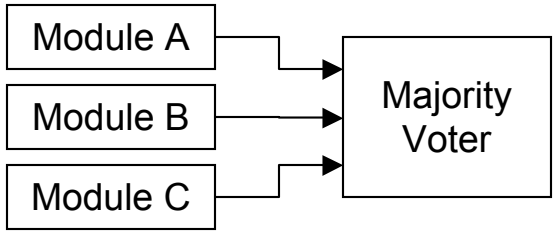
Xilinx Single Event Effects Problems

- Xilinx based FPGAs (ex. Virtex-II, -II Pro, and -4) suffer from the following SEE types:
  - Data SEUs
    Corrupts the data being passed through the FPGA
  - Reconfiguration SEUs
    Causing part or all of the chip to change function
  - SEFIs or “Hangs”
    Reconfiguration of the FPGA to a point that the FPGA locks up, including POR (reset)

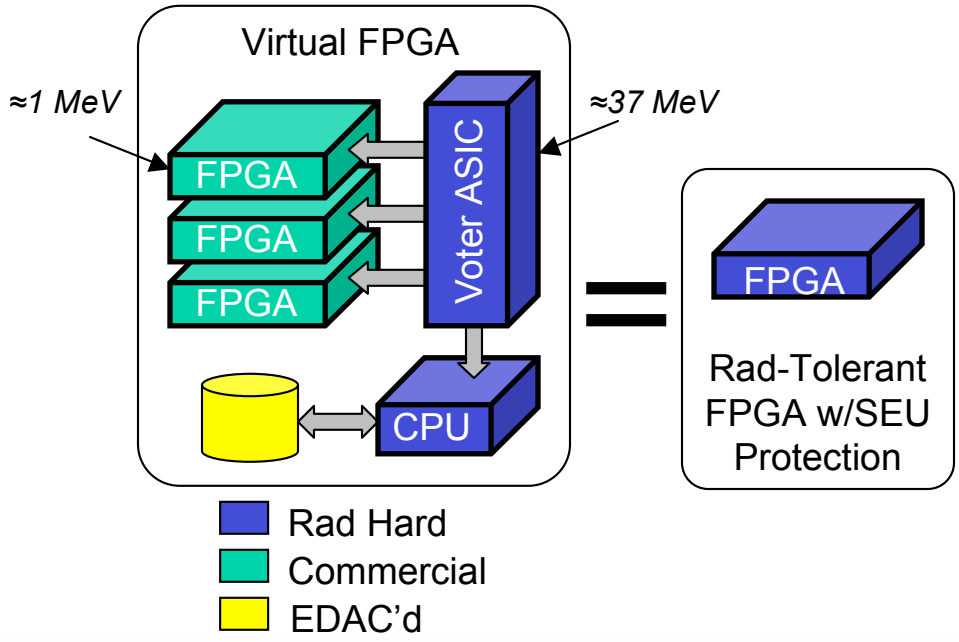
Current SEE Solutions for Xilinx FPGAs

- SEU Solutions
  - Triple Modular Redundancy
    - Need RH ASIC, CPU, EDAC for storage, etc.
    - Works in Actel Can be TMR'd at gate level
- SEFI Solutions
  - Partial or full reconfiguration
- Reconfiguration Solutions
  - Partial reconfiguration
  - Bitstream "scrubbing"

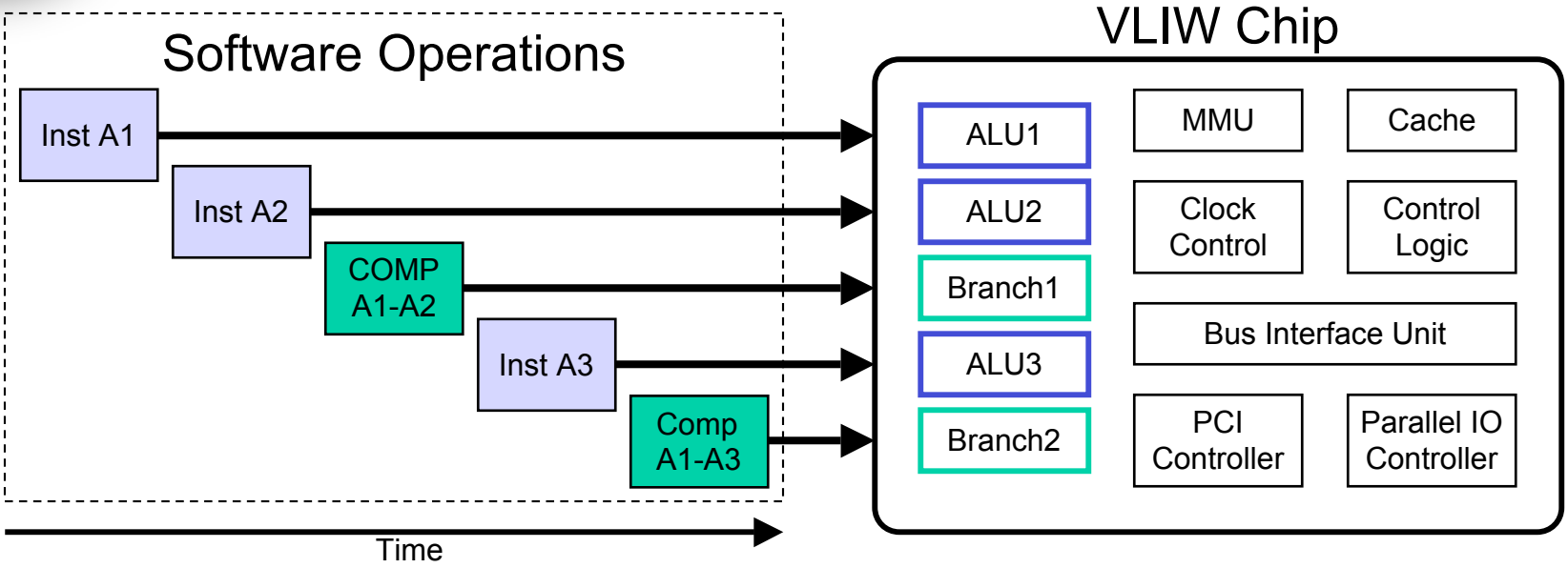
Triple Modular Redundancy



Xilinx Virtex TMR Implementation



SEU Detection and Correction using Time-Triple Modular Redundancy™

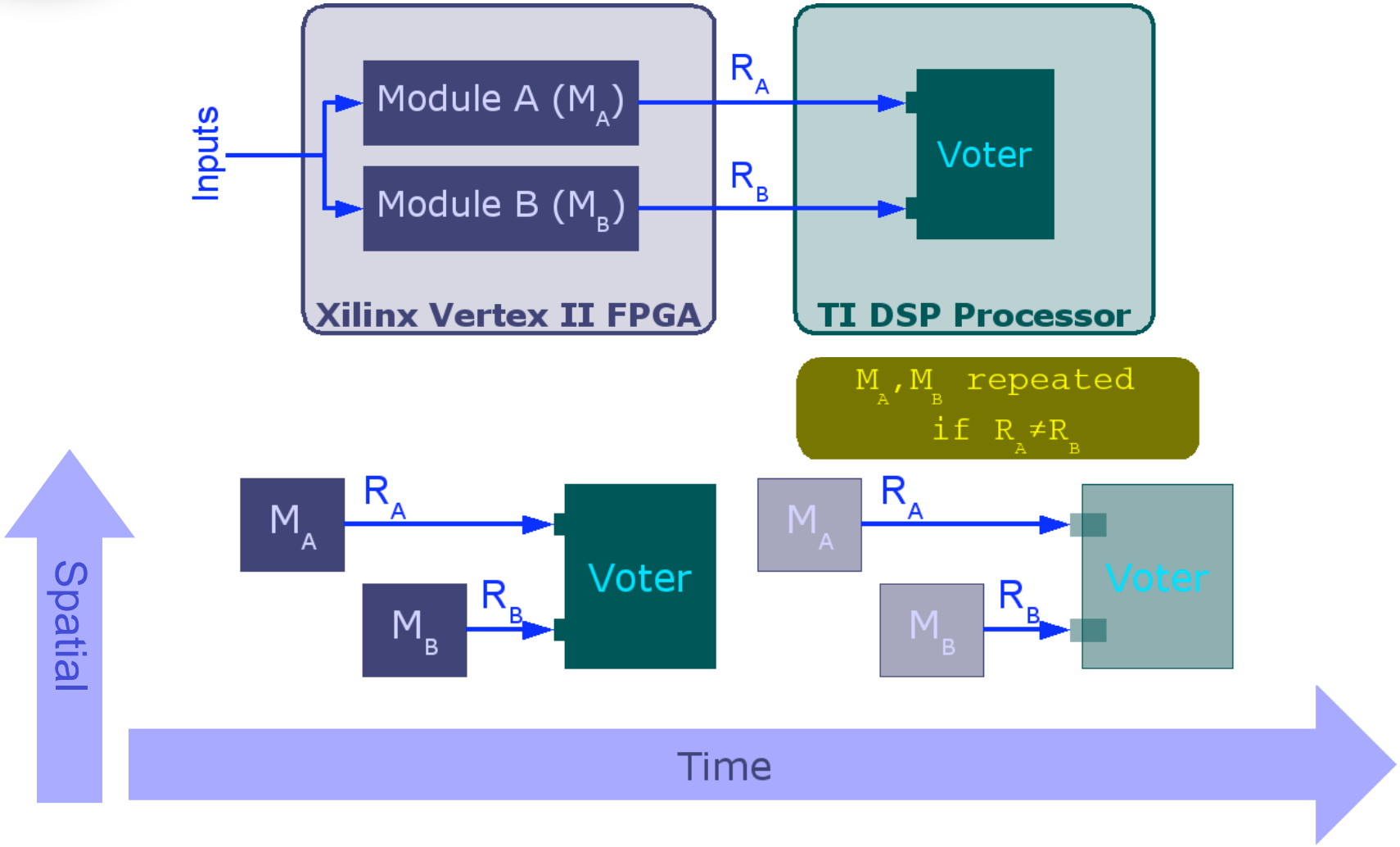


- TTMR™ Combines Time & Spatial redundancy
- Takes advantage of VLIW parallel opportunities
- SEU error rate equal to TMR rates
- SEFI is NOT fixed with TTMR
- Proton radiation tested at 51 MeV
- Detects & corrects SEUs

** Patent Pending **

TTMR for Reconfigurable FPGAs

Algorithm 1 – Dual Method

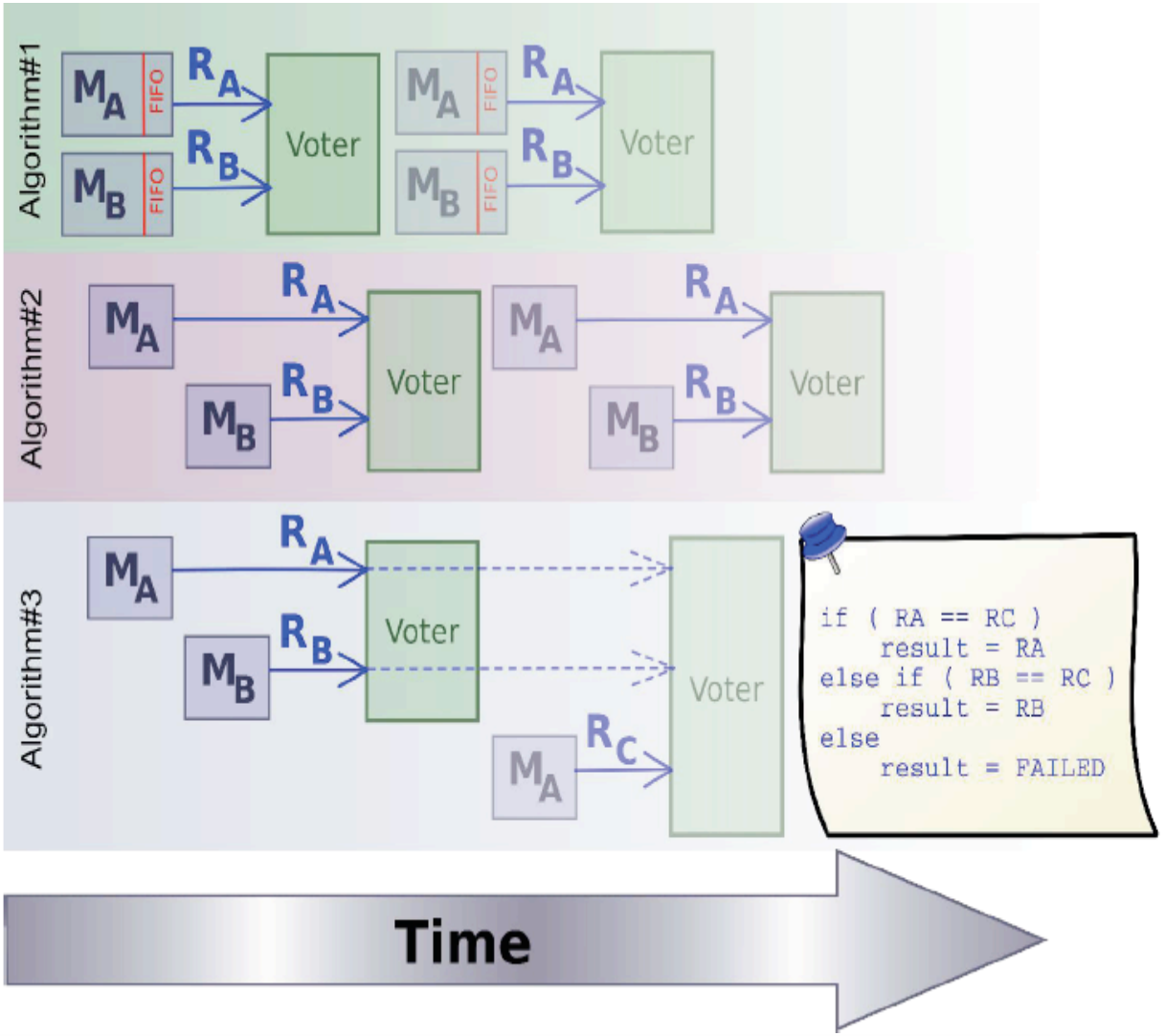


Multiple TTMR Algorithms

Algorithm 1 – Dual Method *with Checksum*

Algorithm 2 – Dual Method on *Per Instruction*

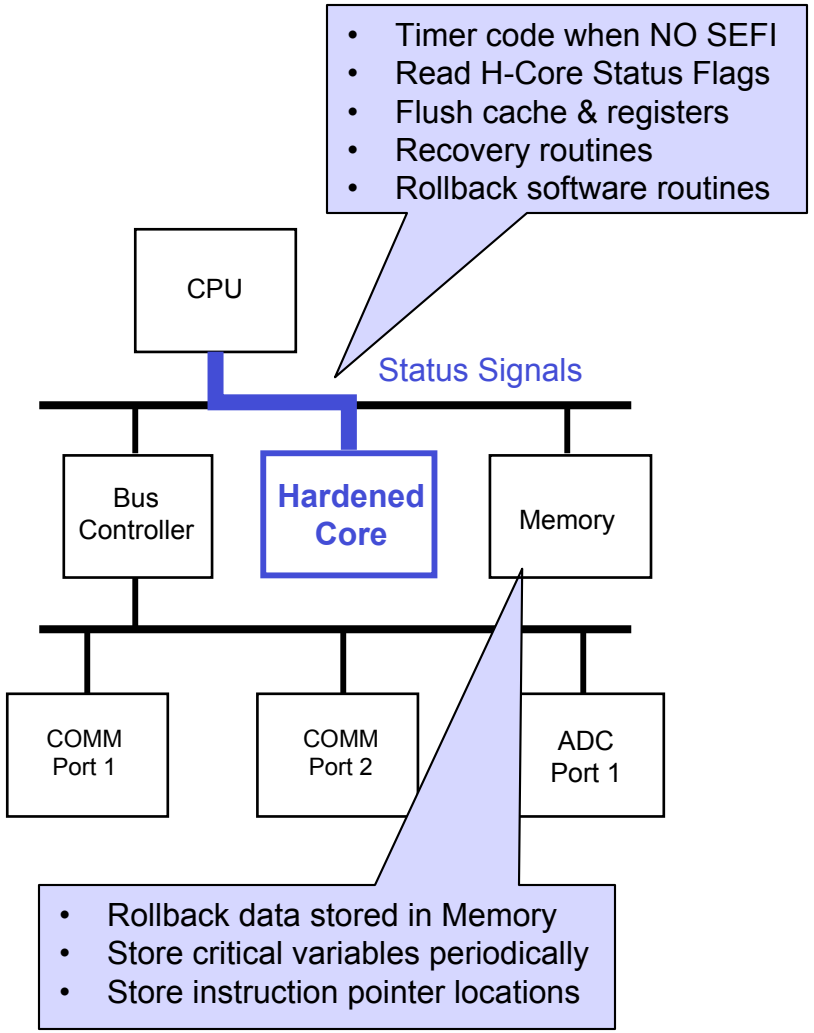
Algorithm 3 – Triple Method



SEFI Detection and Correction using Hardened Core™

- Hardware
  - **Rad Hard** external watchdog, sends interrupts and reset as required
- Software
  - CPU
    Generate health/status signals, run interrupt routines
  - H-Core IC
    Monitor signals, initiate post-SEFI recovery using Interrupts, and full reset as required

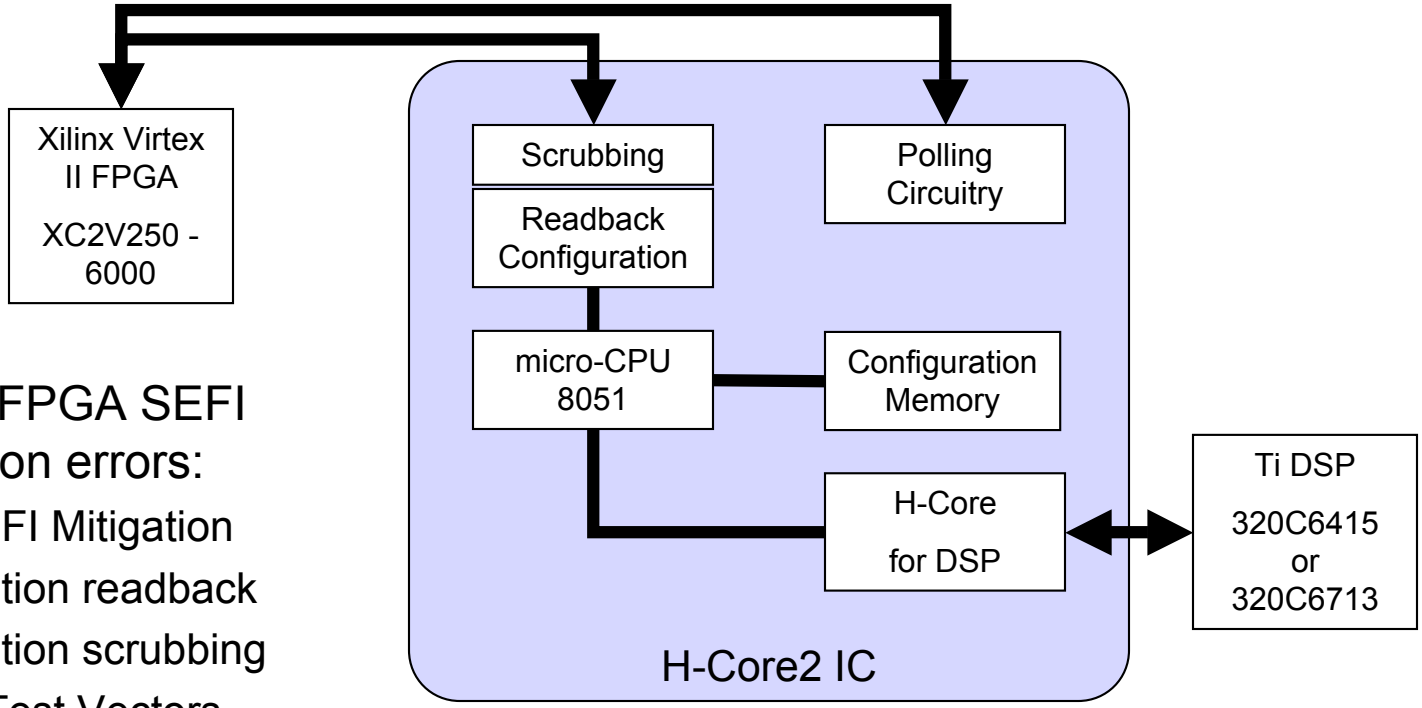
- Tested at UC Davis with 51 MeV Protons
  - Pentium III, BSP-15 and 320C6713 CPUs
- Summary Results:
  - >50 SEFIs induced
  - Many SEFIs return from IRQ & NMI
  - Reset brought back the rest
  - 100 % Recovery of SEFIs
- RESULT: SEFI Watchdog Proven with Protons



** Patent Pending **

H-Core2 SEFI Method for Reconfigurable FPGAs

Use Industry Standard Techniques to Fix SEFI & Reconfiguration

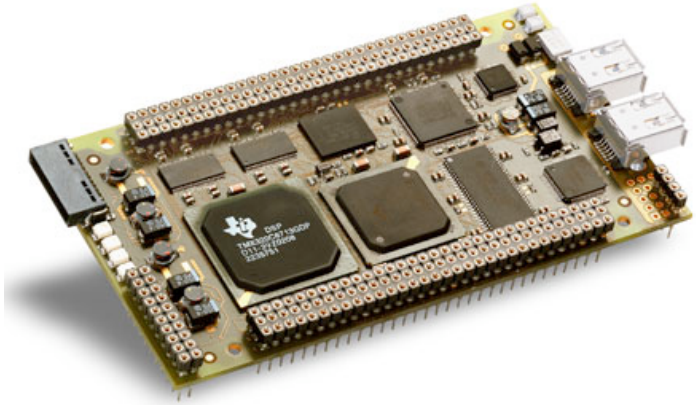


- H-Core2 for FPGA SEFI & configuration errors:
  - FPGA SEFI Mitigation
  - Configuration readback
  - Configuration scrubbing
  - Periodic Test Vectors
  - Signature Analysis

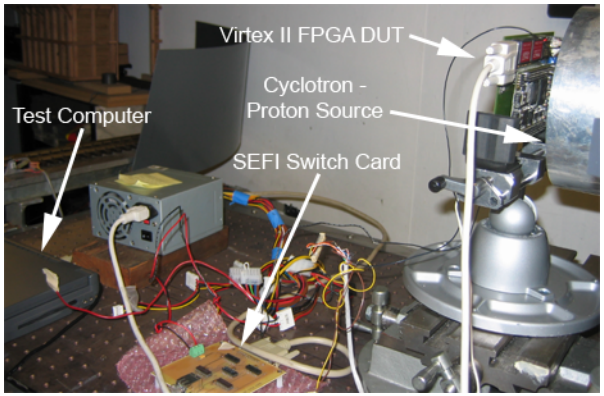
H-Core2 Integrated Circuit for DSP and FPGAs

Radiation Test of Virtex II FPGAs

- Xilinx Virtex II FPGA
  - XC2V250
- TI DSP used as Voter
  - 320C6713
- UC Davis Crocker Lab
- 63 MeV Proton source
- Virtex FPGA irradiated
- Short radiation test (4 hours) was run



Traquair C6713 Test Board

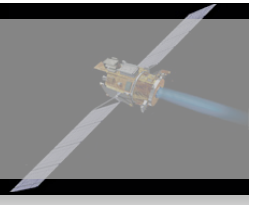


Test Setup at UC Davis

TTMR & H-Core2 Rad Test Data

- 32 different test sequences were performed
- Detection of SEUs was 100%
- 3 TTMR algorithms used
  - Dual redundant TTMR with a FIFO
    - 7 of 7 sequences were successful
    - 2 sequences had too many SEUs, overflowing SEU counter
  - Dual redundant TTMR (no FIFO)
    - 13 of 13 sequences detected SEUs
    - All sequences overflowed SEU counter
  - Triple redundant TTMR
    - 12 of 12 sequences detected SEUs
    - 12 of 12 sequences corrected SEUs
- Limited H-Core2 testing, but some SEFI mitigation was successful
- Initial Proton radiation test results were successful

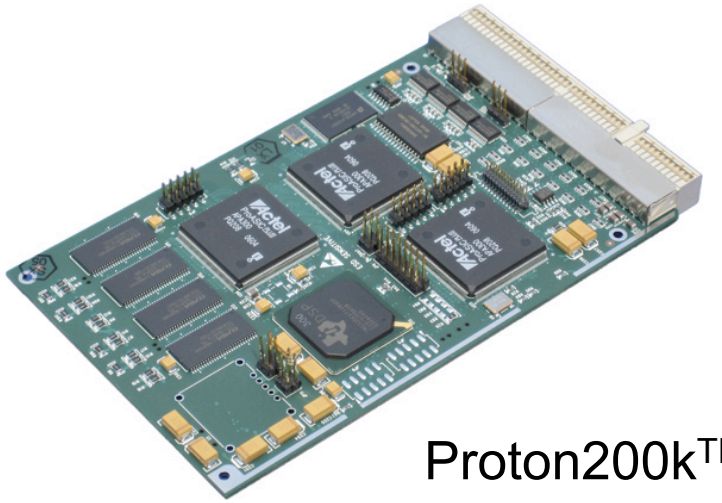
TTMR and H-Core2 Benefits



- Can use a single FPGA for fault tolerance (3 FPGAs are not req'd)
- A Reconfigurable Voter (DSP) is of great value
  - Reconfiguration is much more difficult with a fixed, rad hard ASIC
  - DSP is only 1.7 W at full speed, can provide additional processing (4,000 MIPs or 900 MFLOPS) power
- Checksum solutions provide much higher performance
  - Example: Run 1 million encryption cycles at full speed, calculate checksum with logic and send checksum to DSP
  - Speed Overhead: 10 DSP cycles every 1 million clock cycles (0.001%)
  - Logic Overhead: Dual TTMR = 2.1 times; Triple TTMR = 3.1 times
- TTMR Algorithm types provide multiple algorithms for fixing SEU problems in reconfigurable FPGAs
  - Apply best algorithm to problem
  - Minimize gate count (Dual) or impact to system performance (Triple)
- Implements the good work done by others (JPL, LANL, Xilinx …) for SEFI and reconfiguration into a rad hard H-Core2 ASIC

Implementing Reconfigurable FPGAs

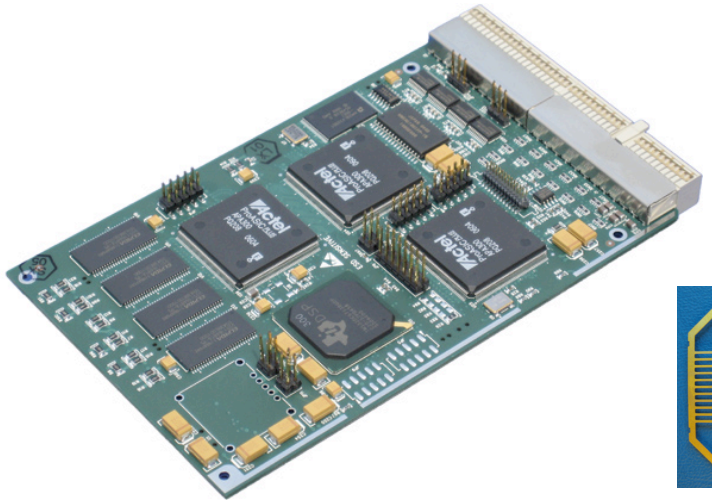
- Proton200k™
  - 32-bit DSP
  - 4,000 MIPS
  - SEU rate of < 1E-4 /day
  - >100 krad (Si) TID
  - No unrecoverable SEFIs
  - SEL Immunity >70 LET
  - Power: 5-7 watts



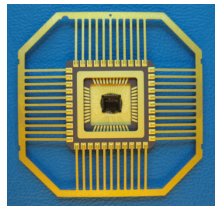
Proton200k™

Implementing Reconfigurable FPGAs

- Proton300k™
  - 6 to 24 M reconfigurable FPGA gates available for user programming
  - 32-bit DSP
  - 4,000 MIPS
  - SEU rate of < 1E-4 /day
  - >100 krad (Si) TID
  - No unrecoverable SEFIs
  - SEL Immunity >70 LET
  - Power: 5-7 watts



Proton200k™



H-Core2™

XILINX®

Proton300k™

Summary

- TTMR can correct SEUs in reconfigurable FPGAs
- H-Core2 can correct SEFIs and reconfiguration problems in reconfigurable FPGAs
- Space Micro radiation tested TTMR & H-Core2 with protons at UC Davis
  - Results showed detection and correction of SEUs in Virtex II FPGAs
  - SEFIs corrected with H-Core2
- DSP provides a reconfigurable voter & additional processing
- Enables high reliability Xilinx Virtex FPGA platform
- More work is needed to finalize these methods