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RF Architecture for Communication, Navigation, and Remote-Sensing with Software-Defined Radio

Contributors

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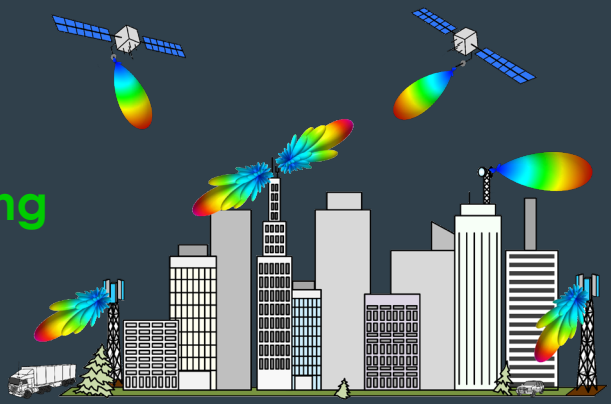
Overview

- Motivations
- Architectures
- Proposed Architecture
- Developed Approach
- FPGA Resilience
- Conclusions

Motivations

- Rapid growth of SmallSat and CubeSat missions has necessitated **re-evaluation** of large satellite **RF architectures**
- Slow adoption of new technology has limited Software-Defined Radio (SDR) for space applications where commercial world has seen widespread adoption
  - 4G/5G cellular networks
  - Internet of Things
  - Remote sensing

Internet of Things

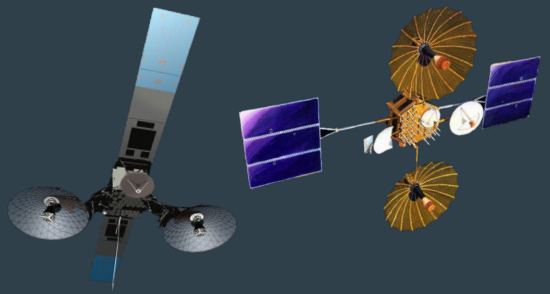


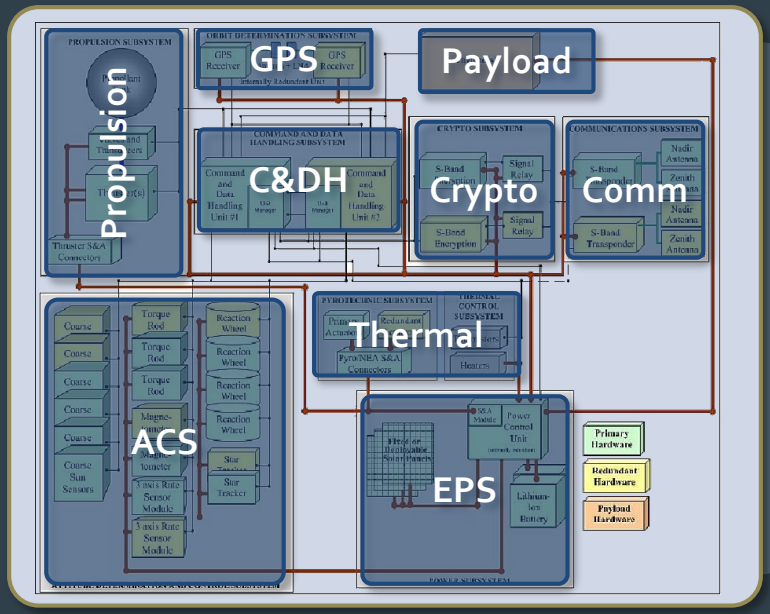
- Robust, reliable, high-performance, and efficient radios have been specifically identified as **enabling** NASA **technology** for future development
  - Small Satellite Missions for Planetary Science
  - Visions and Voyages planetary science decadal
  - 2015 Technology Roadmap & 2020 Technology Taxonomy

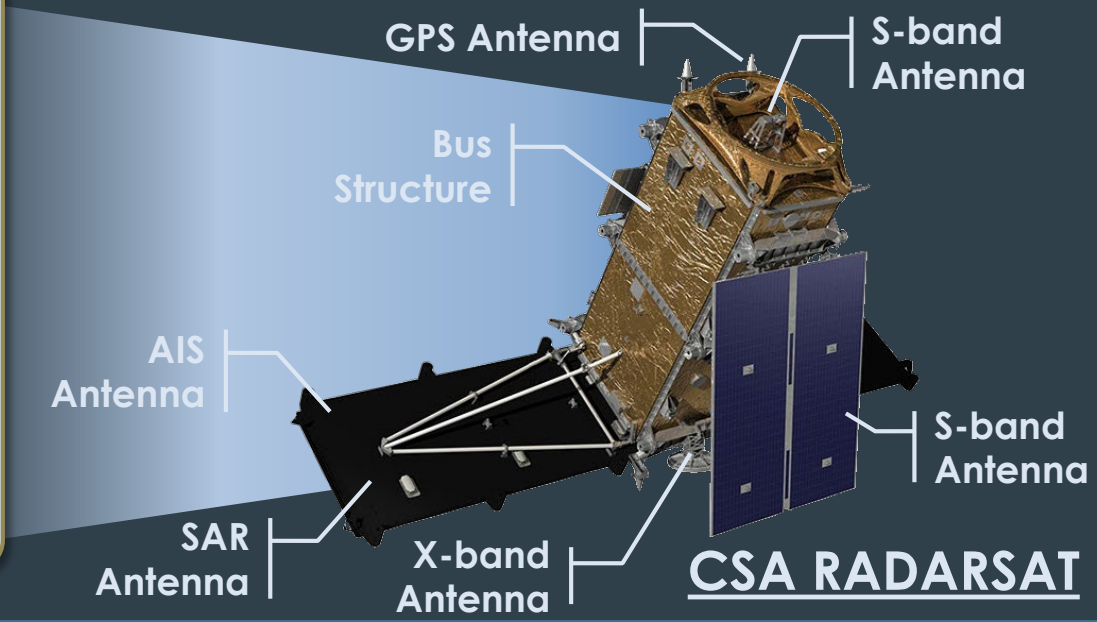
Large Bus Architectures

- Large satellites have **complicated** bus architectures with **high power** requirements resulting from multiple payloads, long mission durations, and internal redundancy
- Communication and remote-sensing systems share common functionality but are designed independently due to disaggregated architecture that leads to **sub-optimal** SWaP-C

NASA Tracking Data Relay Satellite (TDRS)

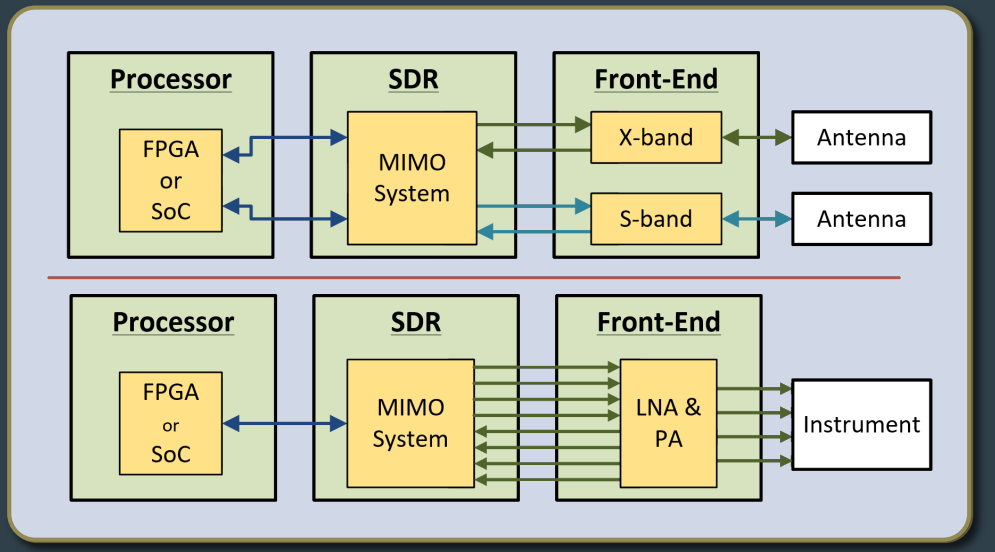




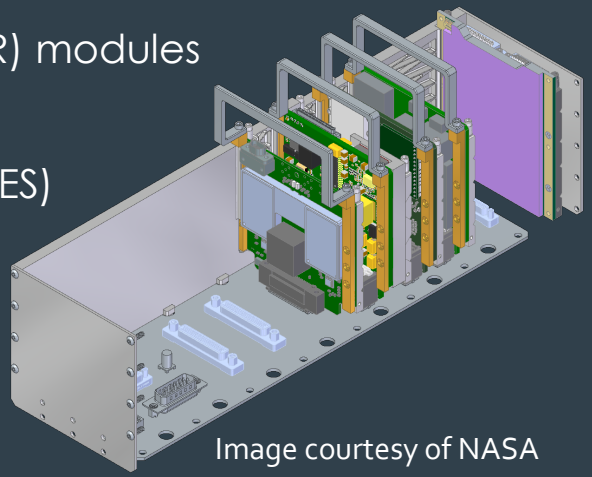


SmallSat Architectures

- Rapid growth of SmallSat and CubeSat missions has **necessitated re-evaluation** of large satellite systems
- Single-Board Computers (SBC) enable **substantial computing resources** to service multiple functions within CubeSat
  - S-band and X-band communication
  - Remote Sensing
  - Navigation and Ranging
  - Beamforming Applications



- RF systems can be replaced by software-defined radio (SDR) modules and provide comparable **functionality** and **performance**
- Modular Architecture for Resilient Extensible SmallSats (MARES) developed at NASA Goddard
  - Highly reliable and flexible architecture to support 3U, 6U and 12U bus configurations
  - Cornerstone is large Xilinx Kintex UltraScale FPGA for instrument processing, communication, and navigation



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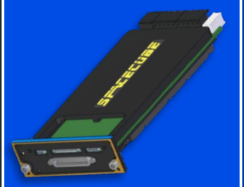
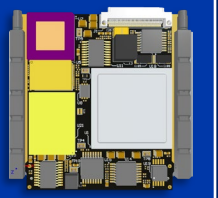
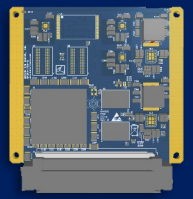
Hybrid Space Processors

- Removing on-board processors and FPGAs from individual subsystems allows for **hardware-agnostic designs**
- FPGA partial reconfiguration provides single interface between front-end RF systems and enable broad range of applications
- Enables optimal SDR layout without complications resulting from onboard processor
  - Noisy Regulators
  - Increased Power Efficiency
  - Higher Reliability Components
- Spacecraft designers can fine tune accompanying SBC to best meet mission requirements
  - Multi-card backplane interface
  - Onboard FMC interface

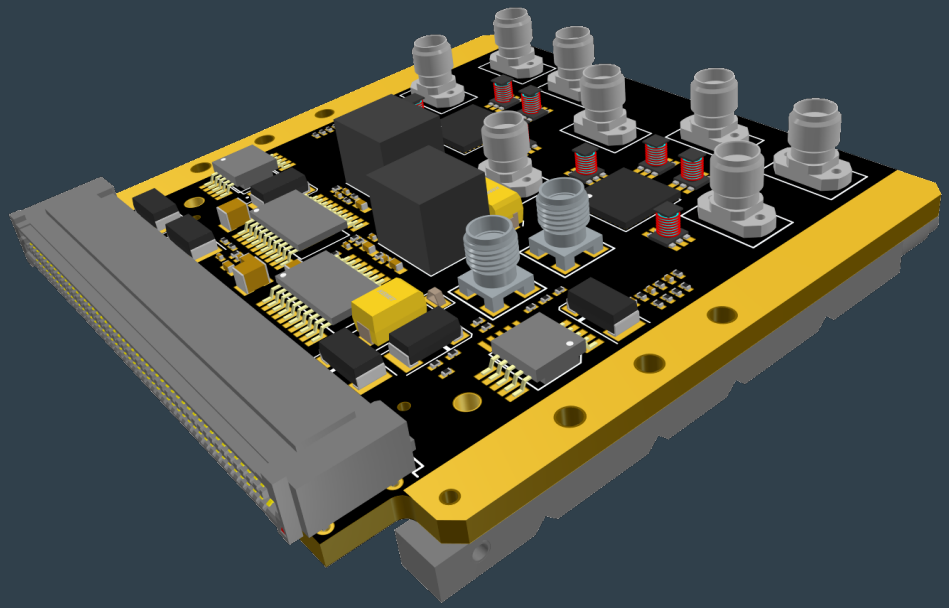
	SpaceCube v3.0 VPX (SC3-VPX)	SpaceCube v3.0 Mini (SC3-M)	SHREC Space Processor (SSP)
			
Form Factor	3U SpaceVPX	CubeSat Card Standard (CS2)	1U
Storage	48 GB	32 GB	4 GB
Memory	4 GB DDR3	2 GB DDR3	1 GB
Processor	Quad ARM Cortex-A53	MicroBlaze / RISC-V	Dual ARM Cortex-A9
MGTs	40 Lanes (12.5 Gbps / Lane)	12 Lanes (12.5 Gbps / Lane)	8 Lanes (10 Gbps / Lane)
Connectivity	Backplane / FMC+	Backplane	Backplane
Reconfigurability	+++	++	+
Power	+++	++	+
Cost	+++	++	+

Evaluating SDRs and Radios

- Industry has adopted disaggregated communication architecture
  - Many SDRs not suitable outside LEO orbit or have non-optimal noise performance
  - Radios provide higher reliability with limited reprogrammability
- Next generation of SmallSat missions require both reprogrammability and reliability

	Frequency	Bandwidth	Resolution	MIMO TX × RX	Radiation (Estimated)	Processor	Size / Weight	Peak Power RF Transmit
GOMspace NanoCom	70 MHz - 6.0 GHz	56 MHz	TX: 12-bit RX: 12-bit	4 × 4	20 krad -	Zynq 7030	9.0 × 6.6 × 3.1 cm^3 350 g	15.1 W 8 dBm
Rincon AstroSDR	70 MHz - 6.0 GHz	56MHz	TX: 12-bit RX: 12-bit	2 × 2	25 – 50 krad 52 MeV·cm^2/mg	Zynq 7045	9.0 × 9.0 × 1.6 cm^3 95 g	30 W 8 dBm
Cesium SDR-1001	300 MHz - 6.0 GHz	100 MHz	TX: 14-bit RX: 16-bit	4 × 4	20 krad -	Not Listed (FPGA)	8.7 × 5.0 × 1.3 cm^3 100 g	14.0 W 7 dBm
SpaceMicro µSDR-C	150 MHz - 6.0 GHz	56 MHz	TX: 12-bit RX: 12-bit	1 × 1	50 / 100 krad 70 MeV·cm^2/mg	Zynq 7020	10.0 × 10.0 × 5.0 cm^3 600 g	15.5 W 8 dBm
JPL Iris V2.1	X-band	TX: 256 kbps RX: 8 kbps		3 × 2	5 krad / 15 krad 37 MeV·cm^2/mg	Virtex 6 (LEON3)	10.0 × 10.0 × 5.6 cm^3 1.2 kg	35 W 36 dBm
IQ SpaceCOM X-Link	X-band S-band (Rx)	TX: 25 Mbps RX: 64 kbps		2 × 2	-	-	9.5 × 6.5 × 2.8 cm^3 200 g	15 W 27 dBm
Vulcan NSR-SDR-S/S	S-band	TX: 2 Mbps RX: 256kbps		1 × 1	-	-	9.2 × 8.2 × 3.4 cm^3 -	15 W 36 dBm
SDL Cadet Plus	S-band	TX: 3.2Mbps RX: 50 kbps		1 × 1	-	-	10.0 × 10.0 × 2.8 cm^3 630 g	8 W 33 dBm

Approach



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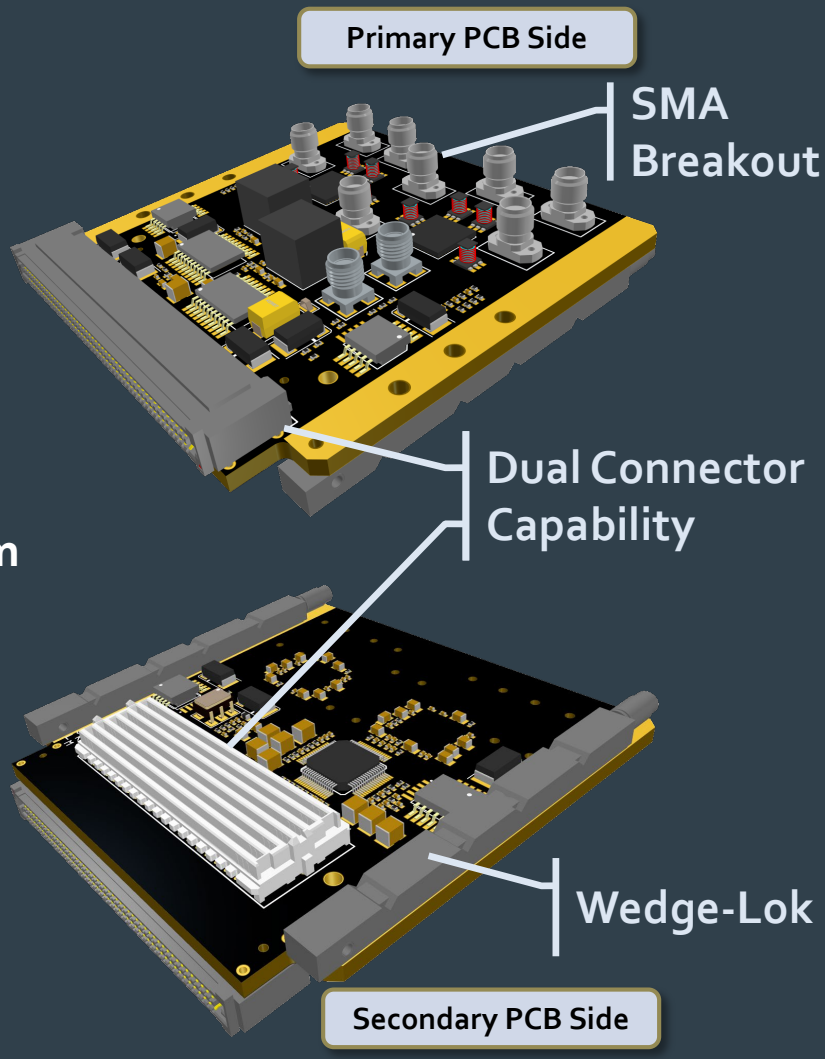
SDR Specifications

- **Dual phase-synchronized Analog AD9361**
  - Internal, on-board, and external **wideband** fractional–N PLL synthesizer
  - **4 × 4 MIMO** configuration and simultaneous control of individual channels
- **Operating frequency from 70 MHz to 6 GHz**
  - 12-bit ADC and DACs
  - Up to **56 MHz channel bandwidth**
- **High-efficiency noise-optimized power system**
  - Remote Sensing: 12W
  - Communication: 5W
- **1U CubeSat Card Standard (CS^2) form-factor**
  - FMC and backplane connector options
  - **Modular capability** with wide range of processors
- **High-reliability component selection and extensive TID and SEL radiation testing**



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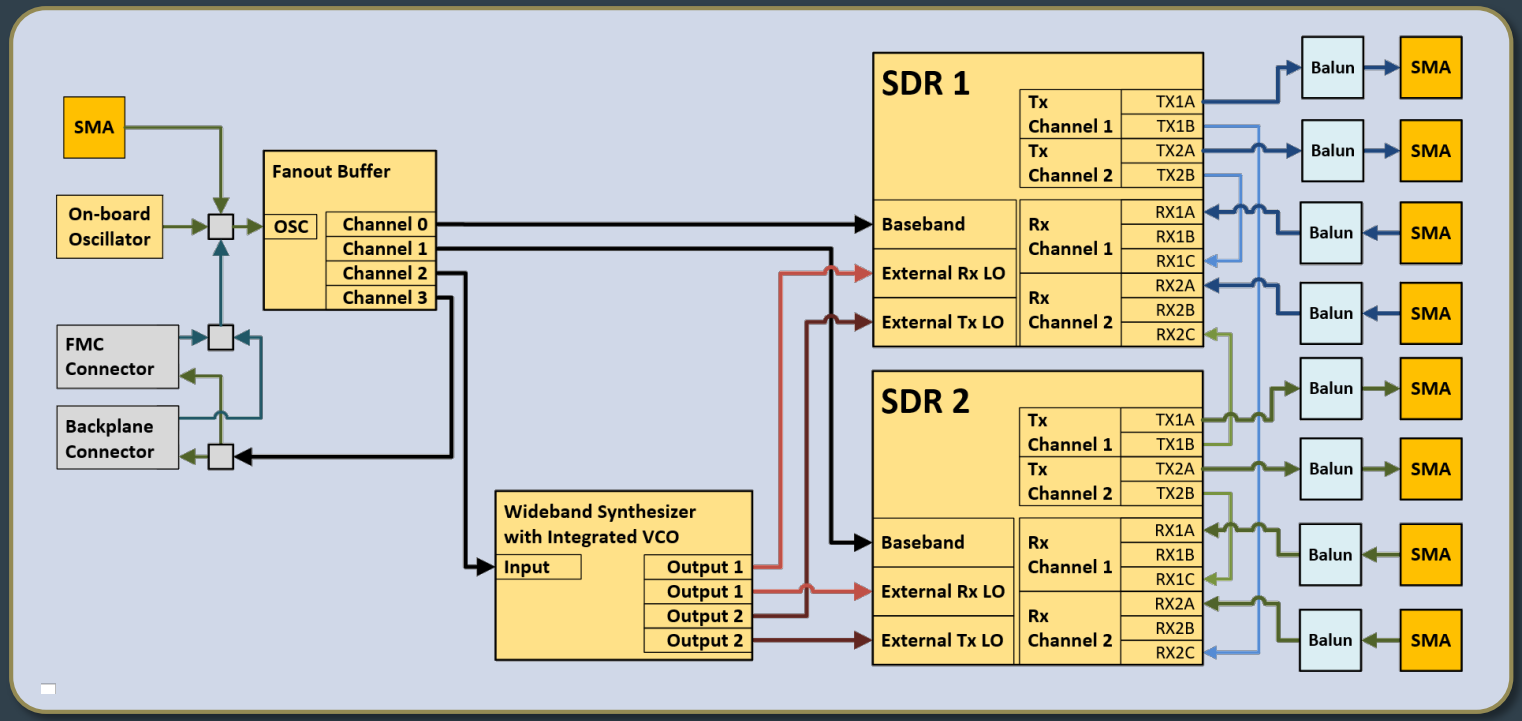
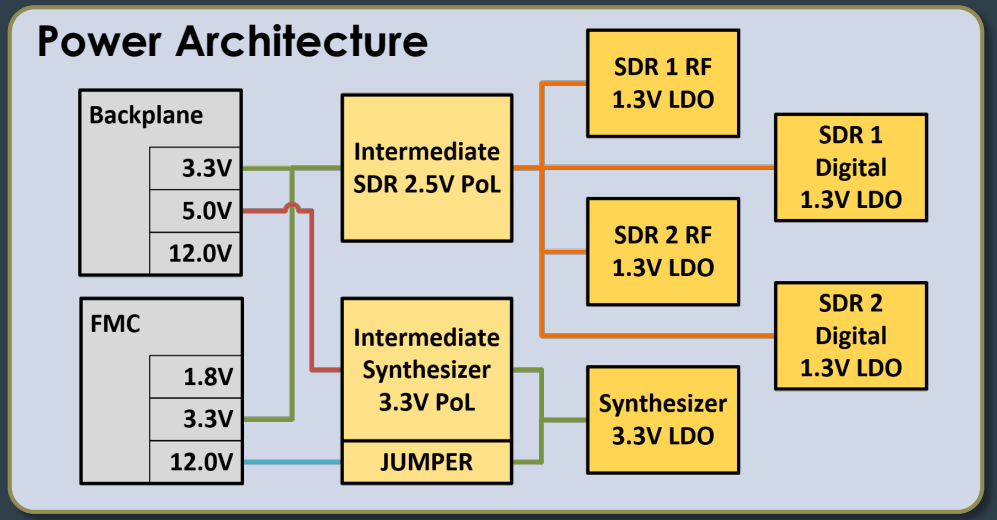
SDR and Synthesizers

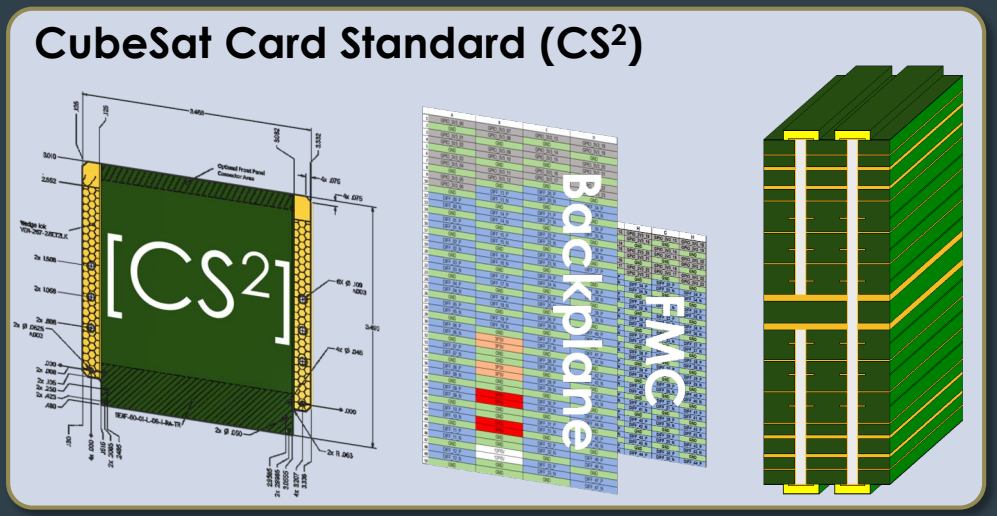
- Hybrid SDR Architecture
  - 4×4 MIMO architecture with baluns and SMAs with RF loopback for **phase coherence**
  - Communication to each AD9361 through 18 LVDS pairs providing highest throughput
- Baseband and RF Synthesizer
  - Baseband operation from 715 MHz to 1.43 GHz
  - Selectable **internal and external synthesizer** configurations to allow synchronization depending on mission requirements



Power and PCB

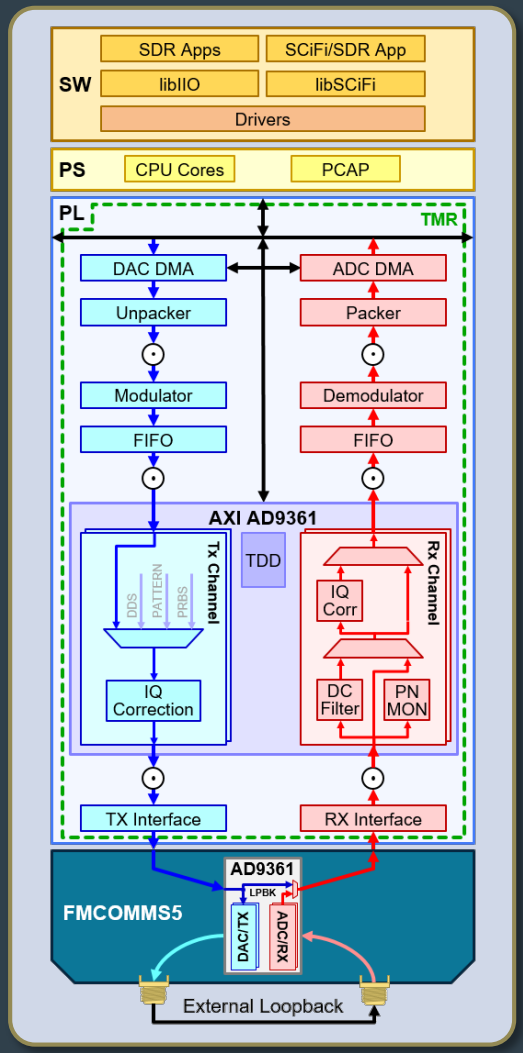
- Power System
  - SmallSat bus architecture must be considered in its entirety and commercially available bus architectures providing 12V, 5V, and 3.3V rails
  - Mixture of linear and point-of-load regulators provide **efficient conversion** and **low-noise** on supply voltages
  - **Selective regulator population** with rad-hard or rad-tolerant components enables variety of mission environments and cost constraints
- CS² Standard and Connector
  - **1U (10 cm × 10 cm) PCB** and connector pinout from CS² for modular system level design
  - Mechanical mount to chassis through either Wedge-Lok or Wedge-Tainer options
  - Class 3DS 22-layer PCB stackup with blind vias
  - Selective connector population for testing and flight capabilities on same hardware
  - FMC provides **test-as-you-fly** functionality to increase confidence in SW/HW stack





HW/SW Stack

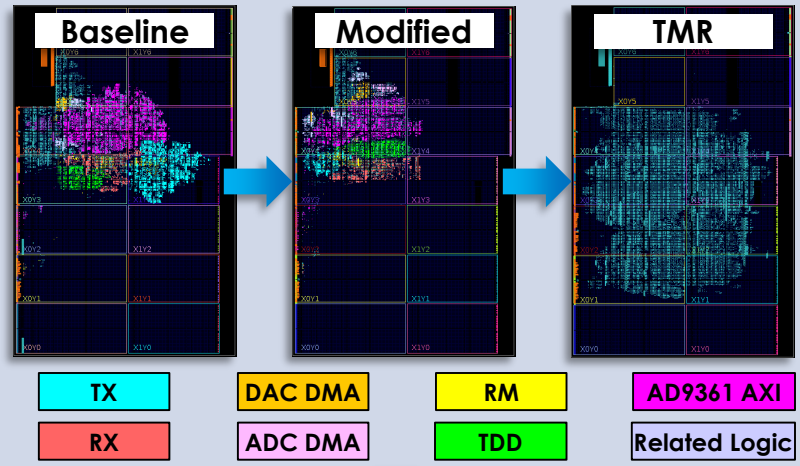
- Operation of each AD9361 requires full **hardware / software (HW/SW) stack**
  - Integration of System-on-Chip (SoC) architecture provides required performance and reconfigurability
  - Development platforms based on Xilinx Zynq-7000 SoC and Zynq UltraScale+ MPSoC
  - FPGAs implementation through SW stack on softcore processor including MicroBlaze or RISC-V
- FPGA HW stack includes:
  - AXI bus for AD9361 control
    - ADC/DAC processing
    - Delay and TDD
    - Device status and control
  - ADC/DAC DMA, packing, and FIFOs
  - Configurable modulation schemes



FPGA Resilience

- FPGA mitigation of radiation effects
  - Apply **Triple-Modular Redundancy (TMR)** and **configuration scrubbing** to improve dependability of HW stack
- Procedure
  - Modify reference design to remove non-essential logic
  - Leverage BL-TMR tool for selectively replication of designs at post-synthesis stage to apply fine-grain TMR to modified design
  - Validate operation of SDR with TMR design
- Evaluation framework
  - Developing framework and methodology for **evaluating FPGA-based SDR designs** through fault-injection
  - Enables formulation of trade-space in terms of performance and dependability
  - Enables development of selective and adaptive strategies for **efficient mitigation**

ZC706/FMCOMMS5 Reference Design



Resource Utilization

	LUTs (218k)	FFs (437k)	BRAM (545)	DSPs (900)	CRAM (846k)
Baseline	10.32%	8.56%	1.83%	7.22%	6.47%
Modified	4.99%	4.98%	1.47%	4.44%	3.68%
TMR	21.87%	14.92%	4.40%	13.33%	13.23%

Conclusions

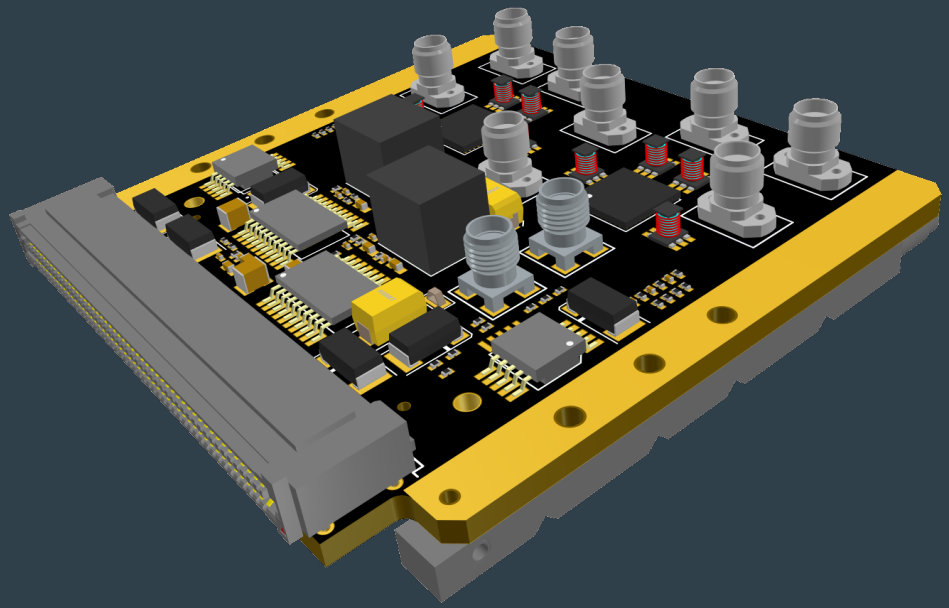
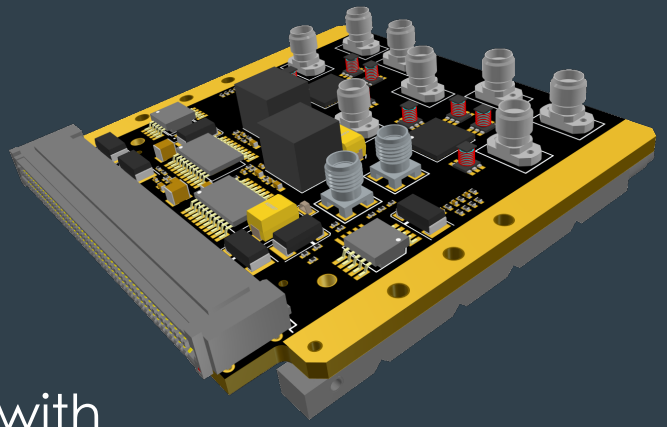
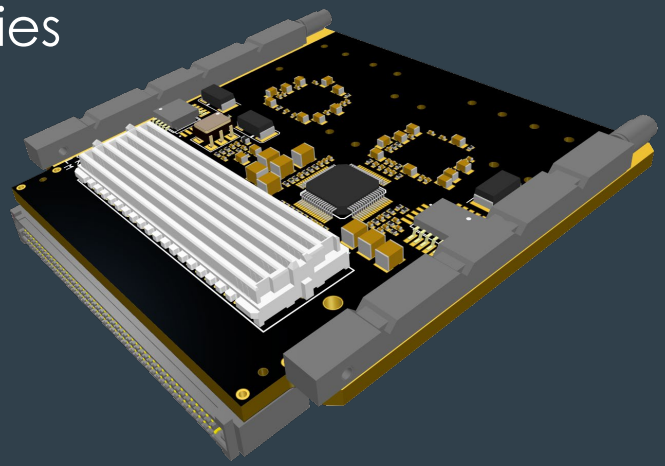


Image courtesy of NASA

Conclusions

- Rapid growth of SmallSat missions has necessitated **re-evaluation** of large satellite RF systems
- Proposed SDR architecture leading to **new generation** of SmallSat missions with tightly integrated remote-sensing, communication and navigation capabilities
- Presented SDR design framework for SWaP-C optimized SmallSat bus
- Provides **reliability** for current missions and **performance** for future **AI systems**





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