

CASPR: Autonomous Sensor Processing Experiment for STP-H7

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ABSTRACT

As computing technologies improve, spacecraft sensors continue to increase in fidelity and resolution, their dataset sizes and data rates increasing concurrently. This increase in data saturates the capabilities of spacecraft-to-ground communications and necessitates the use of powerful onboard computers to process data as it is collected. The pursuit of onboard, autonomous sensor processing while remaining within the power and memory restrictions of embedded computing becomes vital to prevent the saturation of data downlink capabilities. This paper presents a new ISS research experiment to study and evaluate novel technologies in sensors, computers, and intelligent applications for SmallSat-based sensing with autonomous data processing. Configurable and Autonomous Sensor Processing Research (CASPR) is being developed to evaluate autonomous, onboard processing strategies on novel sensors and is set to be installed on the ISS as part of the DoD/NASA Space Test Program – Houston 7 (STP-H7) mission. CASPR features a flight-qualified CSP space computer as central node and two flight-ready SSP space computers for apps execution, both from SHREC, a telescopic, multispectral imager from Satlantis Inc., an event-driven neuromorphic vision sensor, an AMD GPU subsystem, and Intel Optane phase-change memory. CASPR is a highly versatile ISS experiment meant to explore many facets of autonomous sensor processing in space.

I. INTRODUCTION

Throughout the space community, there is a growing need for smaller satellites with onboard capabilities for autonomy in sensor processing and controls. In 2016, the National Research Council (NRC) identified CubeSats and more broadly small satellites (SmallSats) as a major innovation for future space science missions [1]. The NRC concluded that CubeSats excel at simple, short-duration missions that require low-cost development compared to their larger satellite counterparts. Similarly, they state that constellations of CubeSats have the potential to achieve the precision of large, monolithic satellites while enabling easier replenishment of the CubeSats over time as members in the constellation fail. Therefore, CubeSats have become more abundant in various sectors of the space community, shown by the NRC in Figure 1.

Given the advantages of CubeSats and other SmallSats, sensor technologies and downlink capabilities still present a distinct challenge for science mission success. There are two main paths to address this issue: improve downlink capabilities and reduce the amount of data that must be downlinked. Improving downlink capabilities is done by finding new ways to increase communication between space and Earth. For example, Sinclair and Riesing proposed using optical downlinks via laser signals for communication [2]. However, this

method is still limited by the physical capabilities of optical devices and signal integrity over long-distance communication. Ultimately, to further improve downlink capabilities, both paths need to be addressed in conjunction. Reducing the amount of data can be accomplished primarily through of onboard processing.

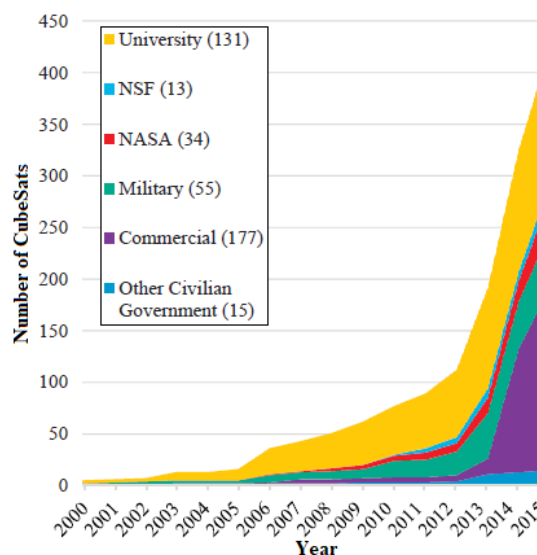


Figure 1: Cumulative Number of CubeSats Launched by Organization Type [1]

Onboard processing in SmallSats presents further challenges that need to be addressed. The challenge lies in the lack of space-qualified computing and sensing technologies to support big data at a small scale. Designs are restricted by size, weight, power, and cost (SWaP-C), limited processing capabilities, and redundancy considerations needed for space. As spacecraft sensors continue to increase in fidelity and resolution, both their data rates and the amount of data generated increase concurrently. This makes the practice of downlink and processing on the ground impractical or entirely infeasible. Instead, many are turning to the deployment of more advanced space computing solutions to allow onboard processing, decision making, and autonomy. This increases the capabilities of spacecraft while further reducing the cost, overhead, and human effort required for their operation.

To make modern spacecraft more autonomous, novel sensors need to be integrated with high-performance and reliable space computers to perform complex, onboard processing. With these advancements, the majority of sensor processing and analysis can be done onboard without the need to downlink large files. Therefore, future spacecraft can achieve an ideal form of compression: thorough answers and solutions in place of large, unprocessed dumps of data. To evaluate powerful computing technologies along with novel sensors, this paper introduces the Configurable Autonomous Sensor Processing Research (CASPR) experiment for the upcoming Space Test Program – Houston 7 (STP-H7) pallet launching to the International Space Station (ISS) in November of 2021.

CASPR is currently being developed by researchers at the National Science Foundation (NSF) Center for Space, High-performance, and Resilient Computing (SHREC) at the University of Pittsburgh in collaboration with SHREC partners. CASPR introduces two novel sensors, including a telescopic, low ground-sampled distance (GSD), and multispectral imager, a neuromorphic vision sensor, and new computing technologies for application acceleration in space. This paper describes the hardware, software, operational framework, and mission goals for CASPR.

II. BACKGROUND

This section provides an overview of the Space Test Program – Houston, the STP-H7 mission, and key concepts for the CASPR experiment. The sensors, space computers, and flight software are introduced, and design challenges are discussed.

Space Test Program – Houston 7

The Department of Defense (DoD) Space Test Program (STP) was established to provide affordable, timely, and efficient spaceflight opportunities for DoD space experiments to the ISS to advance on-orbit research and technology [3]. These opportunities provide the capability to fly multiple experiments with the expense of only one launch, resulting in high experimentation efficiency.

The STP-H7 pallet features several different experiments, including CASPR, from various institutions. The integration of the pallet is under the management of the DoD STP Human Spaceflight Payloads Office. The launch is currently expected for November 2021 situated on the SpaceX CRS-24 vehicle.

Radiation Environment

The radiative space environment presents difficult challenges for computer systems due to radiation. Radiation can manifest itself as transient faults called “single-event effects” (SEEs), as well as more long-term, cumulative effects. SEEs can be destructive (e.g., latchup, burnout, gate rupture, etc.) or nondestructive (e.g., upset, transient, functional interrupt, etc.).

Total-ionizing dose (TID) is the cumulative effect of radiation that describes the dosage of ionizing radiation over time [4]. Eventually, the device experiences a higher dose of radiative flux than its TID specification. This results in increased likelihood of permanent failures. Traditional radiation-hardened (rad-hard) processors are often used for their high TID and enhanced immunity to SEEs. However, these processors tend to be generations behind their commercial-off-the-shelf (COTS) counterparts in terms of performance and energy-efficiency while being much more expensive.

Hybrid Computing

Researchers at the NSF SHREC Center have established a concept for hybrid space computing [5]. The concept involves three main components. First, to attain multi-architectural advantages, a hybrid system-on-chip (SoC) with a CPU and an FPGA fabric is used. Second, mixing high-performance and energy-efficient commercial-off-the-shelf (COTS) technologies with rad-hard and rad-tolerant supporting circuitry for robustness gives a system with capable computing power that retains high reliability. Finally, to enhance reliability further, dependable-computing techniques are used in software. This idea has now been adopted on many space missions.

The hybrid SoCs used in CSP combine distinct computing architectures, such as an FPGA fabric and a CPU in tandem, to gain the advantages presented by each. FPGAs tend to benefit from data-stream-oriented applications, while CPUs are advantageous for general-purpose computing tasks. Combining this hybrid-processor architecture with dependable computing and hybrid component design leads to a capable and dependable space computer.

The first realization of this hybrid-computing concept was the CHREC Space Processor (CSP), shown in Figure 2. The CSP employs a Xilinx Zynq-7020 SoC with an Artix-7 Series FPGA fabric and dual-core ARM Cortex-A9 processor [5]. The system is designed around rad-hard power electronics to ensure long-term stability. Custom flight software has been developed to further improve the reliability of the space computer.

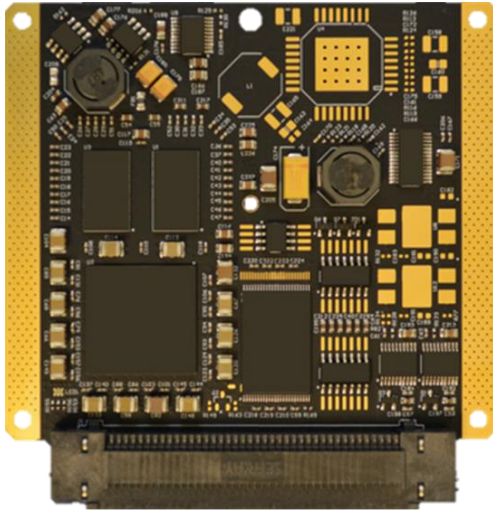


Figure 2: COTS CSP Rev. B (Engineering Model)

The CSP has been flown on two ISS missions to achieve a technology readiness level (TRL) of 9 and has been adopted on many industry and government missions as well. The STP-H5 pallet, currently installed on ELC-1 of the ISS since 2017, contains the STP-H5-CSP experiment. This payload features a dual CSP platform as a sub-experiment of the NASA ISS SpaceCube Experiment Mini (ISEM) [6]. The STP-H6 pallet, currently installed on ELC-3 of the ISS since 2019, contains the STP-H6 Spacecraft Supercomputing for Image and Video Processing (STP-H6-SSIVP) experiment. This system hosts a networked cluster of five CSPs for dependable, high-performance onboard computing [7].

The next generation of our hybrid space computing concept is the SHREC Space Processor (SSP). SSP employs a user-selectable Xilinx Zynq-7030 or -7045, both with a Kintex-7 FPGA fabric and a dual-core

ARM Cortex-A9 processor. The SSP is currently in development at SHREC and offers many advancements over the CSP, including multi-gigabit transceivers (MGTs) for high-speed communication, more than four times more FPGA resources, and dedicated FPGA-interfaced memory.

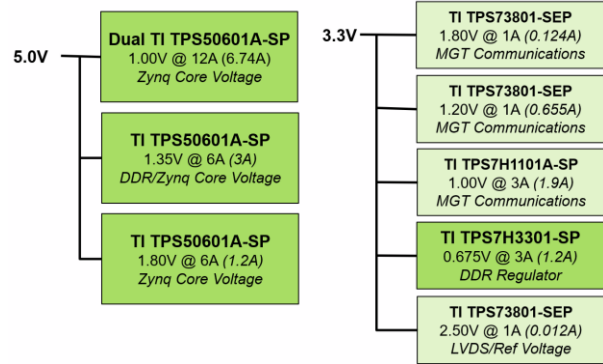


Figure 3: Rad-Hard Texas Instruments Power System of SSP

The hybrid version of the SSP uses Texas Instruments TPS50601A-SP [8] switched converters for the core voltages, TPS7H1101A-SP [9] and TPS73801-SEP [10] low drop out regulators for MGTs, and TPS7H3301-SP [11] DDR regulators for a full rad-hard power system solution shown in Figure 3. A render of the SSP can be seen in Figure 4.



Figure 4: COTS SSP Rev. A (Engineering Model)

μCSP Smart Module

A smaller, lower-power iteration of the CSP concept called the μ CSP was created to perform simple, modular functions [12]. The μ CSP is designed as a system-on-module (SoM), featuring a Microsemi

SmartFusion2 hybrid processor containing a fixed-logic, single-core ARM Cortex-M3 microcontroller and a reconfigurable IGLOO2 FPGA fabric. Similar to the CSP, the μ CSP uses the hybrid-system approach with a COTS processor along with rad-hard components for supplementation.

The μ CSP has flight heritage on STP-H6-SSIVP serving to independently control and monitor a gallium-nitride-transistor-based power sub-experiment. A picture of a μ CSP can be seen in Figure 5 with a U.S. quarter as a size reference.



Figure 5: μ CSP Smart Module

Satlantis iSIM90 Binocular Optics

The binocular optical sensor affixed atop the CASPR gimbal mechanism is the iSIM90, a multispectral imager designed and provided by the company Satlantis. The instrument contains two separate imagers and optical paths directed at the same point to enable synchronous capture of multiple spectra without the need for any moving parts to change a filter. The detectors featured on CASPR will be multispectral imagers with a near-infrared (NIR) broadband filter containing red and near-infrared colors for one imager and a visual (VIS) broadband filter containing blue and green colors for the other. The data flow for image capture can be seen in Figure 6. Based on the characteristics of captured images, many will need to be combined to achieve a high-quality frame, as illustrated in Figure 6. In order to achieve the desired framerate of 26 frames per second, a custom imager frame grabber is implemented in the FPGA of an SSP.

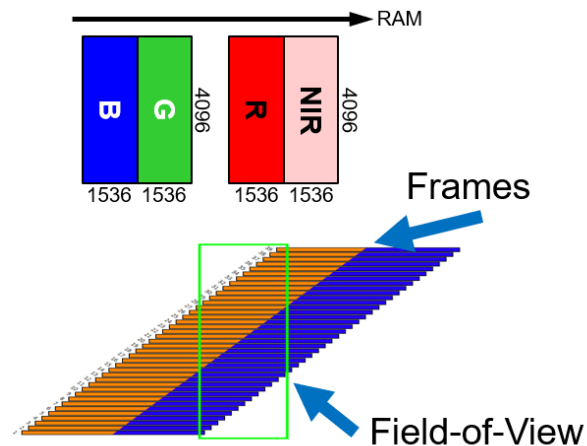


Figure 6: iSIM90 Camera Grid

The iSIM90 optics provide a low GSD, which is the ground distance between adjacent pixels of an image, while still maintaining a small form-factor. Specifically, the GSD of the Satlantis iSIM90 is designed to be less than two meters from an altitude of 500 kilometers for a 12-megapixel image. This low-GSD imagery will support advanced computer-vision and machine-learning applications for Earth observation.

Sysley Neuromorphic Vision Sensor

The second novel sensor that will be featured on CASPR is the Sysley neuromorphic vision sensor developed by the company Prophesee. Neuromorphic vision sensing is very different from conventional imaging in that it is event-driven as opposed to frame-based. Neuromorphic, event-driven sensors are based on biological vision systems and operate by integrating light intensity over time on a per pixel basis. This means that static, redundant background information is disregarded while only dynamic, changing information is passed from the sensor [13]. The reduction of irrelevant, static background information allows for a high framerate with a low data rate, enabling a more efficient use of onboard memory.

These sensors capture information along the time-axis in the form of “events” as opposed to the space-axis used in conventional cameras. Capturing visual information as a time series enables a high temporal resolution on the order of microseconds. This high time resolution enables the use of precise object-tracking and optical-flow applications.

III. CASPR HARDWARE

This section gives an overview of the hardware architecture for the CASPR system. The primary components of CASPR include the computing

infrastructure, the iSIM90 binocular optics, the Sysley neuromorphic vision sensor, the iSIM90 platform control Smart Module, the computing sub-experiments, the power control system, and the mechanical structure. Each component is detailed in one of the following subsections. An overview of the subsystems and their connections to a central backplane can be seen in Figure 7.

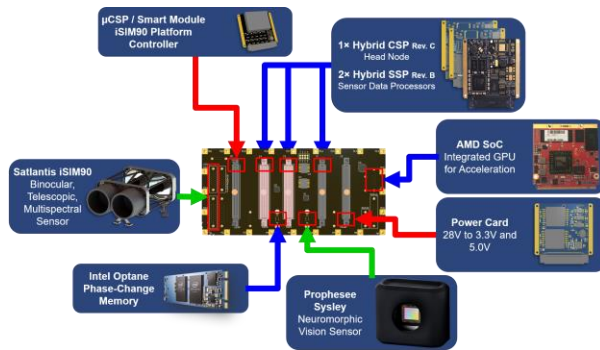


Figure 7: Electronic Hardware Layout for the CASPR Backplane

Computing Infrastructure

The primary mission objective for CASPR is to facilitate and demonstrate onboard, autonomous sensor processing leveraging a heterogeneous cluster of high-performance, fault-tolerant space computers. CASPR includes one hybrid CSP Rev. C computer serving as the system controller, providing an interface to the ISS and managing all other components. It is responsible for receiving, processing, and relaying commands, directing data between components, monitoring mission-critical sensors, and managing payload power states. CASPR also includes two hybrid SSP Rev. B computers serving as accelerators for sensor-data processing. These SSPs are linked via high-speed, high-bandwidth MGTs for effective, scalable parallel processing.

The AMD embedded GPU SoC acts as an additional accelerator for machine-learning and computer-vision (ML/CV) application acceleration and a platform for GPU-reliability experiments. The GPU is an entirely self-contained system but capable of offloading processing from the SSP. Intel's Optane PCM provides additional non-volatile storage for sensor data from the iSIM90 optics.

Thermal and Gimbal Control Smart Module

To ensure the low GSD of the iSIM90 and attain the highest possible image quality, the temperature of the optomechanics must be carefully maintained. This task is outsourced to the μ CSP-powered iSIM90 platform

control Smart Module. This subsystem is responsible for monitoring the temperatures of various points in the iSIM90 optics assembly. If any of the monitored regions are below the threshold for optics operation, individual heaters for those regions will be powered until temperature needs are met. Motor control and position tracking for the gimbal platform are also handled by this Smart Module. The gimble motor is a NEMA 11 vacuum rated stepper motor from LIN Engineering and is driven using two Renesas HS-4080AEH full bridge drivers. Several additional sensors, including a gyroscope and accelerometer, collect data about station orientation and vibrations induced by docking spacecraft or spacefaring occupants.

Sensor Experiments

The iSIM90 optics output a 12-megapixel image of four broadband spectra. This high-fidelity image data will be used to evaluate super-resolution application. Further, compression algorithms will be explored to reduce data size and address low downlink speeds. Furthermore, ML/CV applications will be applied to the images for various classification, segmentation, and data manipulation tasks. The optics will be directed at nadir and have a 1.5-degree field of view for Earth observation and will collect data in short bursts of 26 frames-per-second imaging.

Due to the event-driven nature of the neuromorphic sensor, neuromorphic vision systems excel at object tracking [14]. In CASPR, the neuromorphic sensor will be facing toward the horizon, 15-degrees towards starboard from ram with a 70-degree field of view. The sensor will be continuously streaming information for tracking any passing objects or debris to enable space situational awareness capabilities.

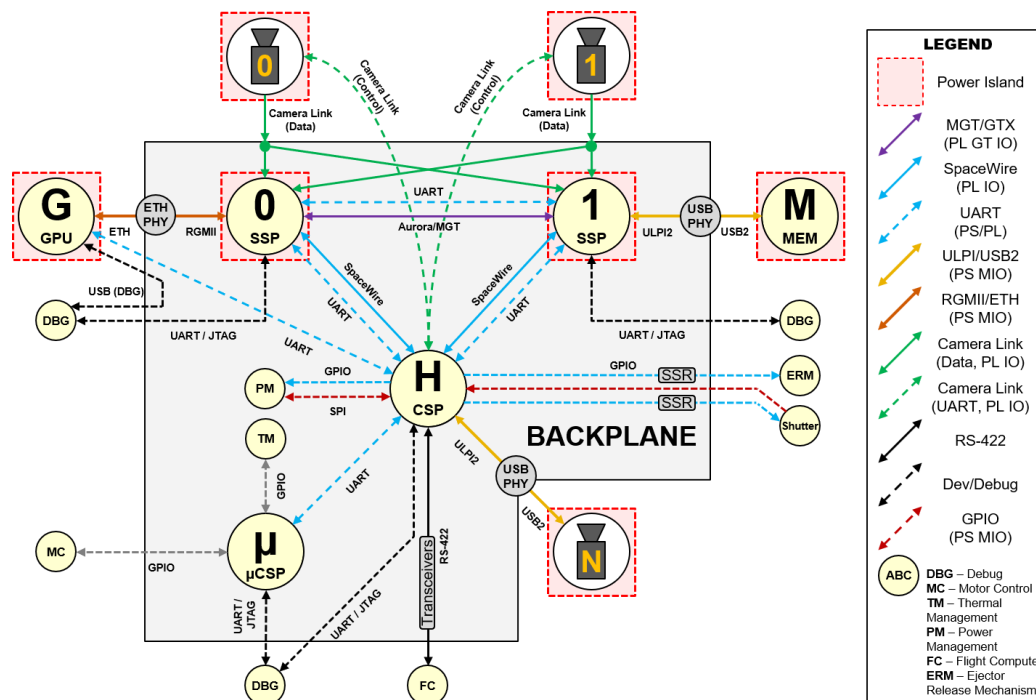
Computing Sub-Experiments

CASPR will also feature two additional space computing technology experiments as peripherals to the main electronics. The first sub-experiment uses an AMD G-Series GX-216HC SoC which combines a dual-core Jaguar x86 processor with integrated RadeonHD-8000 GPU. The GPU subsystem features a custom carrier card to enable interfacing to one of the SSPs via Ethernet. Dependable computing techniques will be demonstrated in software to increase the reliability of the data and operating system. This sub-experiment will evaluate the GPU's ability to perform in the radiative environment of ISS orbit. Furthermore, this sub-experiment will be used to accelerate machine-learning and computer-vision applications with the additional compute capability of the GPU.

A photograph of a custom PCB layout for a Raspberry Pi 4. The board is populated with various components, including the SoC (System on Chip), RAM modules, and power connectors. The layout is shown in a top-down view, with components labeled with their respective part numbers and functions.

Figure 8: CAPSR Backplane Model

All CASPR subsystems communicate with the CSP head node. All commands and operations will be handled through the CSP. A detailed diagram of the system architecture can be seen in Figure 9.



each camera from the CSP head node. The GPU is connected to one SSP via Ethernet and to the CSP via UART. The PCM is connected to the other SSP via USB. Based on this configuration, in the unlikely scenario of a loss of one SSP, only one sub-experiment is lost, and the primary imagers will remain operational. A UART connection is used to link the CSP with the μ CSP, and GPIO on both are used for power management, thermal management, and motor control. Finally, an RS-422 connection is used to interface CASPR to the STP-H7 pallet for ground

communications. While the CSP head node represents a single point of failure, its high TRL, flight-proven status, and supplementary mitigations incorporated into the design serve to minimize risk.

Mechanical Structure

CASPR's mechanical structure is divided into two major assemblies, with the top half consisting of the iSIM90 vision system and the bottom half consisting of the avionics chassis. A gimbal platform connects both assemblies. A design render of the CASPR experiment system can be seen in Figure 10.

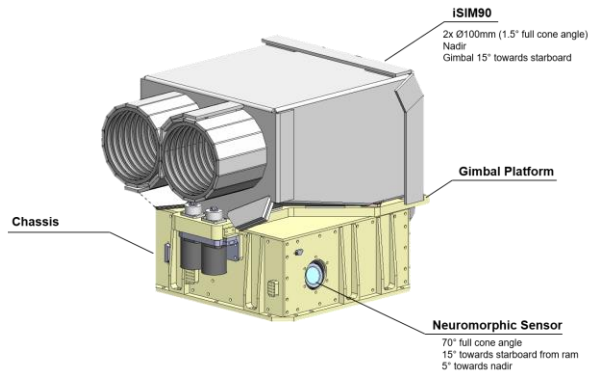


Figure 10: Computer Rendering of CASPR

The bottom chassis contains all the electronics and the neuromorphic vision system. Dual redundant ejectors visible as cylinders at the front of the electronics box serve to secure the gimbal platform for launch and pallet installation. Data and power connectors protrude from the side of the chassis to connect to the STP pallet. The layout of the internal components of the electronics box can be seen in Figure 11.

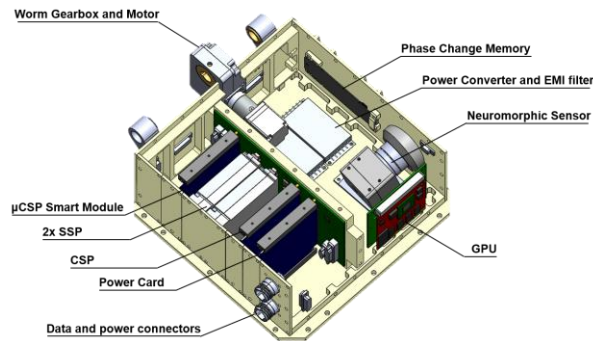


Figure 11: Computer Rendering of Electronics Chassis

Due to the low GSD and resulting small field of view of the binocular optics, a gimbal mechanism has been designed to increase the field of regard and reduce the revisit time of points of interest for imaging. The gimbal allows 15 degrees of cross-track movement

facing starboard from the ISS, significantly increasing the 1.5-degree cone-angle field of view of the optics, seen in Figure 12. Therefore, the gimbal works in conjunction with the binocular optics to achieve a much larger field of regard while still maintaining the low-GRD benefits of the optics.

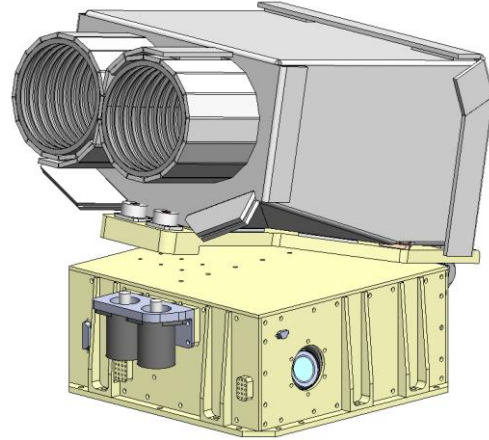


Figure 12: Computer Rendering of CASPR with the Gimbal Platform Fully Open

IV. CASPR FPGA, SOFTWARE, AND OPERATIONS

This section describes the software design and mission operations for the CASPR experiment. The experimental applications, FPGA network architecture, and modes of experiment operation are also discussed.

Flight Software

Both the CSP and SSP run Wumbo Linux, a custom operating system based on Xilinx's Linux kernel fork and BusyBox userland, developed using buildroot. NASA Goddard Space Flight Center's Core Flight Executive and Core Flight System (cFE/cFS) run on Wumbo to enable commanding, telemetry, and other functionality. In Wumbo, an initramfs paradigm is used to create a temporary in-memory filesystem that is restored on reset. A persistent file system is used on the onboard NAND flash to store data, logs, and uplinked files.

The flight images of the operating system contain cFE/cFS frameworks and applications for platform-independent and reusable flight software. Some core cFS applications adopted for CASPR include the cFS Schedule Manager (CSM), camera control for both the iSIM90 and the neuromorphic sensor, and telemetry management. Further core applications are described in Table 1.

Table 1: Description of Core Software Applications

App	Function Description
CSM	Enables schedule upload and cFS app control
HS	Gathers health and status information for each computing device (e.g. temperatures, heartbeats)
FD	Downlinks files to the ground station
FTL	Transfers files between nodes
GND	Controls the serial link with the pallet command input buffer
SHL	Sends a shell command to a node
SYS	Sends OS management commands to node
TO	Collects telemetry output for downlinking

The CSP boots directly from onboard, radiation-tolerant NAND flash memory. Each of the peripherals boot via the Trivial File Transfer Protocol (TFTP) boot with the CSP acting as the TFTP server. Using TFTP boot, the kernel image on the client nodes can be changed by uploading a new image to the head CSP node and rebooting the target node. To ensure reliability, redundant, golden boot images are stored in a read-only partition of the flash memory, enabling a failsafe to redundant images if any damage occurs.

The μ CSP flight computer runs baremetal C code to interface with devices for thermal monitoring, heater and gimbal motor control, and gimbal position tracking. The μ CSP communicates with the CSP via UART, transmitting health and status information and receiving commands to adjust operational parameters.

CSP and SSP SoC Architecture

The architecture of the Zynq-7000 SoC of CSP and SSP, illustrated in Figure 13, includes an interconnect between the fixed-logic processing system (PS) and the reconfigurable programmable logic (PL) side of the Zynq-7000 SoC. Using these interconnects, the PL has access to the PS DDR memory. Similarly, the PS is able to access the PL, enabling full or partial reconfiguration of the FPGA. A custom direct memory access (DMA) controller has been designed to facilitate higher memory bandwidth for FPGA-accelerated applications.

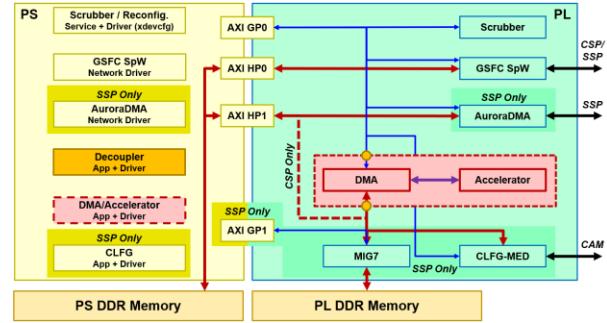


Figure 13: FPGA/SoC Architecture

For MGT communication between the SSPs, the Aurora 64b/66b protocol is used. A custom hardware/software (HW/SW) stack was created to support conventional networking applications over Aurora.

Power System and Modes

The power system uses a single chassis mounted VPT SVRFL2812S 28V to 12V 100W converter and EMI filter that provides power to the entire CASPR mission. The 12V from the chassis converter is then fed into a power card that uses VPT SVPL1209SG point-of-load converters to generate the required 5V and 3.3V bus voltages for the rest of CASPR as shown in Figure 14. Current monitoring of the 12V, 5V, and 3.3V busses is performed on the power card using Allegro ACS71240 ICs to ensure that CASPR does not exceed its 50W power budget from STP and this data is collected using a TI ADC128S102QML-SP [16].

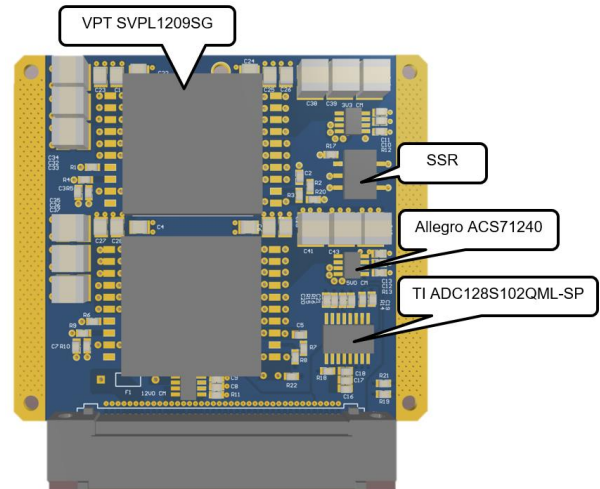


Figure 14: CASPR Power Card

In order to achieve all mission objectives and remain within the 50-Watt power budget allotted by STP-H7, different power modes ensure that the power consumption of all devices does not exceed the allotted budget. A particularly troublesome constraint is the inability to power both SSPs and the main imagers at

the same time. To address this constraint, hardware is divided into multiple power islands controlled by a combination of solid-state relays (SSRs) and software configurations. Several operational states are available to power on a safe set of devices for CASPR to perform a specific mission operation.

Each power mode serves a purpose towards the overall mission objective. There will be six main modes of operation, including a low-power safe mode with minimal functionality. The five other modes consist of a preparation stage, an imaging configuration, a backup imaging configuration, a dedicated compute mode, and a mode for GPU acceleration. A further description of the modes can be viewed in Table 2.

Table 2: CASPR Power Modes

Mode	Power Usage [W]	Mode Description
Safe	5	Only the CSP head node and μ CSP are powered
Preparation	36	Prepare CASPR by opening optics shutter, releasing gimbal ejector, and powering iSIM90 heaters and gimbal motor
Imaging	36	All cameras powered, one SSP active, gimbal motor for camera movement while imaging, and PCM for data storage
Imaging Backup	33	All cameras powered, opposite SSP active to act as backup, gimbal motor for camera movement, PCM no longer accessible
SSP-SSP Compute	34	Both SSPs powered with MGTs active for application acceleration, PCM and neuromorphic sensor also on
SSP-GPU Compute	29	One SSP active and supporting machine-learning and computer-vision application acceleration on the GPU

Experiment Applications

The immense computational capacity and unique sensing capabilities of the CASPR platform enable the deployment of many applications to facilitate on-orbit experiments. A suite of ML/CV apps will be included to adjust, transform, and filter captured images onboard. A tool to monitor and track SEEs in on-chip memory of the CSP and SSP will also enable the system to adaptively reconfigure resources in response to dynamic environmental conditions [17]. An intelligent scheduling system for mission management will govern all system tasks and functions [18]. This system is encapsulated in the CSM application.

The high-resolution and low-GSD nature of the main imagers presents tremendous opportunities for spaceborne computer-vision research. Deep-learning classifiers will be deployed to make intelligent determinations of image contents [19]. Semantic segmentation will be accelerated on SSP FPGAs to rapidly generate simplified representations of image contents, allowing for efficient downlink and space situational awareness [20]. Full images will be compressed through conventional means or more novel techniques enabled by convolutional neural networks [21]. Efforts to improve reliability of many deployed applications via algorithm-based fault tolerance applied to computational kernels will be undertaken [22].

Additional software suites will accompany and bolster the functionality of individual subsystems. Operation of the neuromorphic vision sensor will be governed by its own software for object tracking [23]. A suite of applications will be deployed to the AMD GPU for ML/CV application acceleration and reliability studies. Another suite of apps will enable testing of the function and resilience of the Intel Optane PCM.

This set is only an initial selection of the potential applications that could be deployed to CASPR. The system is designed around the capability to upload and integrate new applications in-flight. This presents the opportunity for a continuously evolving autonomous processing pipeline fitting the needs of research and experimentation for the full mission duration.

V. MISSION OBJECTIVES

The primary purpose of this experiment is to test autonomy with novel sensors and computing technologies for future spacecraft. However, there are many mission requirements necessary to satisfy the conditions for success.

One directive is to advance the TRL of the SSP flight computer, AMD embedded GPU and carrier card, Intel Optane PCM, Satlantis iSIM90 optics and Sysley neuromorphic sensor in low-Earth orbit (LEO). The iSIM90 optics will be tested for its GSD measurement from LEO for various Earth observation experiments. The object-tracking capabilities of the neuromorphic sensor will be tested for accuracy.

Each experiment on CASPR has its own classification of minimum and maximum success criteria. Each computing technology's minimum criteria involves ensuring functionality of the device. This includes observing health and status information from the SSPs and GPU as well as performing basic read and write tests on the PCM. Both sensors have similar minimum successes to capture a significant amount of data for

downlinking. For each experiment to achieve maximum success, it must consistently perform its primary operational objective for the duration of the mission. A detailed list of the success criteria can be seen in Table 3.

Table 3: Experiment Success Criteria

Experiment	Minimum Success	Maximum Success
SSP	View health and status to ensure operations in space	Accelerate computing experiments using MGT communications
GPU	Receive basic health data to observe behavior	Accelerate ML/CV applications
iSIM90	Capture at least one multispectral image for downlinking	Perform low-GSD experiments autonomously
Neuromorphic Sensor	Capture and downlink event data	Tracking of space objects for SSA
PCM	Store and read back data from memory	Long-term storage of data collected from sensors

VI. CONCLUSIONS

As missions continue to include novel, high-resolution sensors, the need for onboard processing and autonomy to combat the increase in data sizes will only continue to grow. In this paper, we introduce the CASPR experiment for the STP-H7 mission, including the flight software, hardware, architectures, and mission objectives. CASPR represents a versatile, capable platform for autonomous sensor processing research and inspires the next generation of autonomous, onboard space computing solutions.

This mission will advance the TRL of all novel sensors and flight computers, including the new Satlantis iSIM90 optics, the Sysley neuromorphic sensor, and the SSP. Following comprehensive mission success, CASPR will remain in continuous development as a research, development, and test platform for new software, FPGA, and application designs. The system will remain in use for Earth observation, computer-vision, space situational awareness, and machine-learning experiments. CASPR will further serve as a demonstration and validation platform for new sensors and technologies of future spacecraft.

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