A Fault Tolerant Integrated Electronics Module for Small Satellites

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Abstract. The Johns Hopkins University Applied Physics Laboratory (JHU/APL) Space Department has developed the JHU/APL Integrated Electronics Module (APL IEM) architecture for future satellites to minimize development costs while maximizing mission flexibility. The architecture supports both low earth orbit and deep space missions. Redundant and single string configurations are possible. Core spacecraft functions including communications, guidance, navigation, attitude, power control, health and safety, command, and data handling are implemented in the APL IEM. Extensive use is made of industry standards. Adhering to these standards at subsystem boundaries allows us to incrementally improve these designs without impacting the remainder of the system. Internal subsystems communicate over redundant, IEEE 1394, high speed, low power, serial buses. External interfaces include dedicated device specific links as well as those already in common satellite use. However, an unusual distributed approach to engineering housekeeping data acquisition based on the I^2C industrial bus improves flexibility and increases design reusability.

Introduction

The Johns Hopkins University Applied Physics Laboratory Space Department has developed the JHU/APL Integrated Electronics Module (APL IEM) architecture for future satellites to minimize development costs while maximizing mission flexibility. Our architecture collapses most core spacecraft control electronics into a single fault tolerant chassis that can be configured to satisfy a wide range of requirements. Each subsystem within the APL IEM has a straightforward, single string design and is implemented on a single circuit board. Fault tolerance is achieved by duplicating critical cards and switching power to a backup in case of failure. Subsystems communicate over a redundant, IEEE 1394[1] high speed, low power, serial bus within the APL IEM and with serial digital links to instruments and sensors elsewhere on the satellite. We also use a low speed auxiliary digital serial bus (I^2C) for collecting status and engineering housekeeping data.

Subsystems can be readily reused on different missions resulting in significant nonrecurring development cost savings. When appropriate, an individual board design may also be upgraded without impact on other subsystems within the APL IEM. The functionality of the core board set is optimized across traditional spacecraft subsystems boundaries to improve power efficiency and reduce mass. Circuitry unique to specific missions can be included and performance can be readily enhanced with additional general purpose processors and/or task specific circuits. Finally, the reusability, flexibility, and enhanceability of the APL IEM architecture mean that investments in advanced miniaturized packaging technology can be amortized over multiple missions[2].

Traditional design approaches to fault tolerant spacecraft electronics design add substantial cost and mass penalties to satellite development. Thus a commonly suggested small satellite design methodology accepts that a single electronics breakdown can result in mission failure. Yet despite the communities' best efforts, even small satellites are still costly, difficult, and time consuming to develop. The consequences of failure are still severe, especially to spacecraft scientists and sponsors, and thus it is still desirable and important to avoid single point failures. Because the APL IEM already provides common chassis and redundant communications, the incremental cost of adding hardware to achieve fault tolerance is reduced to that needed to duplicate an already designed circuit card. The possibility of a single critical electronics fault causing mission failure is eliminated at lower cost than previous designs.

Background

Traditionally, a satellite's electronic circuits are organized in several subsystems, each housed in its own chassis. Subsystem boundaries are determined by the functions performed and hence the spacecraft block dia-

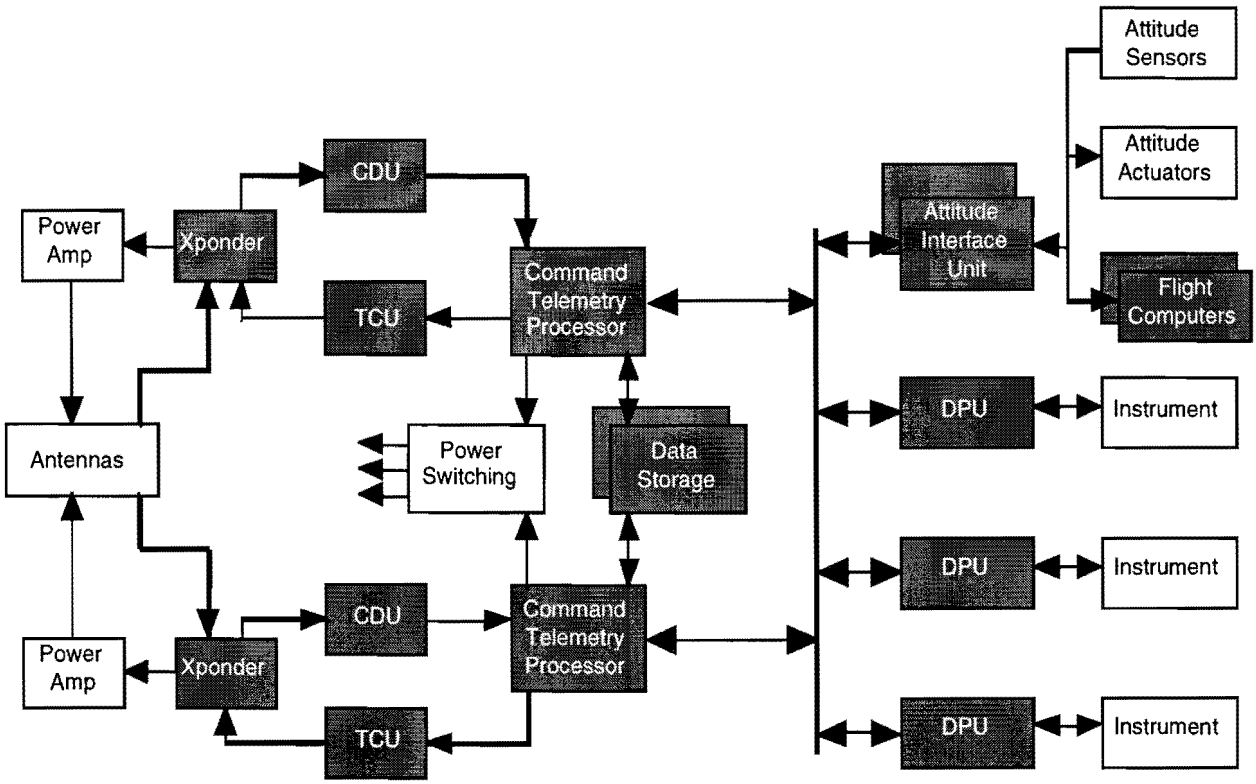

Figure 1. Simplified NEAR electronics block diagram.

gram is essentially based on its functional requirements. Figure 1 is a simplified block diagram of typical spacecraft designed around this principal, the Near Earth Asteroid Rendezvous (NEAR) satellite.[3] NEAR was launched on February 17, 1996 and will enter orbit around the asteroid Eros in early 1999.

The NEAR electronics system architecture is fault tolerant with block redundant mission critical subsystems. These include telecommunications (except for high and medium gain antennas), solid state recorders, command and telemetry processors, Mil-Std 1553 data buses, attitude interface units, guidance and control flight computers, and power subsystem electronics. In addition, NEAR uses 4 inertial measurement sensors, 5 sun sensors, and 11 small thrusters.

The APL IEM can be configured to include the capabilities of the highlighted subsystems shown in Figure 1. The 17 separate electronics boxes on NEAR could be replaced by a single chassis of our new architecture. We estimate that using our IEM would have resulted a mass reduction of over 50 Kg (6.5% of the satellite's wet mass) without applying further packaging miniaturization. This mass savings by itself is insufficient to allow a smaller launch vehicle to be used. However, the extra margin could be used for an extra science instrument or to save costs by easing design requirements elsewhere on the spacecraft.

Requirements

The overall goal of the APL IEM is to lower the cost of developing the electronics that control the core functions of a spacecraft. We sought to achieve this goal by developing a flexible architecture that maximizes design reuse and combines as much electronics as possible into as few as one chassis. By performing these tasks in a single unit, we wanted to reduce spacecraft mass and power by using optimizations that cross traditional subsystem boundaries. The resulting single box implements communications, guidance, navigation, attitude, power control, health and safety, command, and data handling functions for the spacecraft.

The APL IEM design is based on satisfying the major requirements listed below.

- *No single point failure leads to loss of mission;* Despite the current trend for more inexpensive spacecraft with frequent launch opportunities, many missions of scientific importance must last years rather than months. Reliability of aggressive,

commercial based, component technology is, of necessity, unproven in long term space applications especially when these parts are combined into the complex systems needed for the advanced scientific mission concepts now in development. An architecture immune to single point failure can mitigate this concern and thus lead to more capable designs implemented at lower cost.

- *Redundancy is achieved by adding additional unmodified resources*; Fault tolerance is achieved in the APL IEM by duplicating resources. Thus each subsystem has a straightforward and inexpensive single string design. It is the topology of how those devices are interconnected that determines the fault tolerance of the system. Thus our IEM can be built completely single string or with fully dual or even greater redundancy as needed. Subsystems design for all these cases is unchanged.

- *Standardize spacecraft data acquisition interfaces;* Satellite housekeeping and attitude/guidance sensors and actuators equipment needs are very mission dependent. We want to accommodate those differences with minimal design changes in order to achieve the reuse benefits of the architecture.

- *Processor independent and upwardly extensible interconnect bus design;* Microprocessors are evolving at a gratifyingly rapid rate. Our architecture divorces specific processor choice from the remainder of the system design. Furthermore, for loosely coupled tasks, as are typical for controlling core spacecraft functions, additional computers can be added to increase throughput if needed.

- *Connect 20–30 subsystems;* The number of subsystems required for control of a spacecraft is relatively modest. Highly parallel computers may be effective for signal or image processing tasks but are not well suited to spacecraft control tasks. However, such a parallel machine can be treated as a peripheral device that provides summary information to the APL IEM.

- *Data traffic up to 50 Megabits per second across the backplane;* Our analysis of spacecraft indicates that only a modest communications bandwidth between IEM resources is needed to implement core functions. A high performance, parallel, bus such as PCI, VME, or Futurebus+ uses considerable power for transceivers and signal termination and also can consume significant surface area on each circuit card. Because we have not over specified data rate, a serial bus can be used. Load and terminator power consumption are minimized and redundant interconnect structures are much more practical with a serial rather than parallel bus.

While the APL IEM satisfies many important small satellite needs, it is also important to note what it was not designed to do. The relatively modest bandwidth between boards is not appropriate for large volumes of data transfers. For example, uncompressed, high resolution, and continuous image movements from sensor to signal processor can exceed the capability of our internal bus. This example is probably better solved using a dedicated special purpose link between the communicating resources. Flexibility of our architecture supports a modest number of loosely coupled general processors. This topology is poorly suited to highly parallel signal processing tasks such as on-board analysis of synthetic aperture radar data. However, the APL IEM could easily collect summary analyzed data from such a special purpose processor, autonomously evaluate the significance of the results, and then direct further spacecraft activities based on that information.

The APL IEM is an architecture that can reduce the mass and power of a satellite while lowering development costs through design reuse. Our architecture can be implemented with traditional packaging technology but it may also be built using more advanced approaches. Modularity encourages board reuse so that investments in miniaturized manufacturing are more easily amortized over more than one mission even for one of a kind science spacecraft.

Architecture

The APL IEM consists of general purpose and mission specific resources implemented on circuit cards. A block diagram of our IEM configured for a typical deep space mission is illustrated in Figure 2. Board functions were carefully chosen to isolate mission unique interfaces to a small set of boards. The generality of the remaining board designs is such that we believe they will be useful for several missions. In the configuration shown in Figure 2, only the Spacecraft Interface, Instrument Interface, and Converter boards are mission specific. The remaining cards are applicable to many types of spacecraft. For example, a low earth orbiting satellite would use interface cards tailored for its instrument suite and might replace the IMU and Star Camera with IEM boards containing a GPS Receiver. The Spacecraft Control Processor, Communications Link, Main Processor, and Solid State Recorder cards would be unchanged.

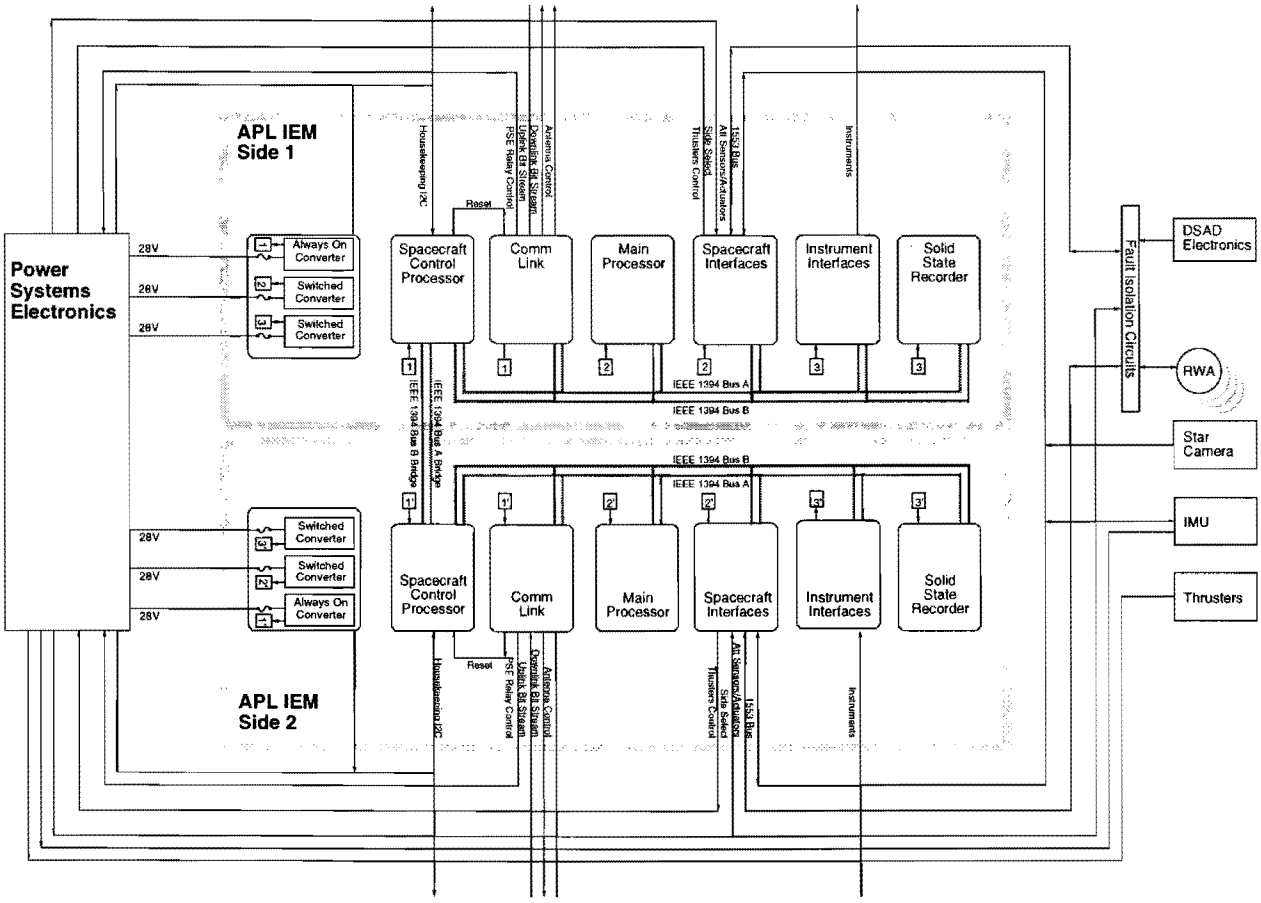

Figure 2. Deep Space APL IEM Configuration

Resources within the APL IEM are interconnected by redundant IEEE 1394 High Speed Serial Data Buses. Each board, when necessary, includes interface circuits to the rest of the spacecraft. We are now developing an application specific integrated circuit IEEE 1394 protocol chip that interfaces each card to the internal backplane serial bus.

External Interfaces

When possible we have defined interfaces between the APL IEM and the rest of the spacecraft based upon industry standards. These include various serial links based on RS-422, I^2C, and Mil-Std 1553. We have also defined a robust, low power, custom serial interface for critical functions such control of power switching.

Unlike a traditional Command and Data Handling (C&DH) subsystem, acquisition of engineering parameters such as structure and subsystem temperatures, voltages, and currents is not centralized in the APL IEM. Instead we use a distributed approach to acquisition of housekeeping data. Information is collected where it is measured and digitally transmitted over a slow serial bus to the IEM. This methodology is flexible and can easily accommodate changes to the number and type of monitored parameters even late in a spacecraft's design cycle. Widely differing requirements can also be accommodated without changing hardware in the APL IEM further encouraging design reuse and cost savings. Finally, harness complexity and mass are reduced since we use a simple low speed serial digital bus for the distributed acquisition components.

We selected the Inter-Integrated Circuit (I^2C) bus[4] for housekeeping data acquisition. The I^2C bus was originally developed by Philips Semiconductor to connect peripheral chips to microcontrollers and is widely used in industrial embedded control applications. I^2C is a very simple bus running at 100 Kbits/sec and uses standard TTL logic levels. A controller node can be implemented in fewer than 1000 gates and easily fits in readily available space qualified field programmable gate arrays.

Unfortunately, the I^2C specification does not include provisions for data transmission error detection or correction. Thus, no action should be taken based on a single sample collected over I^2C. Most algorithms analyzing housekeeping parameters already process multiple samples before raising alarm conditions so the lack of error detection in I^2C is not significant in that application. Extending I^2C to control actuators is more problematic and the APL IEM architecture does not yet use the bus for those purposes. However, we are evaluating several straightforward, albeit nonstandard, protocol extensions that can be layered on top of I^2C when reliable communications are needed.

Key to successfully implementing distributed data acquisition are components with the needed capability that are compatible with the digital housekeeping bus. We have developed a single chip multichannel data acquisition chip, called the Remote Input/Output (RIO) chip[5] that can digitize many types of engineering data and connects directly to the I^2C bus. This component can be housed in small package and attached directly to spacecraft structure or it can be used within a larger subsystem.

Power Systems Electronics (PSE) are controlled by the APL IEM. Currents and voltages are monitored using the I^2C bus previously described. Switches that connect unregulated spacecraft 28V to other loads are commanded by the APL IEM through a custom developed serial control interface. The number of the activated switch is transmitted twice through this link and both values must match before the command is executed. Proper activation of the selected switch is monitored by observing tell tale states over the I^2C bus. Since the power control and switching interfaces are based on standardized connections, APL IEM hardware should not need to be changed even if substantially different PSEs are developed to meet different mission requirements.

Thruster and latch value control relays are also located in the Power Systems Electronics unit to minimize electromagnetic compatibility problems within the IEM. These relays switch large currents and we were concerned that those changes could effect other circuitry. Since the thruster configurations vary significantly between missions and timing of these relays closures is critical the APL IEM will use a dedicated parallel connection for controlling the thruster relays.

Many sensors (especially star cameras and gyroscopes) and instrument packages have been developed that communicate data over a Mil-Std 1553 data bus. However, we expect that 1553 will not achieve universal use, especially on small satellites, because of its high power consumption and modest 1 Mbit/sec maximum data rate. Therefore, we consider 1553 to be a mission unique interface and have thus placed its control logic on a mission specific interface card.

Interfaces to attitude sensors and actuators are chosen to satisfy each mission's unique requirements. There is also little interface standardization between manufacturers of this type of equipment. There is similarly, little commonality in instrument characteristics so it is not yet possible to develop a standard reusable interface between the APL IEM and many sensors, actuators, and instruments that will be used on future small satellites. However, developing these types of mission unique interface cards is straightforward especially since the APL IEM internal bus interface is well defined (IEEE 1394).

Internal Interfaces

The APL IEM uses redundant IEEE 1394[1] high speed serial backplane profile buses for data communications between its boards. Fault tolerance is achieved by using either the primary or secondary serial bus for data transfers and supplying conditioned secondary power to the primary or backup version of each subsystem card. Thus all resources within the IEM are effectively cross strapped and will properly function even after a single failure. IEEE 1394 is rapidly emerging as a significant standard[6] and is gaining widespread support in the computing and digital video industries. There are also several DOD applications of 1394 now in development.

The IEEE 1394 backplane profile describes a serial bus linking nodes within a single backplane. Addressing conventions established by IEEE Std 1212[7] are followed. All nodes share a common 64 bit address space with 16 bits reserved to select the node and the remaining 48 bits (256 terabytes) available to the node. Specific locations are reserved for core resources, serial bus specific registers, and ROM ID area, as well as node specific resources. The bus protocol consists of three stacked layers that implement a complete request/response architecture providing read, write, and lock transactions. All data transfers are quadlet (32 bits) operations to quadlet aligned addresses. Maximum transaction time is less than 62 μs which is about 256 bytes at the currently specified 50 Mbit/sec highest backplane

data rate. Each node can contend for bus control through three different arbitration methods; fair, urgent, and isochronous. Fair arbitration is used for transactions that can equally share bus bandwidth; Urgent arbitration is used to obtain a majority of the bus bandwidth or minimize latency. Isochronous arbitration provides low overhead access to the bus for regularly transferred data.

Each half of the APL IEM contains a complete set of resources. Communications between each half occur through a bus bridge. Data traffic destined for resources in the other half of our IEM are automatically forwarded by the bridging circuits. Electrical loading of the 1394 bus is reduced because of the bridge. If needed to improve mass distribution on the satellite, the bridges enable the APL IEM to be housed in two rather than one chassis. The bridge also allows each Spacecraft Control Processor (SCP) to monitor traffic on both 1394 buses for improved satellite safing.

Resources

The core APL IEM resources are summarized in Table 1. Initially these modules will be implemented as conventional circuit cards but this same set of fundamental functions is equally valid if more aggressive packaging technology is used. If a traditional transponder is used for communications, the APL IEM will include a communications link card that formats and encodes downlink telemetry, detects critical uplink commands, and controls transponder functions. Alternatively we have developed a transceiver card set for our IEM that works directly with S or X band signals.[8]

Spacecraft Control Processor

The Spacecraft Control Processor (SCP) card includes a microprocessor with both volatile and non-volatile memory, IEEE 1394 interfaces, and I^2C controller circuits.

Spacecraft health and status monitoring is performed by the SCP's microprocessor. Because we use the distributed housekeeping data acquisition approach previously described, the I^2C interface on the SCP can acquire status information directly from the rest of the spacecraft. The SCP processes this data to ensure operating conditions are within normal limits and if exceptions are found, the SCP initiates recovery procedures autonomously. Fault repair consists of issuing switch commands to the PSE to turn off the failed device and then turning on its replacement.

Table 1. Core APL IEM Resources

Resource	Mission Type		Functions
	Low Earth	Deep Space	
Spacecraft Control Processor	√	√	safing, cmd proc, autonomy,
Main Processor	√	√	attitude, G&C, Adv autonomy, inst ctl,
Communications Link	•	√	crit cmd proc, pse switch ctl, tlm fmt, tlm encode, xponder config
Command Receiver	√	•	uplink RF, crit cmd proc, pse switch ctl
Downlink Exciter	√	•	tlm fmt, tlm encode, RF mod
GPS Receiver	√		positioning
Solid State Recorder	√	√	bulk data storage

√ Typical application
• Alternate application

Proper operation of the IEEE 1394 is mission critical because it is used for transferring uplink commands and fault recovery power switching commands between the Command Receiver (or Communications Link) and SCP. Hence the SCP continuously monitors performance of the internal IEEE 1394 buses. If abnormal traffic patterns are detected then the SCP is responsible for determining the cause of the problem and initiating corrective action. Similar monitoring of data transfers on the bus bridges between the two sides of the APL IEM is also performed by the SCP. A bridge will be disabled by the SCP if incorrect operation is detected. Because at least one SCP on the spacecraft must work properly, both must be continuously powered.

Normal command packets are sent from the Command Receiver (alternatively, the Communications Link card) to the SCP for processing and validation over the IEEE 1394 bus. Error checking is performed and if successfully verified, the command is queued and executed at the proper time. A small number of emergency commands are defined that are decoded and executed directly by hardware in the Command Receiver (or Communications Link if used). Most of these commands control switches in the PSE but one can directly reset the SCP. Emergency commands are expected to only be issued if the spacecraft enters a backup safe operating mode.

Main Processor

Like the SCP, the Main Processor also includes volatile and non-volatile memory and a redundant IEEE 1394 interface. However, no other I/O circuits are present. Commercial microprocessor technology is far ahead of what has been qualified for space applications and thus

we expect (and hope) that considerable flight processor improvements will occur. By isolating computing functions to a pure processor board we have minimized the changes needed to use alternative microprocessors.

The Main Processor is responsible for all core spacecraft calculations including: attitude determination and control; guidance; instrument data collection and processing; forming telemetry data frames and forwarding them to the transmitter; high level spacecraft autonomous operations; and power systems control.

Solid State Recorder

All potential missions for the APL IEM that we have studied have need for a bulk data storage device. Board area estimates show that 2 to 4 Gbits of memory and control logic will easily fit on a single card. The estimates included Reed-Solomon error detection and correction circuits as well as a storage array based on 64 Mbit Dynamic Random Access Memory (DRAM) chips. Only packaged parts surface mounted on both sides of a printed circuit card were used in our capacity estimates.

Next generation components such as 256 Mbit DRAM will quadruple capacity. More aggressive packaging such as chip on board and stacked memory parts can also increase the amount of data stored in the recorder.

Communications

There are two alternatives for implementing communication functions with the APL IEM. An interface card can control an external transponder. Alternatively a Command Receiver and Downlink Exciter card set we are developing can be used.

The Command Receiver extracts the uplink command bit stream from the RF signal collected by the spacecraft antenna. Circuitry to detect emergency commands embedded in the uplink stream is also included on the receiver card. These commands can reset the SCP and control switches in the PSE. Normal commands are accumulated and forwarded to the SCP for processing. If a spacecraft uses a transponder rather than this receiver card, then the Communications Link card contains the emergency command decoding and forwarding electronics.

The Downlink Exciter modulates data onto the downlink radio frequency carrier. An external amplifier boosts the signal to the required power levels. The board also includes digital circuits to buffer, encode, and format the data. The Communication Link card includes similar digital circuits.

Mission Unique Resources

Spacecraft actuators and sensors including reaction wheels, door mechanisms, and attitude sensors are monitored and controlled by the Main Processor through interface cards in the APL IEM. The precise design of the interface card is likely to vary between spacecraft since each mission will have different actuator mechanisms. However, the standardized backplane interface will provide a flexible and easily used interface so design effort tailoring I/O cards to unique mission needs will be minimal.

In a fault tolerant configuration some devices will need to be connected to interface cards in both sides of the APL IEM. For example, spacecraft commonly include more than the minimally required set of reaction wheels. The wheels are oriented so that attitude can still be controlled even if one has failed. So all reaction wheels must be sensed and controlled from the interface card on either side of the APL IEM. Simple passive isolation circuits for sense voltages and side select switches for speed set voltages are contained on an external fault isolation terminal board (see Figure 2).

Our initial IEM design includes redundant DC/DC Converters to supply regulated secondary power to related groups of boards. These card groups receive spacecraft power from the PSE. Because at least one SCP and Command Receiver (or Communication Link for transponder based designs) must operate properly at all times, these two boards are grouped together and use unswitched primary power. The remaining groups are powered through fused switches in the PSE.

The converters are housed on a circuit card plugged directly into the backplane. Special grounding, shielding, and routing provisions were made to minimize EMI and EMC effects on the backplane motherboard. Wide power distribution traces sized to handle the expected currents with minimal resistance were sandwiched between ground planes. Ground planes were heavily interconnected through a large number (26%) of ground pins. We have conducted interference and compatibility testing on a card based S Band Receiver powered through our backplane from an adjacent Converter card and have noted no degradation in performance.

Mechanical

The IEM consists of one or two chassis where each box is a card cage supporting removable circuit boards interconnected with a passive backplane motherboard. The backplane distributes switched and unswitched secondary

voltages from the DC/DC converter board to specific slots. Sensitive RF signals directly connect to the appropriate card through a connector on the opposite side of the motherboard connection. All other external signals and power leads enter the card through dedicated pins in the main backplane connector. Flexible printed circuit cable carries the external signals from the backplane pin to the external I/O connector.

Those signals that are not used on other IEM boards are conveyed to the external connectors on the sides of the chassis through flex printed circuit cable.

IEEE 1101.7[9] defines the card size for our IEM boards. However, to ease manufacturability, APL uses an Airborne Inc. 075 Series 220 pin position connector or equivalent with pin to pin spacings of 0.75″ rather than the higher density connector specified by the standard.

We have designed and built a prototype chassis for the APL IEM using carbon composite materials. The cage houses 10 circuit boards, a motherboard, and external connectors. The design uses high thermal conductivity fibers in specific areas to spread heat away from the card locks. Lower conductivity fibers are used elsewhere to reduce the costs. Wall thickness is set at the minimum levels needed to meet strength requirements. A photograph of the chassis with a breadboard DC/DC Converter card partially inserted is shown in Figure 3.

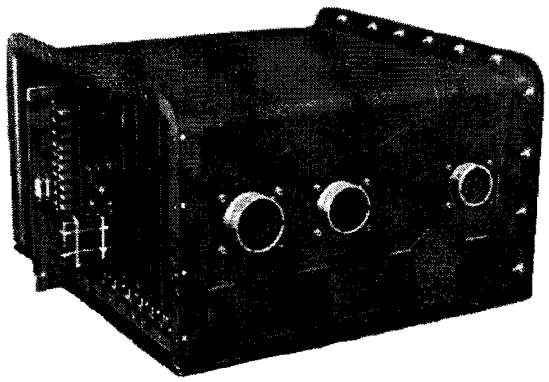

Figure 3. APL IEM Prototype Composite Chassis

The layout of the card cage maximizes heat transfer area to the mounting deck. The card locks are mounted to the top and bottom panels. The cards are installed into a motherboard that mounts vertically at the back of the cage. Circuit board heat dissipation is transferred through the card locks to the bottom panel. The top panel acts to spread localized heat from specific cards over the entire panel. The cage design supports a card dissipation of 10 watts per board on average, and 20 watts peak although none of the card designs we have studied approach these limits. Thermal performance has been modeled and verified using aluminum boards and heaters to simulate the distribution of power dissipation within the chassis. The composite chassis loaded with dummy mass board loads also passed vibration testing at levels typical of launch environments.

Tolerance control is an important feature in the design of the card cage. Typically, it is difficult to control the relative dimensions of the board width, board spacing, motherboard mount points, and connector location tightly enough to make the whole box come together without putting very tight tolerance on all the various pieces. The APL IEM design bonds separate card locks to the box walls. All card locks are mounted relative to the motherboard connector location. The tolerance problem is eliminated while allowing normal tolerance on all the parts.

Bonding of metals and composites is of concern due to the mismatch between their coefficients of thermal expansion. We tested aluminum/composite adhesive joints over a range of temperatures and cycles to quantify the strength of the bonds. The results showed that in all cases the bonded joint was stronger than the laminate beneath it. This surprising observation has generated many new questions about the nature of these types of bonds that we hope to investigate further. However, it is clear that the two materials can be successfully bonded over a wide range of conditions.

Discussion

The APL IEM encourages design reuse. The functionality of our core board set was carefully chosen to maximize reusability. Mission dependent circuits are isolated to a small number custom designed cards. The remaining board designs are of general use in many satellite applications and can be reused without modification. Costs are lowered, schedules are shortened, and program risk is reduced.

Some examples illustrate this principle. The Main Processor board contains no interfaces, other than the internal IEM bus, to the remainder of the spacecraft. Thus it can be used without modification on missions that use Mil-Std 1553, Mil-Std 1773, point to point high speed serial links, hard wired dedicated ports, or any other combination of data handling strategies. The Spacecraft Control Processor uses the I^2C bus to acquire

housekeeping data from all over the spacecraft. The number and type of monitored parameters is not limited by hardware on the SCP. Instead the distributed data acquisition circuits work directly with the specific type of data that is being sampled. The Solid State Recorder also contains no special interfaces. All data transfers to and from the SSR occur over the internal bus. Different instruments are accommodated on the instrument's interface card and the SSR design is not effected.

While the APL IEM encourages reuse, the architecture also gracefully accepts design improvements. As memory density inevitably increases, a higher capacity SSR card could be developed without impacting other resources. Processor designs based on different microprocessors also do not effect other hardware. The net result is that the APL IEM is well suited to incremental improvement and the architecture should continue to be viable for future small satellite programs.

Many have suggested that one way to reduce costs on small satellite programs is to sacrifice fault tolerance. The rationale is commonly promulgated that failure can be tolerated since reduced costs mean that more missions will be launched. Thus loss of a single spacecraft can be tolerated since the funding agency can afford (or at least the principal investigator fervently hopes they can) to build a replacement. This is an unsettling strategy, especially for unique, long duration missions and to those scientists most closely involved with the program.

The APL IEM architecture achieves fault tolerance with only modest cost increase. Only the hardware of already designed boards need be duplicated and qualified. Fault tolerance is achieved by duplicating resources within the APL IEM so there is no single point of failure. The internal IEEE 1394 serial data bus is redundant and both buses are bridged between the two halves of the APL IEM. Data connections between all cards are thus effectively fully cross-strapped. If a failure jams one of the data buses, the redundant bus can still be used. Finally if a fault effects both buses within one side, the unaffected half can disconnect the bus bridge and continue to operate.

Depending on specific equipment requirements, a redundant Mil-Std-1553 serial data bus can connect the APL IEM with off the shelf Inertial Measurement Units and Star Camera attitude sensors. Each side of the IEM also contains thruster control logic and can energize redundant thruster relays. Instrument data collection and control is similarly implemented with interface cards on both sides of the IEM. Each instrument contains interface circuits that provide fault isolation between it and the two sides of the IEM. Finally, a small unpowered terminal board with passive circuits provides isolation between redundant IEM circuits and duplicated resources with non-redundant interfaces; for example, digital sun attitude detector electronics and reaction wheel assemblies.

Integrating satellite electronics into a common chassis enables system level optimizations. The APL IEM uses its computing resources to implement functions previously distributed across several resources. Power and mass are saved by eliminating duplicated hardware such as DC/DC converters and processors. Data communications between functions is also improved. Much information normally sent between traditional subsystems is now directly available within a processor. Other data is sent between resources on the power efficient internal APL IEM data bus. Instrument control and onboard data analysis can be implemented within the APL IEM instead of in separate instrument data processors. Additional Main Processor boards can be readily used, within the constraints of interprocessor bus bandwidth, and can increase computing power for handling multiple loosely coupled tasks. Finally, evolving housekeeping data requirements can be met, even well into spacecraft development because of our distributed approach to housekeeping data acquisition.

The APL IEM architecture was developed to provide large spacecraft capability on small satellite budgets. It can be adapted to both low earth orbit and deep space missions. Fault tolerance can be tailored to satisfy the requirements, and the cost of a fully redundant configuration is only marginally more than a single string design. Mission dependent circuits are isolated to a small number of boards. The remaining resources satisfy requirements of many different missions and hence maximize reuse to lower development cost. The architectural innovations of the APL IEM can reduce small satellite cost and mass while speeding up development schedules. When also combined with advanced packaging technology even more improvement is possible.

Acknowledgments

The APL IEM was designed by a large number of staff members from the JHU/APL Space and Technical Services Departments using internal funding. A committee chartered to insert advanced technology into our space programs, developed the original IEM concept. It has since been refined and enhanced through the efforts of

many other staff members, and the work reported here is due to those contributions and the supportive environment provided by our management team. I would like to thank Rich Conde, Bob Jenkins, Susan Lee, Jim Perschy, Ed Reynolds, Kim Strohbehn, and Tom Zaremba for their contributions to working out details of the APL IEM architecture and Doug Mehoke for his mechanical design concepts.

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References

[1] IEEE Std 1394-1995, "IEEE Standard for a High Performance Serial Bus".

[2] Conde, R.F., B.Q. Le, J.F. Bogdanski, A.L. Lew, J.A. Perschy, and M.A.G. Darrin, "Command and Data Handling in Your Palm," Proceedings of the 11th AIAA/USU Conference on Small Satellites, Logan, UT., September 1997.

[3] Santo, A.G., S.M. Krimigis, R.E. Jenkins, E.L. Reynolds, and T.B. Coughlin, "Lessons for the Future: The NEAR Mission in NASA's Discovery Program," Proceedings of the 47th International Astronautical Congress, Beijing, China, October 1996.

[4] "The I²C-bus and how to use it," *I²C Peripherals*, Philips Semiconductor, 1996.

[5] Paschalidis, N, "A Remote I/O (RIO) Smart Sensor Chip Supporting Serial Communications Bus for Small Satellites," Proceedings of the 11th AIAA/USU Conference on Small Satellites, Logan, UT., September 1997.

[6] Wickelgren, I.J., "The Facts about FireWire," IEEE Spectrum, Vol. 34, No. 4, April 1997.

[7] ISO/IEC 13213: 1994 [ANSI/IEEE Std 1212, 1994], "Control and Status Registers (CSR) Architecture for Microcomputer Buses".

[8] Bokulic, R.S., C.C. DeBoy, D. Minarik, J. Daniels, S. Cheng, and J.H. Sinsky, "A Highly Integrated S-Band Transceiver System with Two-Way Doppler Tracking Capability," Proceedings of the 11th AIAA/USU Conference on Small Satellites, Logan, UT., September 1997.

[9] IEEE Std 1101.7-1995, "Mechanical Standard for Space Applications Module, Extended Height Format E Form Factor".