FAST AURORAL SNAPSHOT MISSION UNIQUE ELECTRONICS COMPLETE SPACECRAFT ELECTRONICS CONTAINED IN A SINGLE ENCLOSURE

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Abstract

The Fast Auroral Snapshot (FAST) Mission Unique Electronics (MUE), housed in a single container, controls all major spacecraft functions. The functions include, Command and Data Handling (C&DH), Attitude Control and Stabilization (ACS), battery charge control and power distribution which comprise the Power System Electronics (PSE), thermal sensing and control, pyrotechnic device firing, spacecraft health and safety functions, Instrument Data Processing Unit (IDPU) interface and Small Launch Vehicle (SLV) interface. Each of the MUE functions have been optimized to conserve mass and power, utilize packaging, mechanical hardware and electronics components that are suitable for the radiation environment in the Auroral regions. The MUE mounts on a 10 by 12 inch footprint and is 10 inches in height. It weighs 30 pounds and typically consumes less than 14 watts.

Nomenclature

ACS Attitude Control and Stabilization
ALE Address Latch Enable
BCH Bose-Chaudhuri-Hocquenghem
CCSDS Consultative Committee for Space Data Systems
C&DH Command and Data Handling
CDU Command Detector Unit
CLCU Command Link Transfer Unit
CLCW Command Language Control Word
CRC Cyclic Redundancy Counter
FAST Fast Auroral Snapshot
FET Field Effects Transistor
FIFO First In First Out
HCI Horizon Crossing Indicator
IDPU Instrument Data Processing Unit
MET Mission Elapsed Timer
MUE Mission Unique Electronics
PROM Programmable Read Only Memory
PSE Power System Electronics
PWM Pulse Width Modulation
RAM Random Access Memory
SSS Spinning Sun Sensor
SLV Small Launch Vehicle
USART Universal Synchronous/Asynchronous Receiver/Transmitter

MUE General Description

The MUE provides interfaces between the major FAST subsystems as shown in Figure 1. The primary interfaces are C&DH, ACS, PSE, pyro devices, thermal, SLV and IDPU. The mechanical enclosure houses 12 removable circuit boards and a motherboard. Electrical interface is made through a series of D connectors and an SMA coaxial connection to the transponder. The enclosure is made of aluminum and uses thermal card locks for conduction of heat from the printed circuit cards to the sidewalls and mounting interface. The MUE is mounted on an instrument deck and has two brackets that partially support the top plate of the satellite as shown in Figure 2.

Figure 1 - FAST MUE System Block Diagram

Figure 2 - MUE Enclosure
The C&DH electronics are partitioned on the Spacecraft Processor Board, 2 Memory Boards, Housekeeping Board and the Uplink/Downlink Board. The Spacecraft Processor and Memory Cards provide dual 8085 processors to individually provide telemetry and spacecraft operating system support. Commands are received from the ground via the transponder and the MUE Uplink interface. The Spacecraft Processor in turn sends the appropriate commands to the IDPU interface to control the science instruments and deployment mechanisms. Nominally science data telemetry is established through a high rate interface from the IDPU through the MUE Downlink interface and then to the transponder. Alternately housekeeping and scientific data can be sent through the MUE Spacecraft Processor, backplane and Downlink card interface to the transponder. Housekeeping circuitry monitors temperatures, voltages and currents throughout the spacecraft.

The ACS electronics functions are distributed on three cards, the ACS Sensor & Clock Card, the Coil Driver and the Housekeeping Card. Sensor electronics include magnetometer, Spinning Sun Sensor (SSS) and Horizon Crossing Indicator (HCI) interfaces. Actuator electronics include a dual programmable constant current power supply to drive the spacecraft spin and precession magnetic torque coils.

The PSE is a direct energy transfer system. The solar arrays and battery provide the spacecraft power. Battery charge is regulated through circuitry contained in the MUE. Any excess charge is dumped into shunts to prevent battery overcharging. The power bus provides power to all spacecraft electronics including the pyros, coil driver, HCI, SSS, transponder and spacecraft instruments. Power to all devices except the transponder is switched by the MUE. The transponder cycles power to the transmitter section only when broadcasting. The internal electronics of the MUE are powered through a DC to DC Converter. The Pyros are commanded via the MUE which cut or release spring loaded latching mechanisms to open instrument covers and deploy wire and axial booms.

Figure 3 shows the circuit card location within the MUE. Each card will be discussed in detail in the sections following.

![FIGURE 3 - MUE Printed Circuit Card Locations]
Spacecraft Processor Card
The FAST Microprocessor board is the main computer interface for the spacecraft. It performs both the Attitude Control and Stabilization (ACS) and the Command and Data Handling (C&DH) functions of the spacecraft. The two processors are logically split into the ACS / PSE functions and C&DH telemetry functions. The microprocessors are redundant in that one processor can take over the combined but reduced role of both ACS and C&DH functions. The board is based on dual radiation hardened 8085 microprocessors sharing a backplane. These two microprocessors are two completely separate systems, each has its own RAM, ROM, interrupt scheme, and I/O scheme. However, when they access the external bus (i.e. to talk with another card) they are governed by a hardware arbitration circuit. This arbitration allows the first processor on the bus to complete its function and then will relinquish the bus to the 2nd processor. This arbitration is not active unless both microprocessors want the external bus at the same time. The microprocessor card contains two 8085 radiation hardened microprocessors. Each microprocessor has the following subsystems: interrupt latches, Input/Output scheme, 4k PROM Space, 48k RAM space, Watchdog Chain, and a Power Up reset circuit. The board also contains the hardware Backplane arbitration scheme, and 4 USARTS. A block diagram is shown in Figure 4.

Each Microprocessor is capable of addressing up to 64K of memory space. Table 1 is a list of the memory map of both microprocessors:

<table>
<thead>
<tr>
<th>MEMORY MAP</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>C000 - FFFF</td>
<td>16K RAM SPACE</td>
</tr>
<tr>
<td>4000 - BFFF</td>
<td>32K RAM SPACE</td>
</tr>
<tr>
<td>2000 - 3FFF</td>
<td>NOT USED</td>
</tr>
<tr>
<td>1800 - 1FFF</td>
<td>I/O WINDOW</td>
</tr>
<tr>
<td>1700 - 17FF</td>
<td>INTERRUPT READ</td>
</tr>
<tr>
<td>1600 - 16FF</td>
<td>INTERRUPT CLEAR</td>
</tr>
<tr>
<td>1500 - 15FF</td>
<td>LATCH A16-A23</td>
</tr>
<tr>
<td>1400 - 14FF</td>
<td>LATCH A8-A15</td>
</tr>
<tr>
<td>1100 - 13FF</td>
<td>NOT USED</td>
</tr>
<tr>
<td>1000 - 10FF</td>
<td>RESET WATCHDOG</td>
</tr>
<tr>
<td>0800 - 09FF</td>
<td>2K PROM SPACE</td>
</tr>
<tr>
<td>0000 - 07FF</td>
<td>2K PROM SPACE</td>
</tr>
</tbody>
</table>

Table 1. Microprocessor Memory Map

Synchronous Counter Chain and Clocks
The Microprocessors run at 4 MHz (the radiation hardened 8085 is specified at a maximum of 4 MHz clock); this clock is provided by simply dividing an 8 MHz crystal by 2. The board contains two 8 MHz crystals, however, only one crystal is used to drive both microprocessors. The other crystal is there for

Figure 4. - FAST Microprocessor Block Diagram
redundancy. The 2nd crystal is switched in and out by a spacecraft watchdog which sets a flip flop. The clocks for each microprocessor are ideally 180° out of phase; this was done in order to prevent both microprocessors from accessing the backplane at exactly the same time. The arbitration circuit is built around an 54AC74 which can go into an unsteady state when the preset and clear pins change at exactly the same time. By keeping the two microprocessors 180° out of phase, they will always be 250 ns apart from any accesses to the backplane.

The 8 MHz oscillator is divided by a 7-stage synchronous binary counter chain using a look ahead carry circuit. A slow gate (54HSC244) was inserted between the ripple carry out and the "enables" to the next stage. This "slow" gate ensures that the hold time for CEP (count enable) is present particularly when bits are switching from all 1's to all 0's. This counter chain provides the clocks necessary for the operating system "tick", the baud rate, the microprocessor clock, and also 6 hardware setable watchdog time-outs.

Interrupts

The 8085 has five interrupts available: INTR, RST 5.5, RST 6.5, RST 7.5, and the TRAP interrupt. INTR and TRAP are not used in this design. RST 5.5 and RST 6.5 are logic high-level interrupts while RST 7.5 is a rising edge triggered interrupt.

RST 5.5 is used as an indicator to the processor that the magnetometer phase has revolved one period. RST 7.5 is used as the operating system tick; it is clocked at 65 Hz which is obtained from the watchdog timing chain, and is the highest priority interrupt.

RST 6.5 has 8 interrupts multiplexed into 1 signal. Each output of the latch is connected to a D-type flip flop, and finally, the signals are "ORed" down to one signal (RST 6.5). The outputs of the flip flops are buffered and clocked so they can be read by the microprocessor. The circuit also provides means to mask out each of the interrupts, this prevents any one particular interrupt from running away and interrupting a processor to death. Table 2 lists the interrupt and its corresponding data bit.

<table>
<thead>
<tr>
<th>DATA BIT</th>
<th>INTERRUPT</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>PIP INTR</td>
</tr>
<tr>
<td>D1</td>
<td>S/E INTR</td>
</tr>
<tr>
<td>D2</td>
<td>E/S INTR</td>
</tr>
<tr>
<td>D3</td>
<td>1 Hz INTR</td>
</tr>
<tr>
<td>D4</td>
<td>PORT A2 INTR</td>
</tr>
<tr>
<td>D5</td>
<td>GSE 2 INTR</td>
</tr>
<tr>
<td>D6</td>
<td>PORT A1 INTR</td>
</tr>
<tr>
<td>D7</td>
<td>GSE 1 INTR</td>
</tr>
</tbody>
</table>

Table 2. Data Bit Corresponding to Interrupt

It should be noted that of the 8 muxed interrupts 4 were designed as level triggered interrupts and 4 were designed as edge triggered interrupts. Interface constraints required some level interrupts be latched in sync with the processor clock to avoid missing them during an interrupt service routine. The level interrupts are clocked in at 8 MHz and will remain until the device causing the interrupt is cleared hence, they will not be missed by the processor.

Power Up Reset

Each microprocessor has its own power up reset circuit. The circuit is a voltage sensing circuit, hence it is not vulnerable to the speed at which the power supply ramps up. The reset pulse lasts approximately 40 milliseconds after the power supply has ramped up to approximately 4V. A spacecraft watchdog and cycling power to the system are the only means to receive a complete backplane and microprocessor reset. The spacecraft watchdog can be achieved in two ways: 1) If 24 hours has elapsed and no communication has been received from the ground, then a complete reset is done, and 2) a command called "SWAP", this command will swap the two processors functions (C&DH becomes ACS, ACS becomes C&DH). This function should only be used if the spacecraft is in trouble and a reset is needed.

Input/Output

The system uses memory mapped I/O thru a 256 byte bus window. This I/O design requires several steps before data can be transferred. They are as follows:

- Latch A23-A16
- Latch A15-A8
- Enable A7-A0, Enable A8-A23, RD or WR strobe (by writing to the bus window)
Once the software sets up the latches the processor can access the bus as if it were local RAM. Since the 8085 has an 8 bit data bus and a 16 bit address bus, additional address lines had to be designed into the card. Therefore, A8-A23 to the backplane are built through latches and enabled to the backplane when the data and lower address lines are written out. This enabled the designers to add two bulk memory cards with 32K of PROM space and 512K of RAM space.

There are several control signals which are active when the data is strobed out onto the backplane. These signals are shown in Table 3.

<table>
<thead>
<tr>
<th>MICRO 1</th>
<th>MICRO 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTR1</td>
<td>CONTRA</td>
</tr>
<tr>
<td>CS3</td>
<td>SCS3</td>
</tr>
<tr>
<td>RD or WR (Backplane)</td>
<td>RD or WR (Backplane)</td>
</tr>
</tbody>
</table>

Table 3. Active Backplane Signals

ALE and Secondary ALE are the address latch enable from each respective processor; CS3 and SCS3 are the bus window chip selects that select a backplane access and signal the arbitrate that the processor wants the bus; and CNTR1 and CONTRA are the enables generated by the arbitrate circuitry.

The address/data lines are not enabled to the backplane unless all of the above signals are active. This combination of control lines also ensures a stable backplane before allowing the next operation to begin on the backplane. When neither processor wants the backplane (both are doing internal calculations etc.), all address/data lines are tri-stated.

Backplane Arbitration

The arbitration circuitry is used to decide which processor can have the backplane and which should wait until the other is off the backplane. The arbitration circuitry provides several of the control signals needed for proper operation of the backplane. The control signals are vital to prevent collisions or backplane contention between the two processors.

Special care had to be addressed when dealing with software VS hardware design. The software uses a special double read/double write involving only one op-code fetch. Should a processor collision occur, it was possible the arbitrate would give up the backplane in the middle of an operation such as this. Therefore ALE had to be taken out of the equation for the chip select which drives the arbitration, however ALE was needed for the fuse PROM's used, hence ALE was added to the equation for the backplane itself. This eliminated the problem of the arbitration giving up the bus prematurely, and also kept ALE in the fuse PROM equation. Table 4 gives the truth table for the control signals and the arbitrate scheme.

<table>
<thead>
<tr>
<th>CS3</th>
<th>SCS3</th>
<th>CNTR1</th>
<th>CONTRA</th>
<th>RDY1</th>
<th>RDY2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Micro 1 state present 1st

<table>
<thead>
<tr>
<th>RDY1</th>
<th>RDY2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

| 1    | 1    |

Micro 2 state present 1st

X= Don't Care

Table 4. Arbitration truth Table

RDY1 and RDY2 are "Ready" lines which are used to put the microprocessor to sleep (arbitrate the microprocessors) for less than 1 microsecond. The ready lines remain high unless a backplane collision between the processors occur. The truth table shows the characteristics based on which processor was on the backplane 1st.

The card was designed to allow both processors to operate internally, and only put one to sleep should both require the backplane at the same time. The CNTR signals are different in that they enable/disable the backplane as access is requested, which are part of the equation for the ready signals. The control signals remain in the same state until a change is forced by the other processor, in a sense it is the only communication between the two processors. The chip selects actually inform the arbitration that the processor is requesting the backplane; it is also the bus window. The arbitrate bases its decision on which processor requested the backplane 1st, and will turn the other OFF during a collision.
USARTS

The microprocessor board contains 4 Universal Synchronous Asynchronous Receiver Transmitters which act as the interface between the MUE, the instrument, GSE and SLV. Two of the USARTS are for ground support equipment and two are for the instrument, thus providing some redundancy. Either processor can access all 4 USARTS since they are considered off card. Due to the nature of the interrupt scheme it was necessary to keep the transmitter off unless the user actually needed to transmit. This cycling of the transmitter provides the microprocessor with an interrupt to alert the processor that transmission is complete and started.

Additional Registers

There are two additional registers that provide necessary information to the processors. They are located on the backplane so both processors can read them. They are defined as follows:

- **READ GSE STATUS** -- this register lets the software know that the GSE serial port is connected.
- **READ SLV STATUS** -- this register lets the software know when the launch vehicle has separated from the spacecraft. This register is pulled down until the launch vehicle separates and pulled up by interface.
- **SPACECRAFT WATCHDOG** -- this register is used by software to determine whether it should be the C&DH or the ACS processor. This register changes on a power on reset or "swap" command.

Both registers will always power up the same way.

Special Control Circuits

Special control circuits are needed to ensure setup times, delay times, and backplane timing constraints. The READY signals (originating from the arbitrate, to put a processor to sleep if needed) are gated to the microprocessor as shown in Figure 5.

This circuit is required to ensure the ready setup time of at least 250 ns to leading edge of the 2 MHz clock. This ensures that the ready line remains stable for at least 250 ns as required by the 8085RH specification.

The microprocessor reads and writes to the backplane are clocked to the backplane as shown in Figure 6. The delay of the read and write strobe was needed to accommodate a FIFO used on the Uplink/Downlink card in the

![Figure 5. RDY Line 250 ns Delay](image)

MUE. This clocks data in on the falling edge of read and write, making it necessary to ensure that the data and address lines are stable before clocking.

![Figure 6. - READ/WRITE to Backplane](image)

The 1 and 8 MHz clocks are muxed to provide redundancy. Should an oscillator fail, the other can be switched to by a spacecraft watchdog. This toggles a flip flop which will enable a separate buffer and disable the primary buffer, thus allowing the 2nd set of signals to the system as shown in Figure 7.
Memory 1 and 2 are identical from an electrical design standpoint. The boards each contain 32K bytes of PROM and 512K bytes of static RAM. The board address is jumper selectable and decoded and buffered locally. The Spacecraft Processor accesses this memory through the backplane. The devices used are radiation hardened 32K Byte SRAMS and 2K Fuse PROMS. Table 5 defines the physical address of MUE memory in the processor address space.

<table>
<thead>
<tr>
<th>MEMORY TYPE</th>
<th>MEMORY ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOARD 1 PROM</td>
<td>100000H - 107FFFFH</td>
</tr>
<tr>
<td>BOARD 1 SRAM</td>
<td>180000H - 1FFFFFFH</td>
</tr>
<tr>
<td>BOARD 2 PROM</td>
<td>600000H - 607FFFFH</td>
</tr>
<tr>
<td>BOARD 2 SRAM</td>
<td>680000H - 6FFFFFH</td>
</tr>
</tbody>
</table>

Table 5. - MUE Memory Address Locations

Housekeeping Board

The MUE Housekeeping Board is used to multiplex and condition 64 analog signals to a 12-bit analog to digital converter. In addition the board houses the ACS Magnetometer interface circuitry. Several MUE and Spacecraft parameters are monitored including voltages, currents, temperatures and status bits. Figure 8 shows the MUE Housekeeping Multiplexer.

ACS Sensor and Clock Board

The ACS Sensor and Clock Card provides several functions that interface or provide timing for both attitude determination and telemetry data generation. The first function is the Mission Elapsed Timer (MET) that provides reference timing for the different interfaces on this card. Specific timing signals required by the MUE and/or the experiment are derived from the outputs of the MET. The software adds a ground commanded offset to the MET to adjust the actual mission time. The second major function is to provide interface ports to the Spinning Sun Sensor (SSS) angle and time of occurrence, the Horizon Crossing Indicator (HCI) times of occurrence, and the magnetometer phase occurrences. The MUE uses these sensor inputs for attitude determination. The third function is an interface for obtaining the time of occurrence of the Barker Code Detect (BCD) signal. The ground operations system uses the occurrence of the Barker Code Detect signal time stamp to synchronize its internal time with ground station time. There are separate control and time interfaces for the two MUE processors to determine attitude and generate telemetry data. Finally there are control and status ports for interfacing to the Instrument Data
Processing Unit (IDPU) to control the on-board experiments.

The ACS Sensor and Clock Card is divided into the following circuits: Microprocessor Interface, Address Decoder, Reset/Oscillator Circuit, Mission Elapsed Timer (MET), Timing Signals Generator, Processor A Latch, Processor B Latch, HCI Space to Earth Latch and Interrupt, HCI Earth to Space Latch and Interrupt, Magphase Latch, BCD Latch, IDPU Control and Status Ports, SSS Input Buffers, SSS Latch and Interrupt, and Output Data Buffer. Figure 9 is a block diagram of the card.

FIGURE 9 - ACS Clock and Sensor Card

Uplink/Downlink Board

The Uplink/Downlink board provides a telecommunication channel that allows data to be transmitted from the MUE to the transponder and allows the MUE to receive uplinked commands.

Uplink

The Uplink functions of the Uplink/Downlink card provide the coding layer services of the CCSDS seven-layer architecture. The Uplink functions interface with the transponder Command Detector Unit (CDU) to establish a reliable, error-controlled data channel through which telecommand data bits may be transferred. The telecommand data is encoded to reduce the noise effects in the data's physical layer channel. The Uplink functions mimic the ground encoding techniques to provide command status verification to the next layer. The Command Link Transfer Unit (CLTU) data structure provides the codeblock synchronization and the delimits the beginning of the user data to the Uplink functions. The Uplink functions receive CLTUs consisting of a 16-bit start sequence, a series of codeblocks with correct Bose-Chaudri-Hocquenghem following (BCH) codes, and a tail sequence. The Uplink functions ensure normal data polarity of these CLTUs, pass them to the MUE upon command, and provide status of the card's internal operation. Additionally, the Uplink functions provide detect circuitry for a "critical command" which will swap the two processors. The Uplink functions also provide control pulses for the transponder functions.

The transponder provides four control signals to the Uplink functions: Detected Command Data, Bit Timing, Command Detector Unit (CDU) Lock, and Receiver Lock.

The Uplink functions, shown in Figure 10, operate in three states: Inactive, Search, and Decode. The card will be in the Inactive state until CDU Lock and Receiver Lock have occurred. It then transitions to the Search state until it detects the Start Sequence. The Start Sequence, which consists of a 16-bit synchronization pattern, 1110101110010000-Binary, can be sent normal or inverted to show the polarity of the data. The Uplink will normalize inverted data and signal the occurrence of the Start Sequence detection by generating a rising edge pulse labeled Barker Code Detect to the spacecraft processor. Once the Start Sequence has been detected, the Uplink functions transition to a Decode state. In this state, the Uplink functions transfer codeblocks into the card's codeblock FIFO.

The Uplink functions perform a parity check on each codeblock. The code used is a (63,56) modified BCH code that uses the generator polynomial, \( g(x) = x^7 + x^6 + x^2 + x^0 \), to produce seven parity bits. If a parity error is detected, the Uplink functions assert a flag that is stored in the codeblock FIFO along with the seven parity bits. All codeblocks are written into the codeblock FIFO regardless of their parity status. The Uplink functions show the presence of a codeblock in the FIFO by incrementing a counter. The Uplink functions return to the Search State upon detection of a parity error.

The Uplink functions also support the detection of a special command bit pattern known as the Critical Command. This 56-bit pattern is stored in the Uplink PROM. Each time a Start Sequence is detected, the Uplink functions perform a bit by bit comparison on the first 56 bits succeeding the Start Sequence and calculates its parity. If these bits and their Uplink parity are identical to those in the
PROM, the Uplink functions signal the occurrence of the Critical Command by producing a rising edge pulse to the MUE backplane. The Uplink functions only search the first codeblock after the Start Sequence for this command.

Downlink

The Downlink functions provide the channel coding layer of the CCSDS architecture. The Downlink card transmits telemetry at four different data rates (4.096 Kb/s, 900 Kb/s, 1.5 Mb/s, and 2.25 Mb/s) and supports four encoding options (NRZ-L, Biphase, Convolutional, and Convolutional-Biphase). Telemetry is input to the Downlink functions via the Instrument Data Processing Unit (IDPU) or the MUE backplane. In addition, the Downlink functions construct CCSDS transfer frames by inserting the Frame Synchronization Mark and the transfer frame trailer. The Downlink functions output telemetry to the transponder. The Downlink functions also provide operational status to the MUE.

The Downlink functions, shown in Figure 11 are controlled via the MUE software which selects the data rate, coding options, data input source, and output voltage amplitude. The software also enables and disables the Downlink functions.

When the card is enabled, it generates and downlinks the 32-bit Frame Synchronization Mark (1ACFFCID-Hex), the data, the Command Link Control Word (CLCW), and the 16-bit Cyclic Redundancy Check (CRC) in that order. The card ensures contiguous transfer frames by time-multiplexing data from four sources: the Downlink PROM, the IDPU or the MUE, the CLCW FIFO, and the CRC generator. The time multiplexing is controlled by signals stored in one of the card's PROMs. The MUE software controls which data source is downlinked by setting a bit in the card's control register. When the IDPU is selected as the data source, the Downlink functions generate a rising edge signal called Data Request to the IDPU to signal that the MUE is ready for data. This signal is followed by multiple clock pulses from the Downlink functions which enable synchronous data transfer. The MUE to IDPU downlink telemetry electrical interface is a three-wire, single-ended, non-redundant interface. When the MUE is selected as the data source, the Downlink functions accept data from the MUE backplane via a FIFO at the 4.096 KHz rate only. The Downlink functions retrieve the data from the FIFO and inserts it into the telemetry stream. Data transfer for this mode is asynchronous.

Following the data field of the transfer frame, the card transmits the CLCW which is written to a second FIFO by the MUE software.
Succeeding the CLCW, the 16-bit CRC is transmitted for error control. The CRC is based on the polynomial $x^{16} + x^{12} + x^5 + 1$ with the data and the CLCW as input.

The operation of the Downlink functions depends on three Programmable Read Only Memories (PROMs). PROM 1 and PROM 2 function as state machines that produce the signals required to retrieve data from the card's data FIFOs and the IDPU. These PROMs also contain the frame synchronization field and produce the signals required to control the channels on the card's multiplexing circuits.

The third PROM provides telemetry encoding. This PROM functions as a look up table whose values represent the bit patterns for all four codes (NRZ-L, Biphasic, Convolutional, and Convolutional-Biphasic).

The telemetry is output through the card's transponder interface circuit. This driver uses a weighted resistor configuration which is controlled through the card's control register to produce an output voltage waveform whose output voltage amplitude varies from 1.49 to 2.41 Volts (peak to peak), in approximate 0.02 Volt increments. The output impedance of the circuit is designed to be 50 ohms ±5% to match the input impedance of the transponder.

**Watchdog/Pyro Card**

The FAST Watchdog/Pyro card is designed to drive ten primary and ten redundant pyros and five primary and five redundant meltwires. A Spacecraft Watchdog Timer, three discrete non-volatile memory bits, three discrete ground support inputs, three spacecraft separation inputs, and two relay drivers are also included on the card. The card receives inputs from the microprocessor across a backplane and decodes each individual pyro or meltwire function in a three part sequence. The top four address bits are used to determine the board address and the lower five address bits are used to command the board. Figure 12 shows the pyro circuit function.

**Figure 11 - MUE Downlink Functional Block Diagram**

**Figure 12 - MUE Pyro Circuit**
To fire a pyro, three steps must be followed in the interest of safety. First, write data to specify which pyro is to be fired. This data is to be written to the correct Pyro Latch and the Redundant Pyro Latch. Next, the Arm_Pyros and Arm_Redundant_Pyros addresses need to be strobed to put +28 Volts on the Pyro Buses. This initiates two relay driver circuits that drive a non-latching relay for ten seconds. After this command, there must be a pause of 50 ms to allow the relays to settle. Finally, the Fire_Pyros and Fire_Redundant_Pyros addresses must be strobed. This initiates a timed pulses that fire the pyros for 250 ms. As a precaution, the Clear_Pyro_Latches address is normally strobed before these steps are taken.

Each pyro circuit is selected by a bit which enables the pyro. The path from latch to pyro is identical for each pyro circuit. The latch drives the anode of a photodiode inside an optoisolator. The cathode of the photodiode is tied to a ground by a 100-K ohm resistor and is also tied to an AC logic circuit that provides a 250-ms active low pulse to fire the pyro circuitry. A 64-Hz clock is the input for the frequency divider that provides the 250-ms pulse and provides a 1- and 2-second clock for the meltwire driver and the relay driver. The output of the optoisolator drives the input of a FET. A zener diode limits the optoisolator's output voltage to 27 Volts. There is one zener diode for each set of ten pyro circuits. Each input to the FET is protected by a 10-Volt zener from gate to source. The source of the FET goes out the connector to the spacecraft harness.

There are two 5-amp current limiting circuits, one for each set of ten pyros. The drains of the FETs are connected to the output of these current limiting circuits. The current limiting circuit is made of four components. They are a NPN power darlington transistor, a power zener diode, and two different wire-wound power resistors. The input power comes through a relay that provides unprotected battery voltage, called the pyro bus, to the circuit. The pyro buses are called Pyro Bus A and Pyro Bus B. Each provides power to one of the current limiting circuits. The pyro bus connects to the collector of the drive transistor and the smaller power resistor. The other end of the resistor connects to the base of the transistor. The cathode of the power zener diode is also connected to the transistor's base. The anode of the diode is connected to the circuit's output. The large power resistor connects to the emitter of the transistor and the output of the circuit. The actual path of the five amps is through the transistor and large power resistor. The zener diode is used as feedback to limit the current output. Provisions have been made to allow fine tuning of the output circuit if necessary by adjusting the voltage drop of the zener diode and the resistance of the large power resistor. To optimize the current limiting circuit, the voltage drop across the circuit must be kept to a minimum. Keeping the voltage drop low enables the circuit to provide the necessary current through a higher resistive load.

Meltwires

Meltwires are similar to those for firing pyros. The two differences are: first, the Clear_Pyro_Latches does not affect the meltwire latches; second, the address Initiate_Meltwire_Timing must be strobed before strobing the addresses for Arm_Pyros and Arm_Redundant_Pyros. Each meltwire firing circuit is driven by latched data bit. Data is latched in this chip by the processor, but the Output Enable is controlled by some AC logic. This logic consists of a D Flip Flop and a counter. The counter is driven by a 1-Hz clock, and after 16 seconds it turns off the output to the meltwires. One bit of the data latch drives one input of one of an eight-channel darlington drivers. These drivers are powered by the pyro buses and each output channel turns on a power darlington transistor that puts the voltage of the pyro bus minus the drop of the transistor across the corresponding meltwire. The same relay driver is used to provide the pyro bus power, but the input clock is divided by two by the Initiate_Meltwire_Timing command. Therefore, the relay drivers arm the pyro buses for twenty seconds rather than ten. This is needed for the sixteen second firing time of the meltwires.

Relay Driver

The relay driver is commanded by the processor. AC logic drives the input of an optoisolator, which drives the base of an NPN bipolar transistor. The transistor sinks current through the base of a PNP bipolar transistor, which has its emitter tied to the +28_VOLT_MUE power. This power transistor energizes the coil of a non-latching relay for 10 seconds, which arms the pyro bus. The ten second timeout is accomplished by combining a 4-second clock and a 2-second clock. Once this relay driver is initiated, it cannot be
restarted until the circuit has timed out. As stated earlier, the relay driver times out after twenty seconds for meltwire firing. After a twenty-second relay timeout, the input clock divide by two circuitry is disabled, and the 10-second timeout is enabled. The Clear Pyro Latch Command also clears the state of the timing circuitry and resets the relays to an off state.

Non-Volatile Memory

These three bits are stored in latching relays and will not change state during power cycling. This data is spacecraft information that will be read by the spacecraft processor after the MUE has powered up and will determine the state of the spacecraft before power was lost. After the spacecraft has been powered up for the first time on orbit, the status bits must be written to ensure correct data. The stored data is the last written state before launch.

**Coil Driver Card**

The FAST MUE Coil Driver card which drives the spin and precession magnetic torquer coils on the FAST S/C, is a digitally programmable, high compliance, current source. The design consists of two fully independent forward converter power stage topologies and two bi-directional, H-bridge amplifier stages that furnish regulated drive current to each torque coil assembly. An EMI filter, common to each coil driver circuit, is used to condition power from the 28V bus. The Coil Driver is interfaced via an on-card command-decoder logic network to the microprocessor bus on the MUE backplane. Address and data bits written to the interface circuit are used to select between the spin and precession coil driver stages, and to set both the magnitude and, in case of the precession coil, direction of coil current. The spin coil current is commutated autonomously by a magnetometer signal (i.e., the magphase input) from the FAST S/C.

Line regulation for each coil driver stage was accomplished with a fixed frequency, variable on-time control format, using a current-mode pulse width modulator (PWM). Each PWM controller operates at 125 KHz, and provides a variable duty-factor pulsed drive signal to an N-channel MOSFET power switch. The power transistor switch drives the primary winding of an associated power transformer that downconverts voltage from the 28V bus to the compliance voltage levels required by the coil loads. The compliance voltage produced by each converter stage is impressed across the combined H-bridge/torquer coil loads, and will adjust itself as required in order to maintain the coil current at its programmed level, despite variations in supply voltage (21 - 35 VDC) and variations in coil resistance (±20%) over temperature. In addition, L-C filters are employed on each power transformer secondary to provide energy storage and ripple attenuation at each programmable current level. Gate voltage drive to the high-side switches in each H-bridge is accomplished with charge-pump circuits, referenced to the positive output voltage rail in each converter stage. The charge-pumps consist of digital one-shot stages, Schmitt trigger buffers, and voltage multipliers. The one-shot networks are synchronized to the secondaries of each power transformer at 125 KHz.

The spin coil driver current is adjustable in 8 discrete steps from 0 to 283mA ±5% (approx. 42mA/step), and can be commutated in 2 directions by a FAST S/C magnetometer signal at repetition rates exceeding 1 Hz. The precession coil current is also adjustable in 8 discrete steps from 0 to 373mA ±5% (approx. 53mA/step) and is reversible with a logic command from the microprocessor bus. During operation, precision current sense resistors on the return side of each H-bridge provide a feedback voltage proportional to coil current that is compared with a programming voltage at a voltage error amplifier in the main control loop. The programming voltage is produced by a R-2R ladder network that serves as a 3-bit digital-to-analog converter for data written to the command decoder logic from the microprocessor bus octal latches are used to buffer data at the inputs to both the spin and precession coil drivers). The error amplifier's output voltage then drives the main current control loop. Note that the current-to-voltage programming sensitivity at the input to this amplifier is approximately 1.0 V/A for both the spin and precession coil drivers. This low sensitivity allows the amplifier's common mode voltages, at all current settings, to remain below the limit imposed by the +5V digital supply that operates the on-card AC logic and the R-2R ladder network. It also reduces the sensitivity of the control loop to cumulative amplifier offset voltages.

Since the spin/precession coil loads are transformer-isolated from the primary side-referenced (i.e., 28V ground return) power stages, the voltage feedback signal from the error amplifier is coupled across the isolation
boundary by means of a magnetic pulse feedback circuit. The feedback circuit for each power stage consists of a synchronous transistor inverter stage driving a low-power pulse transformer, whose primary winding samples the current control loop's error signal at the 125 KHz switching frequency. An additional, buffered unity gain amplifier stage is included between the error amplifier and the sampling network, in order to provide sufficient magnetizing current to the pulse transformer's primary. The secondary winding voltage is peak detected, filtered, and then attenuated to a level compatible with the 2.5V temperature-compensated reference furnished by each PWM controller. The PWM controller then width-modulates the drive pulses to the main MOSFET power switch and adjusts the overall duty-factor of the power stage to vary the output compliance voltage and maintain constant torque coil current.

Using this technique, regulation accuracy, at line voltage settings ranging from 21 - 35Vdc, falls easily within the ±5% tolerance limits specified for each S/C torquer coil. Additionally, the supply voltages to the op amp gain stages in the control loops for each coil driver were reduced to ±12V, in order to conform with device derating requirements. The use of magnetic pulse feedback also affords each coil driver's control loop protection from the damaging effects of ionizing and total-dose radiation.

Regarding fault detection capability, the use of the current-mode PWM controllers enables the spin/precession coil driver stages to limit fault or short-circuit currents on a pulse-by-pulse basis, and recover automatically upon removal of the fault. An active over-voltage detection network is also employed in each coil driver, using opto-couplers to isolate the threshold detecting circuitry from the PWM controllers in each power stage. These networks can provide auxiliary voltage feedback to either coil driver's PWM controller, in the event that a voltage feedback loop fails and a power stage attempts to operate open loop. This will ensure that the output compliance voltage across the H-bridge PWM amplifier stages remains at a non-destructive level below 30V.

Finally, telemetry amplifiers are provided for each coil driver stage, in order to furnish bipolar voltage signals proportional to the magnitude and direction of current in each torquer coil. The op-amps configured as single-ended inverting amplifiers and single-ended inverting amplifiers are used to sense the voltage across each pair of 2.0 ohm current-sense resistors on the return side of each bi-directional H-bridge. The gain of each amplifier is set at 10V/V, resulting in an overall scale factor of 20V/A for telemetry purposes, and S/C level control of the FAST magnetic torquer coils.

**DC to DC Converter Card**

The FAST MUE DC-DC Converter is a redundant design that consists of two identical, transformer-isolated, feed-forward power stage topologies, that share a common input EMI filter and an array of common L-C output filter components. Each power stage/filter combination is designed to furnish power to the Mission Unique Electronics (MUE) box printed wiring board assemblies at the following levels: +5V at 1.5A, and ±15V at ±0.15A. The total 12W load demand per power stage includes the probable loading effects of both ionizing and total dose radiation over a 1 year mission duration. The tolerances on the 5V digital and ±15V analog outputs, over a 21 - 35V input voltage range and the maximum specified load excursions, are ±5% and ±3% respectively. Peak-to-peak switching ripple and common-mode noise is approximately 50mVpp for each regulated output.

Input power from the 28V bus can be steered to either power stage (i.e., Converter A or B) via a DPST magnetic latching relay. Relay status is determined by a CMOS counter/switchover logic circuit that is actuated by a "watchdog timer" signal from the MUE Housekeeping Card. In response to a watchdog timer signal, the switchover logic will disable the on-line power stage (i.e., converter "A") and, following a 10 sec. delay interval, enable the redundant power stage (converter "B"). The switchover logic can thus toggle repeatedly between either converter in response to periodic watchdog timer commands (which may occur at 24 hr. intervals during a S/C safehold condition). At turn-on, following the initial application of 28V power to the DC-DC converter board, converter "A" is enabled by default. Provisions were also made to disable the Spin/Precession Coil Driver Card during the 10 sec. delay interval, in order to protect on-card power stage and control circuitry.

Line/load regulation for each power stage was accomplished with a fixed frequency, variable on-time control format, using the current-mode
pulse width modulator (PWM). Each PWM controller operates at 125 KHz, and provides a variable duty-factor pulsed drive signal to an N-channel MOSFET power switch. The power transistor switch drives the primary winding of an associated power transformer that down-converts voltage from the 28V bus to the +5V and ±15V levels (i.e., accounting for rectifier diode drops and backplane distribution losses) required by the MUE ACS loads. In addition, each regulated output has a L-C filter stage to provide energy storage and ripple attenuation at its anticipated load demand, and a secondary common/differential-mode filter to suppress high frequency switching transients.

To maintain constant output voltage, the PWM controllers modulate the duty-factor of each power stage by comparing a dynamic feedback signal proportional to the peak current in each power transformer primary with a control voltage threshold, that is determined by feedback from the +5V digital output. The resulting nested control loop scheme enables the converters to respond, on a pulse-by-pulse basis at 125 KHz, to both wide input voltage excursions on the 28V bus and wide variations in output load demand. The control loop parameters will vary in such a manner as to maintain a constant output voltage within the limits imposed by component tolerances, amplifier offset voltages, and control loop gain. The primary current control loops, on both converters also have the ability to provide short circuit protection for each regulated output.

Since the +5V and ±15V outputs are transformer-isolated from the primary side-referenced power stages, the voltage feedback signal from the +5V digital output is coupled across the isolation boundary by means of a magnetic pulse feedback circuit. The feedback circuit for each power stage consists of a synchronous transistor inverter stage driving a low-power pulse transformer, whose primary winding samples the +5V output at the 125 KHz switching frequency. The secondary winding voltage is peak detected, filtered, and then attenuated to a level compatible with the 2.5V temperature-compensated reference furnished by each PWM controller.

An active over-voltage detection network is also employed on the +5V output, using opto-couplers to isolate its comparator stage output from the controllers in each power stage. This network can provide auxiliary voltage feedback to either controller stage (converter "A" or "B") in the event that a voltage feedback loop fails and a power stage attempts to operate open loop. This will ensure that the +5V digital output never exceeds the 6V maximum operational limit specified for the MUE box AC-logic loads, and constrain the ±15V analog outputs to non-destructive levels below ±17V.

Finally, telemetry amplifiers are provided in order to furnish voltage signals proportional to the load demand on each regulated output. Op-amps configured as single-ended non-inverting amplifiers (+5V and +15V current monitors) and a single-ended inverting amplifier (-15V current monitor) are used for telemetry. Current sense resistors (0.1 ohms for the 5V output and 1.0 ohms for the ±15V outputs) are located on the ground return side of each regulated output. The resulting scale factor for each amplifier stage is 20V/ampere.

**Battery Charge Control Card**

The Battery Charge Control (BCC) provides circuitry to provide Voltage/Temperature (V-T) Control, Current Control, Overvoltage Control and a precision current monitor that is used as the sensor for a software Amp Hour Integrator. The BCC Card is shown in Figure 13.

![Figure 13 - BCC Card Block Diagram](image)

The BCC holds eight relays which are used to enable and configure the state of the controller. All relays are magnetic latching to hold states in between modes and commanded configuration changes. The MUE software reads the top, bottom and half voltages of the battery approximately once per second. If the voltage is out of tolerance for three cycles the MUE software will shut down non-essential loads. The charge control card drives an external and redundant sequential shunt regulator. The voltage and temperature controls are monitored and controlled according to the V-T levels shown in Figure 14.
The battery used on the FAST spacecraft is a 9 ampere-hour battery. The constant C represents the current time capacity of the battery. In this case C = 9 Amp-Hours. In this case the maximum charge rate is limited to C. In the Trickle charge mode the charge rates are selected to either C/50 or C/100.

In V-T control mode when the battery reaches the selected voltage limit the V-T Controller will activate the shunt regulator. The battery temperature is read from platinum wire temperature sensors located in the battery. Sixteen different V-T levels are available and commandable from the ground.

The Overvoltage controller will activate the shunt regulators when the battery approaches 34.5 ± 0.5 VDC.

Power Distribution Card

The Power Distribution Card provides 11 relays that apply 28 Volt power to the experiment, deployment mechanisms, heaters and ACS sensors. The relays used are magnetic latching relays and are commanded from the ground through the Spacecraft Processor. In addition the card provides analog multiplexing capability to send PSE housekeeping data to the ADC on the Housekeeping Card. All loads are routed through an fuse connector that is accessible at the FAST umbilical connector. Anti-magnetic design techniques were used to minimize large current loop areas which would contribute to magnetic fields. Particular attention to cabling layout, twisted pairs, shielding and PC layout techniques was made during design and fabrication.

PSE End Panel

The PSE End Panel holds higher current magnetic latching relays used to connect the battery, select shunt drivers, enable pyros and meltwires. Figure 15 shows the function.
MUE System Interconnection

The MUE was designed to interconnect all satellite subsystems. Each card has connections and interfaces with other subsystems as shown in Figure 16. The direct energy transfer system or 28 VDC spacecraft bus is connected through the MUE PSE elements and redistributed to other spacecraft loads and subsystems. The devices that can be removed from the bus without affecting satellite operation are considered Non-Essential loads and are switched and interconnected through the Non-Essential Bus (NEB).

Since a major goal of the MUE design was to minimize magnetic contributions to the spacecraft, careful consideration was made with respect to signal returns and isolation between various subsystems. Figure 17 represents the power distribution and grounding philosophy of the MUE.

The MUE Motherboard distributes power and ground to the various cards within the MUE. The local power for the MUE is isolated and filtered by the DC/DC Converter Card. In addition the 28 VDC Bus is filtered with bulk capacitors located on the MUE End Panel Card.

Shielding of the Coil Driver and DC/DC Converter Cards is provided by printed circuit card ground planes and metallic shield enclosures. The net result is good performance in EMI testing and Magnetic Field Compliance Testing.

Figure 16 - MUE Connector Locations
Conclusion

The MUE has been developed and integrated into the FAST satellite which is currently on hold for a launch date. The testing program proceeded well and the MUE has met its stated operational requirements.

Given the combination of requirements including space environment, radiation tolerance requirements and electromagnetic contamination requirements, the MUE represents a consolidated package which operates at very low on orbit average power that can be used to control a spinning type satellite providing rotational information from the Horizon Crossing Indicator, Spinning Sun Sensors and Magnetometer.

The real time software developed for the MUE was designed with modularity and expansion in mind. To date it has been thoroughly tested and demonstrates robust functionality. It represents a set of spacecraft management and telemetry functions that can readily be adapted to similar spacecraft applications. Given current part availability, the PROM space on the Spacecraft Processor Card and the Memory Cards can be expanded to meet more complex software requirements.

In the future the MUE concept can be used as a design basis and readily modified to perform any combination of spacecraft management functions. Designs from other satellite programs can readily be incorporated into the MUE card form factor. The number of cards could be expanded to add more sensor and actuator interfaces. The external shunt driver can be designed to handle larger power systems. In some instances circuitry in the MUE could be consolidated using programmable logic arrays which are now available in more radiation tolerant configurations.
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