A Spacecraft Computer for High-Performance Applications

John M. Stone*
and
Joseph L. Kroesche Jr.**
Southwest Research Institute, San Antonio, Texas 78228

A high-performance processor circuit called the SC-3 has been developed to meet the requirements of advanced experiment and attitude control applications. It is based on the 16 MHz Intel 80386/80387 chip set and implements a dual bus system configuration which allows high-speed, 32-bit wide memory and low-speed, 16-bit wide Input/Output(I/O) circuits to be separated. This separation maintains compatibility with a wide range of current I/O circuit designs while exploiting the high-bandwidth memory access capabilities of the 80386. Performance is further enhanced by means of a cache on the 32-bit bus. Gibson, Whetstone, and Dhrystone instruction mixes have been used to evaluate performance under various operating modes. When the SC-3 is constrained to execute from 16-bit memory, the Gibson mix indicates a 32% performance improvement compared to previous 16-bit processors. An average of 1.1 million Whetstones per second are performed over the typical range of memory wait states. The average Dhrystone performance improvement between 32-bit non-cached and 32-bit cached operation over a typical range of memory wait states is 115%. The initial application of this processor circuit is on Stanford University's Gravity Probe-B experiment.

Introduction

The invention of the microprocessor in the mid 1970's, and the availability of large semiconductor memories, revolutionized the computer industry and greatly affected space-flight hardware design efforts. It allowed the development of a generation of computers which were smaller, cheaper, more power efficient, and often more flexible than those of the previous generation. The characteristic advantages of these microcomputers made them very attractive to designers of spaceflight hardware, and they soon became an integral part of attitude and experiment control systems on many missions. Their small size and low power consumption allowed them to be used in applications where their bulky and power hungry predecessors could not, and their programming flexibility fostered the design of increasingly sophisticated instruments and spacecraft.

Southwest Research Institute (SwRI) has been involved in the development of space-flight hardware since the mid-1970's. It offered its first space-flight qualified, general purpose data processing unit in 1982 [1]. This computer (called the SC-1) was originally designed to be used in place of the NASA Standard Spacecraft Computer II (NSSC-II) on the Space Experiments with Particle Accelerators (SEPAC) component of the Spacelab 1 mission. Several revisions of this computer were produced, as was a repackaged derivative (the SC-2). Prominent characteristics of these computers are summarized in table 1. The SC-1 and SC-2 have found numerous applications as attitude and experiment control processors on both NASA and SDI missions.

The SC-1 and SC-2 are too limited in terms of memory size and bus width, clock speed, and numeric capabilities to meet the demands of many increasingly complicated

*Senior Research Engineer, Instrumentation and Space Research Division, P.O. Drawer 28510, San Antonio, TX 78228-0510

**Research Engineer, Instrumentation and Space Research Division, P.O. Drawer 28510, San Antonio, Texas 78228-0510

experiment and attitude control applications. For experiments which quickly accumulate large amounts of data and have either a limited telemetry bandwidth or only periodic access to data transmission resources, huge amounts of data may need to be stored while waiting for post-processing and data transfer to occur. The amount of stored data, when combined with the memory required to run the various control algorithms, can easily require more than a total 1 Mbyte of memory. Additionally, the algorithms necessary to process this raw data into a manageable size (an FFT for example) depend strongly upon the numeric capabilities of the processor, and the 8087 numeric co-processor is relatively slow and inefficient compared to newer numeric co-processors. The limited memory bandwidth and relatively slow clock speeds of both the SC-1 and SC-2 place an unacceptable limit on their ability to satisfy the requirements of many advanced experiment control applications. In attitude control applications, the lack of direct 8087 support for some trigonometric functions degrades performance. Additionally, for relatively complicated attitude control requirements, or attitude control algorithms that depend upon a large number of input signals, the execution speeds of the SC-1 and SC-2 are barely adequate or, in some cases, totally inadequate.

In order to meet current and future performance requirements for space-flight computers, SwRI has developed a new processor circuit. Several considerations influenced the design of this circuit: the need to remove the aforementioned speed and memory limitations, the need to maintain bus level compatibility with previously existing I/O circuits to avoid costly redesigns, the need to provide a circuit which would fit into a variety of single- and multiple-board computer configurations, and a desire to provide a familiar software development environment to the end user. These considerations imposed an evolutionary design approach which allowed us to develop a circuit meeting the performance improvement requirements, while maintaining a significant level of hardware and software compatibility with the SC-1 and SC-2 and providing the flexibility necessary to integrate it into new designs.

The resulting circuit is called the SC-3. This paper discusses the overall design of the processor circuit, outlines and presents the results of the performance evaluation tests, briefly describes the first flight implementation of the circuit, and presents proposed future developments.

Table 1. SC-1 and SC-2 Configuration Summary

	SC-1	SC-2
Central Processor:	8086	8086
Numeric Processor:	8087	8087
Clock Speed:	5 MHz	8 MHz
Physical Memory Size Limit:	1 Mbyte	1 Mbyte
Data Bus Width:	16 bit	16 bit
Configuration:	Single board computer containing fixed memory and support resources with attached expansion chassis for custom I/O circuits.	Multiple board backplane oriented computer with configurable memory, I/O and processor support resources (16, 20, or 40 card slots).

Hardware Description

Overview

The SC-3 processor circuit is based on the Intel 80386/80387 chip set, which is used in many IBM and IBM compatible PC's. The 80386 has a 32-bit data bus, which doubles the 8086 bus width, and a 32-bit address bus which provides a 4 Gigabyte potential physical address space. It also executes code more efficiently than the 8086. The 80387 contains several enhancements over the 8087, including direct support for all trigonometric functions and more efficient floating point execution. Finally, the 80386 and 80387 are upwardly compatible with the 8086 and 8087, which means that the SC-3 will execute non-hardware dependent code developed for the SC-1 and SC-2. Choosing the 80386/80387 chip set for the SC-3 processor circuit alleviates the memory space and numeric processor limitations present in the SC-1 and SC-2 and provides a familiar software environment for any end-user familiar with a PC or previous SwRI computers.

The SC-3 processor circuit, which runs at 16 MHz, can perform a no-wait state 32-bit memory access in 125 ns. The fastest no wait state 16-bit access performable by an SC-2 is 500 ns. From these figures, the SC-3 provides a best case 8-fold increase in memory access time, with a proportional increase in performance. The performance improvement indicated by the raw memory access speed is not realizable in practice, but it provides an upper bound for the actual performance improvement. The potential improvement is limited by the need to maintain compatibility with current I/O circuit designs, the need for a flexible system configuration, the need to provide Error Detect and Correct (EDC) circuits on program memory, and the timing limitations imposed by the available electronic parts.

The SC-3 processor circuit implements a dual bus computer with a cache provided for program and data memory (see figure 1). One bus is 16 data bits wide and provides access primarily to I/O and processor support circuits

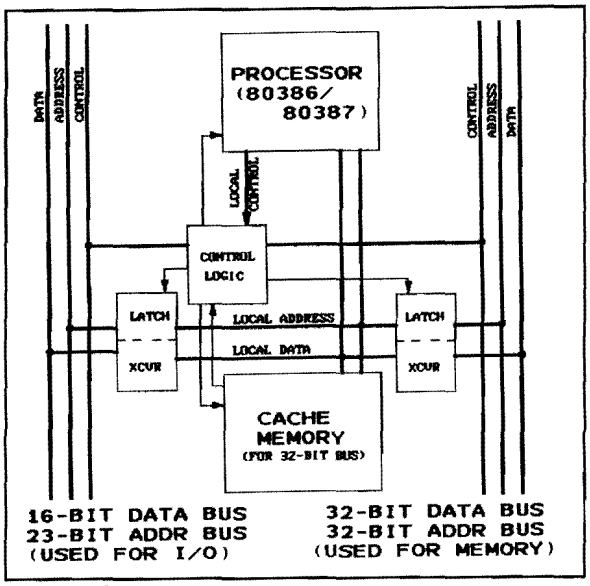

Figure 1.

(timers and interrupt controllers). The other bus is 32 data bits wide and is designed for interfacing to program and data memory and to fast, wide bandwidth I/O circuits. The address space allotted for each bus is configurable via programmable logic. The dual bus configuration allows the computer's resources to be split along natural divisions. Input/Output circuits, which are relatively slow, accessed infrequently, and seldom require or provide more than 16-bits of information at a time, are separated from program and data memory resources, which are much faster, accessed frequently, and use a full 32-bit data width. The dual bus system maintains compatibility with previous I/O designs, and simplifies decoding, control signal generation, cache design, and EDC memory design in computers containing the SC-3 processor circuit.

Bus Descriptions

The SC-3's 16-bit bus is signal and timing compatible with the SC-2's bus which allows all I/O and processor support circuits developed for the SC-1 and SC-2 computers to be used in SC-3 based computers. Maintaining this compatibility slows down accesses to the I/O bus, but separating these circuits from program

and data memory resources minimizes the impact on overall system performance. The design of this bus allows the addition or subtraction of I/O and processor support resources without affecting the high speed memory section of the computer. Additionally, a small circuit modification and the implementation of an arbitration circuit would allow the inclusion of a dedicated I/O processor to decrease the load on the SC-3 circuit for exceptionally heavy I/O access requirements.

The SC-3's 32-bit bus is intended to accommodate main memory and any new I/O designs which need the fast access and wide bandwidth of the full 32-bit bus. Separating this bus from the 16-bit bus allows memory resources to be modified without requiring a change in the I/O and processor support circuitry. Because the 32-bit bus is not constrained by any compatibility requirements, it is optimized to take advantage of the shorter bus access time possible with the 80386. Because of device limitations, the fastest possible normal memory access introduces 1 wait state (basically, the round-trip ready generation time). In reality, almost all accesses will introduce additional wait states because of the need to provide EDC for main memory. The relatively slow access times provided by most large non-volatile memory technologies also limit the performance of this bus. To remove as much of the performance penalty introduced by the wait states as possible, the SC-3 processor circuit implements a cache memory sub-system on 32-bit memory. The cache system and 32-bit bus memory design combine to exploit the performance advantages inherent in the 80386/80387 processor chip set.

Cache Description

The cache implemented by the SC-3 processor circuit may be configured by programmable logic to cache an arbitrary amount of 32-bit memory. It may be disabled, or its entries may be invalidated, under software control. Zero wait-state cache hit operation is implemented by using the 80386's address pipelining mechanism. The relatively large cache size, together with the typical structure of most software- highly 'local' programs, more frequent memory reads than writes, and few back to back memory writes, allows the direct mapped, posted write configuration of this cache to provide significant performance improvement over a non-cached design. The SC-3 cache characteristics are outlined in table 2.

Table 2. SC-3 Processor Circuit Cache Design Characteristics

Total Size:	32 kbytes
Line Size:	4 bytes
Mapping:	Direct
Write Policy:	Write Through (Posted)
Wait States:	
Read Hit:	0 (125 ns total cycle time)
Read Miss:	Dependent on main memory access time
Write:	0 (preceded by a read)
	Dependent on main memory access time (when preceded by another write)
Desired Hit Rate:	> 85%

Performance Evaluation

Methodology

Three standard performance benchmarks were used to evaluate the performance of the SC-3 processor board: the qualified Gibson mix [2], the Whetstone mix [3], and the Dhrystone 2.1 mix [4,5]. The Whetstone and Dhrystone mixes were compiled using the Metaware High-C compiler. To allow this evaluation under various conditions, the SC-3 was installed in an SC-2 backplane containing a 16-bit memory board and a UART/Timer Board, both of which are SC-2 compatible. A 32-bit memory card with 512 kbytes of RAM and 128 kbytes of UVPROM, capable of introducing 2 to 5 wait states (typical for most EDC), was attached to the 32-bit bus. This configuration provided the necessary timer resources to determine performance test execution time and allowed the SC-3 16-bit bus performance to be compared to the original SC-2 CPU performance. It also allowed benchmark performance for SC-3 32-bit non-cached, and 32-bit cached memory accesses to be calculated and compared over a realistic range of induced wait states. An in-circuit emulator was used to simplify program loading and execution.

The qualified Gibson mix was used to analyze the performance improvement inherent in the change from the 8086/8087 processor pair to the 80386/80387 processor pair when the latter is limited to an SC-2 bus compatible access. This code was inserted into the 16-bit memory board and executed by both the SC-2 CPU card and the SC-3 processor circuit. The results are tabulated and discussed in the next section.

The Whetstone and Dhrystone mixes were used to compare performance between the SC-3 executing code on the 32-bit bus and typical desktop computers. The Dhrystone benchmark was also used to evaluate the performance increase introduced by the SC-3's cache. To give results which are valid over the typical range of response times provided by EDC memory systems, the programs were executed with the 32-bit memory board introducing 2 and 5 wait states. The results are tabulated and discussed in the next section.

Results and Discussion

The qualified Gibson mix results are presented in Table 3 and show a 32% performance increase due to the processor upgrade. The test was conducted using the same binary executable image running out of 16-bit memory. This ensured that the change in performance was solely due to the change in microprocessors.

The Dhrystone 2.1 benchmark was used to determine SC-3 performance in different cache and memory configurations and to provide a comparison with 25 MHz and 33 MHz desktop 386 personal computers. The C source code was used exactly as distributed by Weicker [5,6] with the exception that operating system dependent features were removed. These were the calls to malloc() and the use of console I/O. None of the source within the measurement loop was changed. As can be seen from Table 4, performance improved by 70% when the cache was used with 2 wait-state memory, and by 159% with the 5 wait-state memory. This is a result of the decrease in the time of an average memory access when the cache is used. It should be noted that the Dhrystone program is smaller than the cache and after one pass through, all of the code and read-only data would reside entirely in the cache. This is why there is very little performance difference between the 2 and 5 wait-state tests when the

Table 3. Gibson Performance Summary

Machine	Performance 10^3 Gibson Operations/Second
SC-2 (8086/8087)	539
SC-3 (386/387)	713

Table 4. Dhrystone 2.1 Performance Summary

Configuration	Performance Dhrystones/Second	Ratio Perf./Clock Freq(MHz)
SC-3, 32 bit memory, 2 wait states, non-cached	3902	244
SC-3, 32 bit memory, 2 wait states, cached	6620	414
SC-3, 32 bit memory, 5 wait states, non-cached	2533	158
SC-3, 32 bit memory, 5 wait states, cached	6564	410
25 MHz 386 PC-AT clone	10638	426
33 MHz 386 PC-AT clone	13514	410

cache was used. The 5 wait state memory is probably more representative of a main memory with full error detection and correction capability. When compared to a desktop 386 PC, the SC-3 Dhrystone performance scales almost linearly with clock speed when the cache is used. To illustrate this, the ratio of Dhrystone performance to clock speed is also presented in Table 4. The PC's tested were also equipped with caches that can hold the entire benchmark program.

Floating point performance is measured using the Whetstone benchmark which executes a sequence of floating point intensive instructions. The results are presented in table 5. The Whetstone source was the same on the PC and the SC-3. Although it was linked differently for the two systems, the actual measurement loop execution was unchanged. The SC-3's Whetstone performance did not compare as well to the desktop 386 PC as did its Dhrystone performance. However, it should be noted that the SC-3 cache was not used for this test. Additional testing using the cache should show a performance improvement similar to that of the Dhrystone. The Whetstone's performance change between 2 and 5 wait states was not as great as the change for the Dhrystone, implying that it is more compute bound.

Initial SC-3 Flight Implementation

The initial flight implementation of the SC-3 processor circuit is as the Dedicated Experiment Processor (DEP) for the Shuttle Test Unit (STU) portion of Stanford University's Gravity Probe-B (GP-B) experiment. This

Table 5. Whetstone Performance Summary

Configuration	Performance 10^6 Whetstones/Second	Ratio (x 1000) Perf./Clock Freq.
SC-3, 32 bit memory, 2 wait states, non-cached	1.244	77.8
SC-3, 32 bit memory, 5 wait states, non-cached	0.966	60.4
25 MHz 386 PC-AT clone	2.500	100
33 MHz 386 PC-AT clone	3.302	100

experiment is intended to experimentally verify Einstein's general theory of relativity. The STU is intended to validate the hardware to be used prior to its installation in a free-flying satellite. The GP-B DEP, built around the SC-3 processor circuit, is responsible for collecting time sequence and housekeeping data from the experiment's gyroscope systems, performing FFT calculations on the gyroscope spin data, and packeting and managing the telemetry stream. The STU DEP has 1.640 Mbytes of memory and over 400 I/O channels (analog and digital combined). This computer is an example of the application for which the SC-3 processor circuit was designed.

Conclusions

SwRI has developed a dual-bus, 16 MHz 80386/80387 based processor circuit, called the SC-3, which maintains bus compatibility with previously developed I/O and processor support circuits without affecting the overall performance improvement provided by the 80386/80387 processor chip set. It accomplishes this by implementing a 32-bit cached memory bus separated from the 16-bit compatible bus. The dual bus design gives it the flexibility to be customized to a wide variety of applications. Standard benchmark tests have been run to quantify the relative performance of the new circuit. The results, presented elsewhere in this paper, demonstrate that the SC-3 provides a level of performance consistent with that of commercially available 386 based-PCs and better than previous spaceflight computers. The initial flight implementation of this processor circuit is as the GP-B STU DEP.

Planned Additional Work

Additional testing, with test programs bigger than the size of the cache, is planned in order to give a more accurate evaluation of the performance improvement provided by the cache. An attempt will also be made to integrate the processor control state machines, currently contained in nine Programmable Logic Devices(PLD), into fewer devices. This will be accomplished either by designing a gate array, or by using advanced PLDs as they become available. The results of this repackaging will be lower power consumption, reduced chip count, and faster operation, which will in turn allow increasing the processor clock speed.

Acknowledgements

We would like to thank M. Sattler, B. Piepgrass, R. Youngblood, B. Stone, J. Cornelius, and K. Matull for technical and logistical support during this project. This project was wholly funded by the SwRI Advisory Committee for Research (project 15-9594). Deep thanks go to the committee and Ed Hayden, the project mentor.

References

1) Gibson, W. C., "The Development of a Low-Power Spacecraft Data System," Southwest Research Institute, San Antonio, Texas, December 1983.

2) Carney, Phillip C., "Selecting On-Board Satellite Computer Systems," *Computer*, Vol. 16, No. 4, April 1983, pp. 38-40.

3) Curnow, H. and Wickman, B., "A Synthetic Benchmark," *The Computer Journal*, Vol. 19, No. 1, February 1976, pp. 43-49.

4) Weicker, R.P., "Dhrystone: A Synthetic Systems Programming Benchmark," *Comm. ACM,* Vol 27, No. 10, Oct. 1984, pp. 1013-1030.

5) Weicker, R.P., "Dhrystone Benchmark: Rationale for Version 2 and Measurement Rules," *SIGPlan Notices,* Vol. 23, No. 8, Aug. 1988, pp. 49-62.

6) Weicker, R.P., "An Overview of Common Benchmarks," *Computer,* Vol. 23, No. 12, Dec. 1990, pp. 65-75.