

Rapid Development of Electronic Systems for Space Applications

AIAA/USU Conference on Small Satellites

M. Brett McMickell, Ph.D.

Thom Kreider, Lindsay Harding, Ron Strong, Brad Mouring, Kosta Ilic

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Complexity versus Abstraction

"It is estimated that 50% of the functionality in future satellite systems will be instantiated in FPGAs"

-US Air Force Research Laboratory

"..we no longer have humans writing those codes line by line."

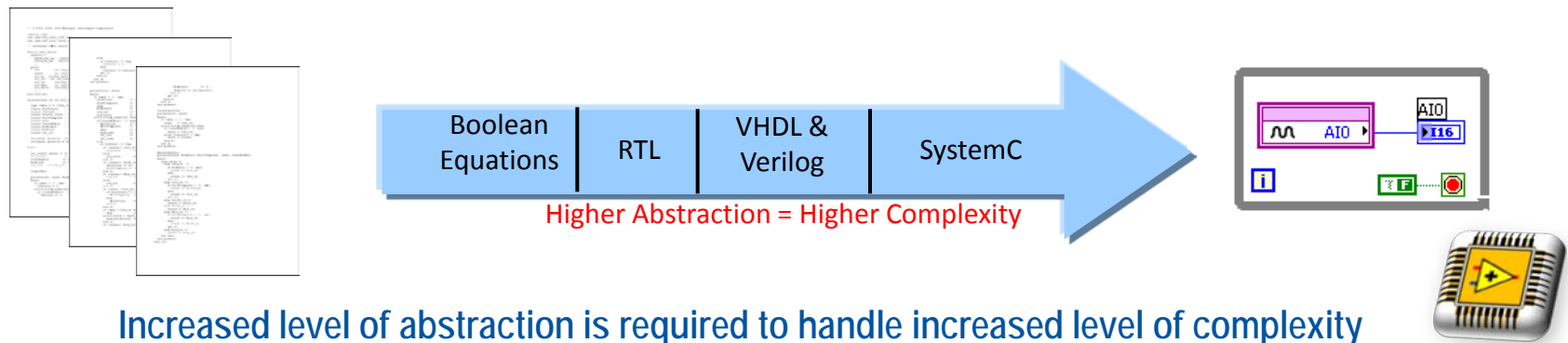
"If those lines were still written by humans, the number of errors in them would be so large that we couldn't build those millions of lines of code."

-Dr. Werner Dahm, Chief Scientist of Air Force, AIAA America October 2010

Scalability of Existing FPGA Tools will Drive a Cost/Schedule Explosion at these levels of Complexity

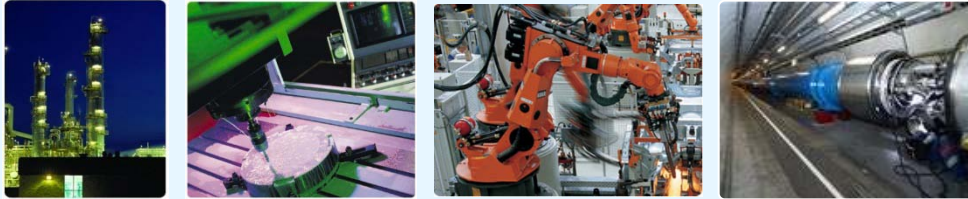
Higher Order Abstraction Enables the Management of Associated Increase in System Complexity

LabVIEW FPGA - Commercial Success due to Reliable Abstraction of the FPGA Development Process



Increased level of abstraction is required to handle increased level of complexity

Leverage Successful *Commercial* Technology for *Space*



National Instruments - Commercial & Industrial FPGA Products



R Series Multifunction RIO
 • General Purpose I/O for Measurement and Control



NI CompactRIO
 • Industrial Control and Monitoring



NI SingleboardRIO
 • Embedded Systems

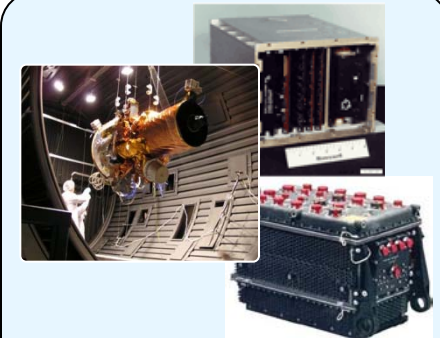


NI FlexRIO
 • Manufacturing Test and Design Validation



Other
 • RIO IF Transceiver
 • PCIe Framegrabbers
 • Compact Vision System

Full Spectrum with LabVIEW FPGA



Honeywell Defense & Space



Honeywell RDE
 •Rugged Embedded Systems
 •Path to Space

Honeywell's Responsive Digital Electronics

General Specifications

- 3.1W measured board-level, operational power
- Xilinx Rad-Hard Virtex-5QV or Industrial FX130T FPGA Options
- LabVIEW FPGA 2011 graphical programming
- Xilinx ISE 12.4

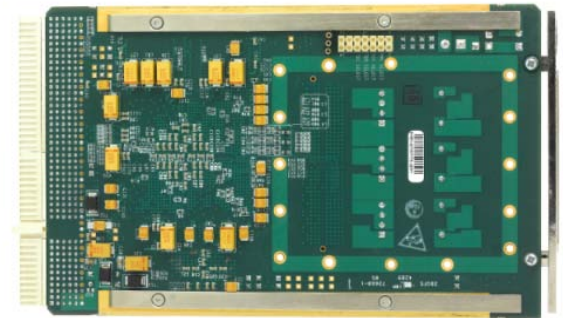
- Conduction Cooled, Rugged 3U CompactPCI form factor
- Vacuum-rated VITA-57 FMC 'High Density' user I/O connector
- Conduction and Convection cooling compatible

- 160 single ended or 80 50-ohm differential pairs,
- 4 GTX pairs - 3 Gbps high-speed serial channels
- 64-bit, 33MHz cPCI interface bus capable of bus mastering

- 40 MHz oscillator with 5 programmable Phase-Locked-Loops (PLLs)

- 512 Kword, 32-bit word SRAM, 10nSec access*
- 512 Mbit, 16-bit word User Flash ROM with page mode*
- 512 Mbit, 16-bit word FPGA configuration Flash ROM*
- 8 - 64Mbit externally selectable FPGA configuration images with auto-failover
- JTAG and in-service programming options via user-configurable channels

* User accessible and controlled at any time after FPGA is configured and running



Compatibility with NI FPGA Ecosystem

Responsive Digital Electronics (RDE)

Standard cPCI connectors

Compatible with NI PXI-1042 Chassis for power & cPCI

Double cPCI slot width

FMC Breakout boards

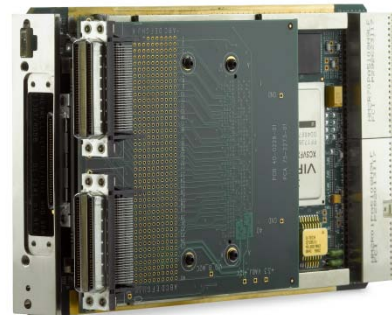
Compatible with R Series DIO connectors

Lower breakout – 1x 40 DIO

Upper breakout – 4x 40 DIO



RDE & Upper Breakout installed in NI PXI-1042 chassis with NI 6868-RDIO cable and SCB-68 chassis. NI PXI-7854R board (left)



RDE, left to right, bare board, with Lower Breakout board, with Upper Breakout boards



NI PXI-7813R with 160 DIO

Thrust Control System Demo Overview

Goal: Implement *Thrust Control System* (TCS) on the RDE

RDE controls the roll, pitch and yaw actuation for a thrust control application

Four solenoid driven valves

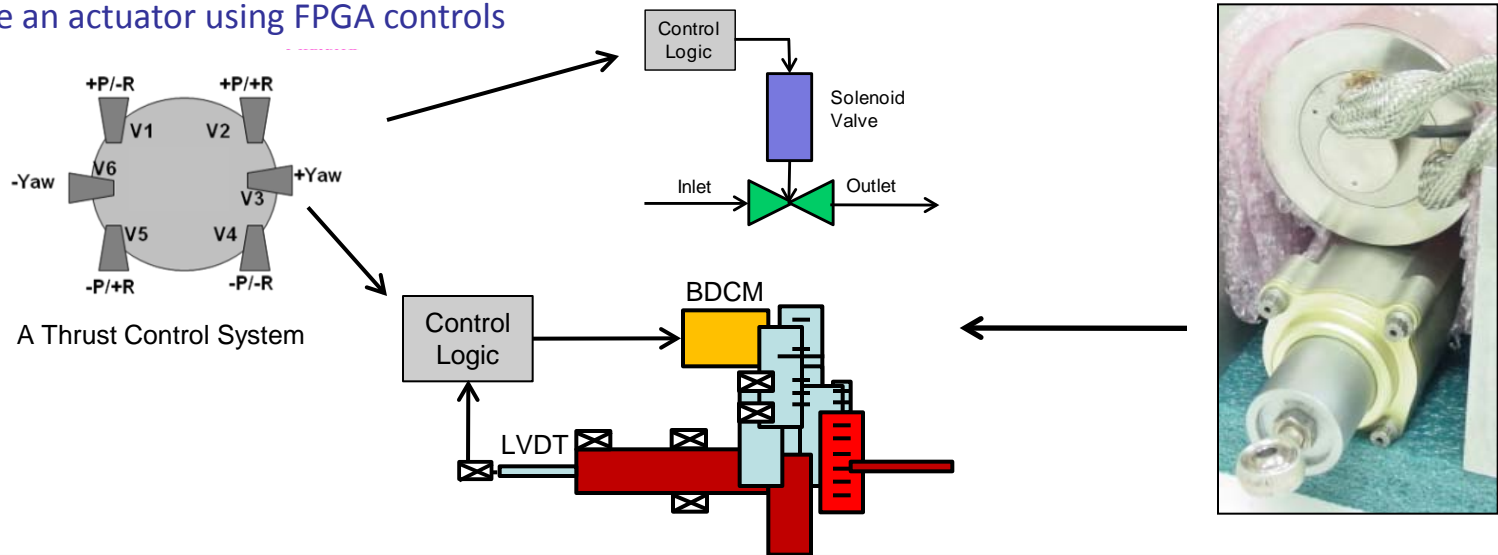
Two motor brushless DC Motor (BCDM) valves

Program started in May 2009, Demonstrated in 7 months

Milestones:

Drive a solenoid using FPGA controls

Drive an actuator using FPGA controls



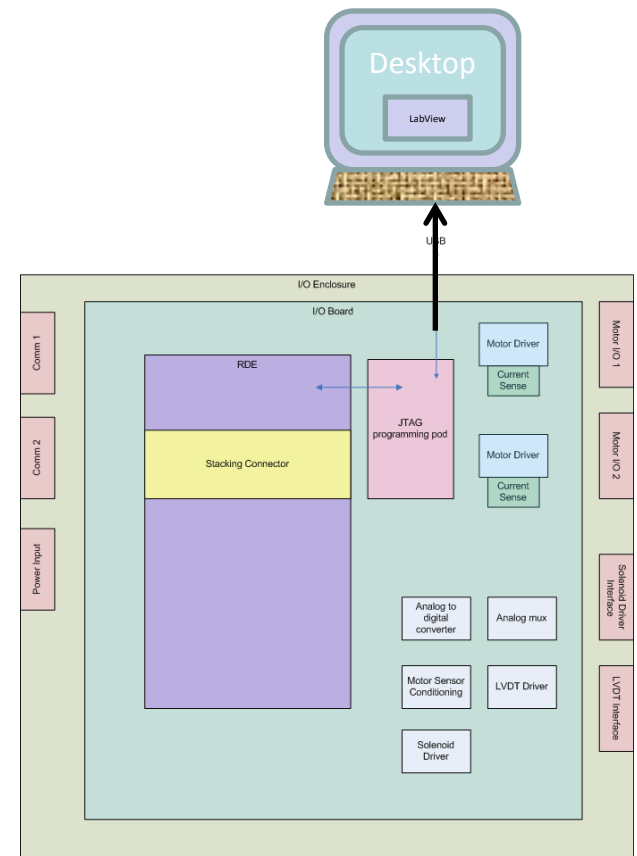
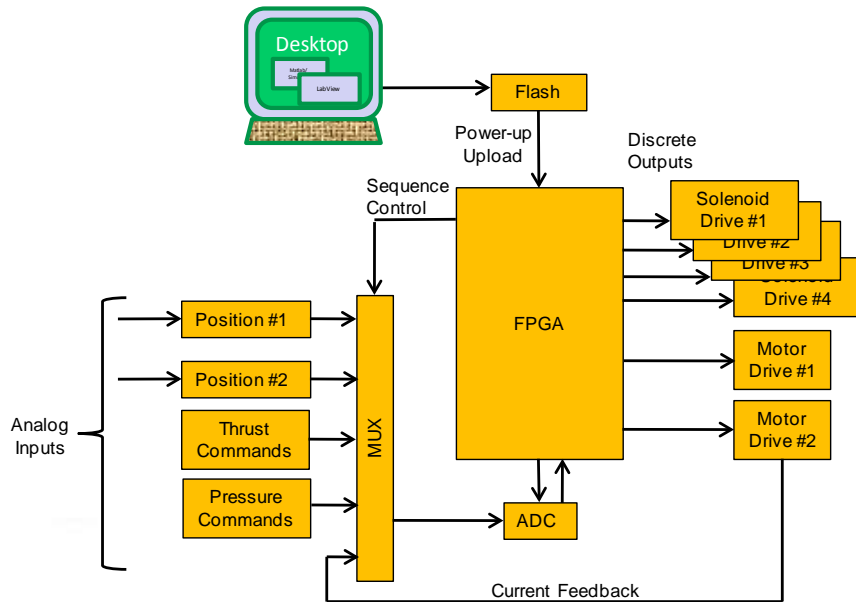
Demonstration Architecture

Project kickoff

Candidate system architecture developed with internal customers

Demonstration

- Hardware built to architecture,
- Control laws integrated with RDE,
- Control of actual flight hardware



Demonstration Integration

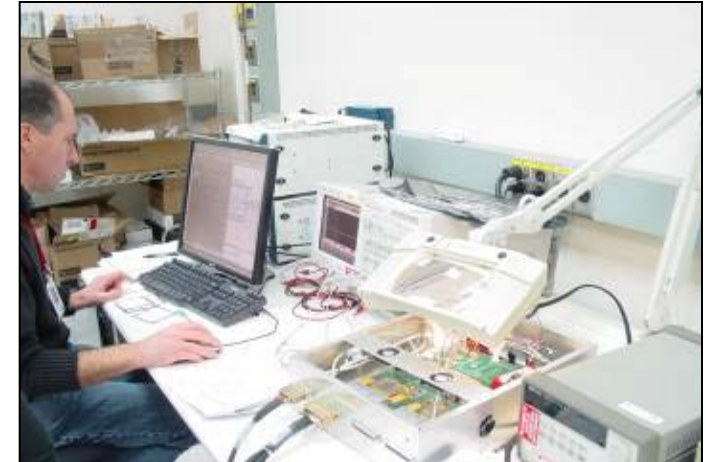
Reused existing actuators, solenoids, and cables

Primary efforts

- Bring-up of RDE LabVIEW FPGA target
- Integration of LabVIEW FPGA and RDE hardware
- Custom electronics for application sensors/effectors
- Conversion of model to LabVIEW

Subsystem pre-integration tests & calibration

- ADC, Conditioning, LVDT, and motor drivers all tested prior to closed loop test
- LabVIEW environment allowed for quick modification of sensor and actuator gains
- LabVIEW also allowed for quick correction of interface debug and integration issues

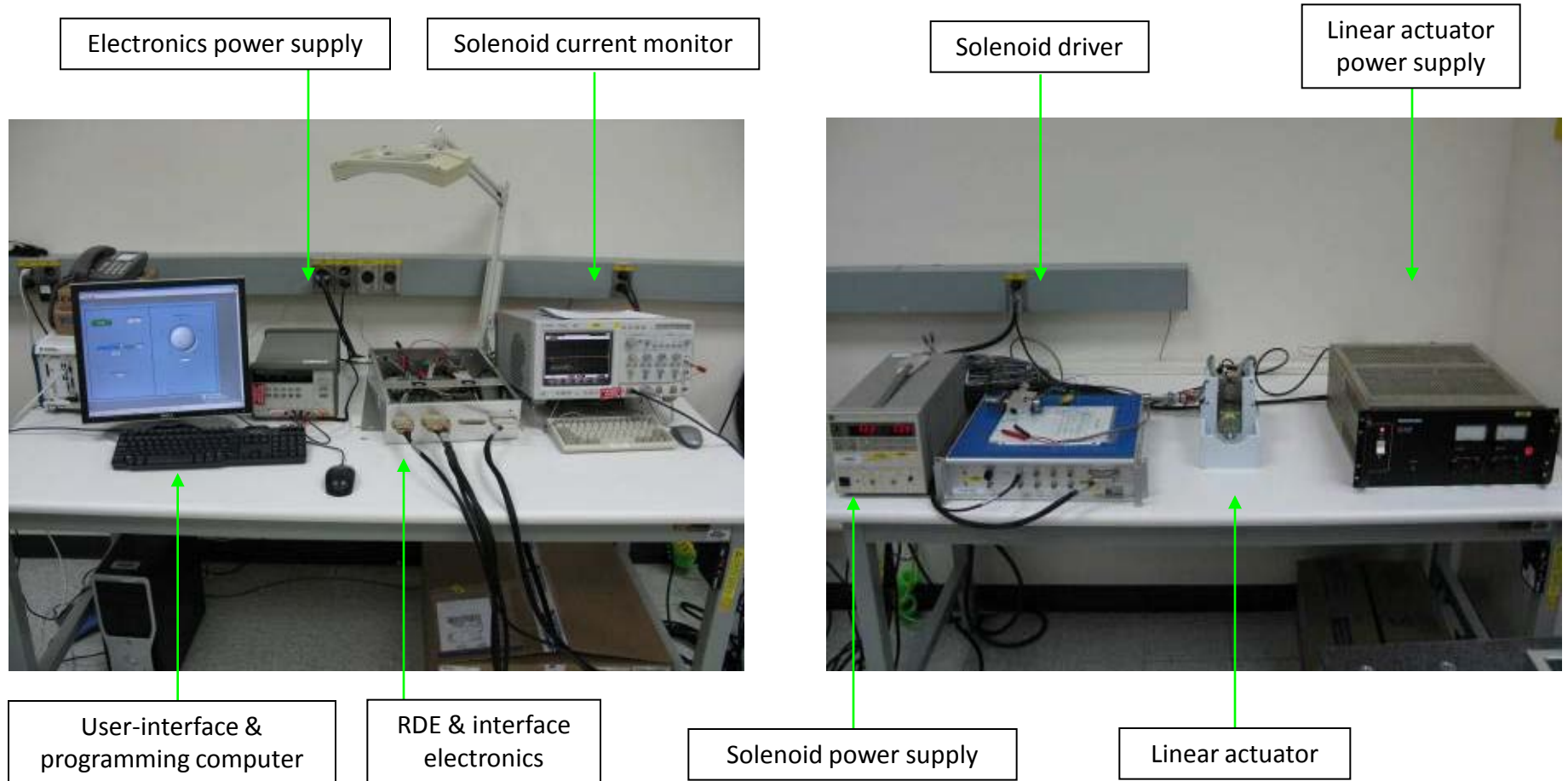


Test setup with RDE controller and custom electronics



Actuator with motor, angle sensor, and LVDT

Demonstration Results



Commercial Responsiveness with Flight Rugged

DESIGN

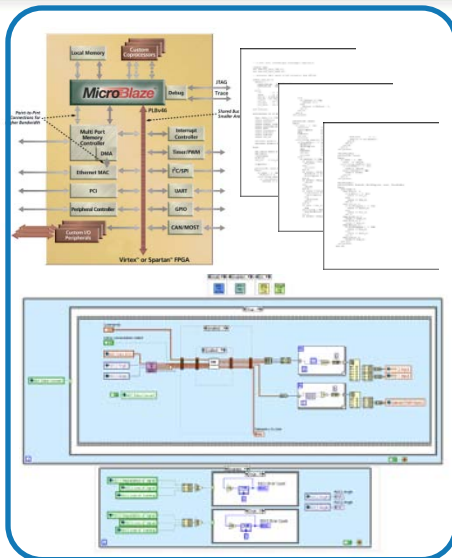
Concept
Iterate on algorithm or model development with real-world stimulus

PROTOTYPE

Verification/Validation
Quickly implement design on COTS hardware devices and validate functionality

DEPLOY

Environmental Test/Flight
Target application to Honeywell RDE with Xilinx Virtex-5QV Rad-Hard FPGA



Conclusions and Next Steps

- The Responsive Digital Electronics platform supports rapid development of complex digital computing and control applications for space.
- Commercially successful FPGA programming tools brings significant cost savings to the development of complex applications.
- Honeywell is moving forward with flight qualification of the Responsive Digital Electronics